REFERENCE DESIGN

RD016 | Gigabit-Ethernet Front End

Dr.-Ing. Heinz Zenkner

01. INTRODUCTION

This document provides the circuit developer with an optimized circuit design and layout with all technical data for a Gigabit Ethernet Front End.

The electronics board has two interfaces, one USB C (USB 3.1) - and one Gigabit RJ45/Ethernet interface. The GB-Ethernet-USB adapter was developed on the basis of the EVB-LAN7800LC Evaluation Board from Microchip. The circuit is built on a 4-layer PCB and in the present design is supplied with voltage via the USB interface. The first part of this Application Note presents the technical basics necessary for understanding the reference design. The second part details the 1 GB Ethernet interface up to the physical layer (PHY in the OSI model). EMC aspects are dealt with in detail in Application Note ANP116.

02. THE 1 GIGABIT ETHERNET INTERFACE

2.1 Data rate, technology, signals

Ethernet was initially distributed worldwide at 10 Mbps (megabits per second) over coaxial cable and later over unshielded twisted-pair lines with 10BASE-T. Today we have 100BASE-TX (Fast Ethernet, 100 Mbps), Gigabit Ethernet (1 Gbps), 10-Gigabit Ethernet (10 Gbps) and 100-Gigabit Ethernet (100 Gbps) at our disposal. For most purposes, Gigabit Ethernet works well with a regular Ethernet cable, specifically using the CAT5e, CAT6 and CAT6a cabling standards. These cable types follow the 1000BASE-T cabling standard, also known as IEEE 802.3ab.

Factors such as network protocol overhead, retransmission due to collisions on the transmission path, or sporadic data errors, limit the maximum usable data rate under normal conditions to 900 Mbps. The average connection speed varies due to many factors, such as the hardware structure of the PC, the number of clients on the router and not least the “quality” of the Ethernet cabling.

The 1 GB Ethernet interface operates according to the 802.3ab-1999 (CL40) standard and requires 4 wire pairs / channels for signal transmission. This results in a symbol rate of 125 megabaud (MBd) with a bandwidth of 62.5 MHz per channel (2 bits per symbol). The GB-Ethernet protocol has some special features. The 1000BASE-T (Gigabit Ethernet) PHY executes a connection configuration protocol known as Autonegotiation. The 8-bit data bytes are converted into 10-bit code groups, the 8B/10B code is robust and has outstanding properties such as transition density, run-length limitation, DC compensation and error robustness. All single, double and triple bit errors in a frame are detected with 100% reliability. The signal voltage for 1000BASE-T averages 750 mV differential; the limits are > 670 mV, < 820 mV at 100 Ω load.

2.2 Interface structure, necessary hardware

RJ45 interfaces are designed for full-duplex transmission, i.e., simultaneous transmission of send and receive data. This is possible because the connector has four wire pairs, whereby one pair is always required for one direction (differential voltage principle). Basically, an unshielded twisted pair (UTP) has an impedance of 100 Ω and a shielded twisted pair (STP) 150 Ω (1000BASE-T: IEEE 802.3, e.g., section 39). In the case of branded cables: CAT5e, 6 and 6a are available both shielded and unshielded, whereas categories 7 and 7a are always shielded. For each RJ45 connection, the IEEE standard requires galvanic isolation with a transformer. This transformer protects the devices from damage due to high voltage on the line and prevents voltage offsets that can arise due to potential differences between the devices. Figure 1 shows the schematic of the interface.

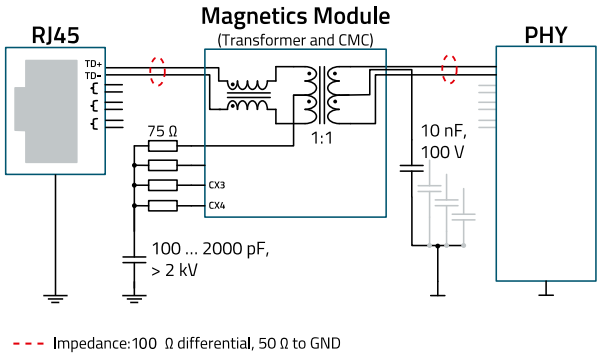


Figure 1: Schematic of the GB-Ethernet interface, one of four channels is shown

The Ethernet signal from the RJ45 interface reaches the transformers via the common-mode choke. Figure 1 shows

one of the four channels. The transformer has a center tap which, in signal terms, represents a zero potential. Asymmetries lead to a voltage at the center tap and are terminated to ground via the 75 Ω resistors, which are AC decoupled via the capacitor. The transformer has a transformation ratio of 1:1. On the secondary side, the Ethernet signal reaches the PHY via the four channels. Here, too, the impedance is 100 Ω differential, or 50 Ω to ground (GND) in each case. The center tap on the secondary side of the transformer is AC connected to ground via capacitors.

03. CONCEPT AND CONSTRUCTION OF THE ADAPTER BOARD

The GB-Ethernet-USB Adapter is available in two different variants.

The V1.0 variant contains discrete components in the Ethernet interface. This means that the matching network and the inductance block, consisting of common-mode chokes and transformers, are individual components placed on the printed circuit board (Figure 2). In the V2.0 variant, the above components are integrated into the housing of the RJ45 jack (Figure 3).

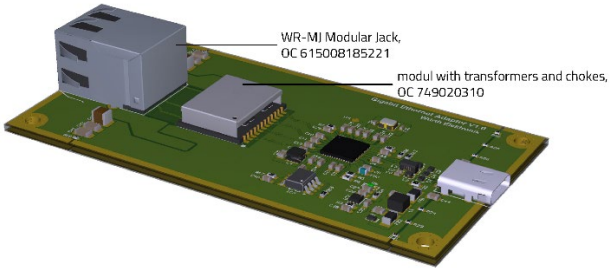


Figure 2: Graphical representation of the GB-Ethernet-USB adapter in the discrete V1.0 version; the module with the transformers and common-mode chokes is placed next to the RJ45 jack.

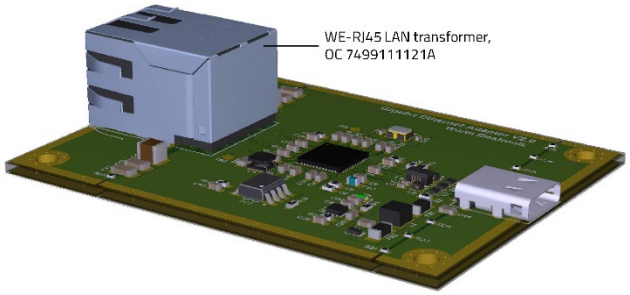


Figure 3: Graphical representation of the GB-Ethernet-USB adapter in the integrated V2.0 variant. The module shown in Figure 2 is integrated into the RJ45 jack.

3.1 Block diagram

The LAN7800 USB 3.1 Gigabit Ethernet controller connects the USB interface to the Ethernet interface as a "bridge" (Figure 4). So only the signal adaptations and decouplings have to be realized for wiring the interfaces. On the USB side, a DC-DC controller generates the 3.3 V supply voltage required for the LAN7800. The LAN7800 requires an additional 4 kbit EEPROM for the firmware.

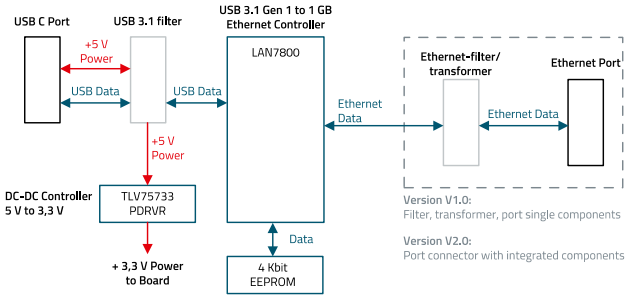


Figure 4: Block diagram of the GB-Ethernet-USB adapter, both variants

The overall schematics of both variants, analogous to the block diagram, are shown in Figure 5 and Figure 6.

3.2 Overall schematic

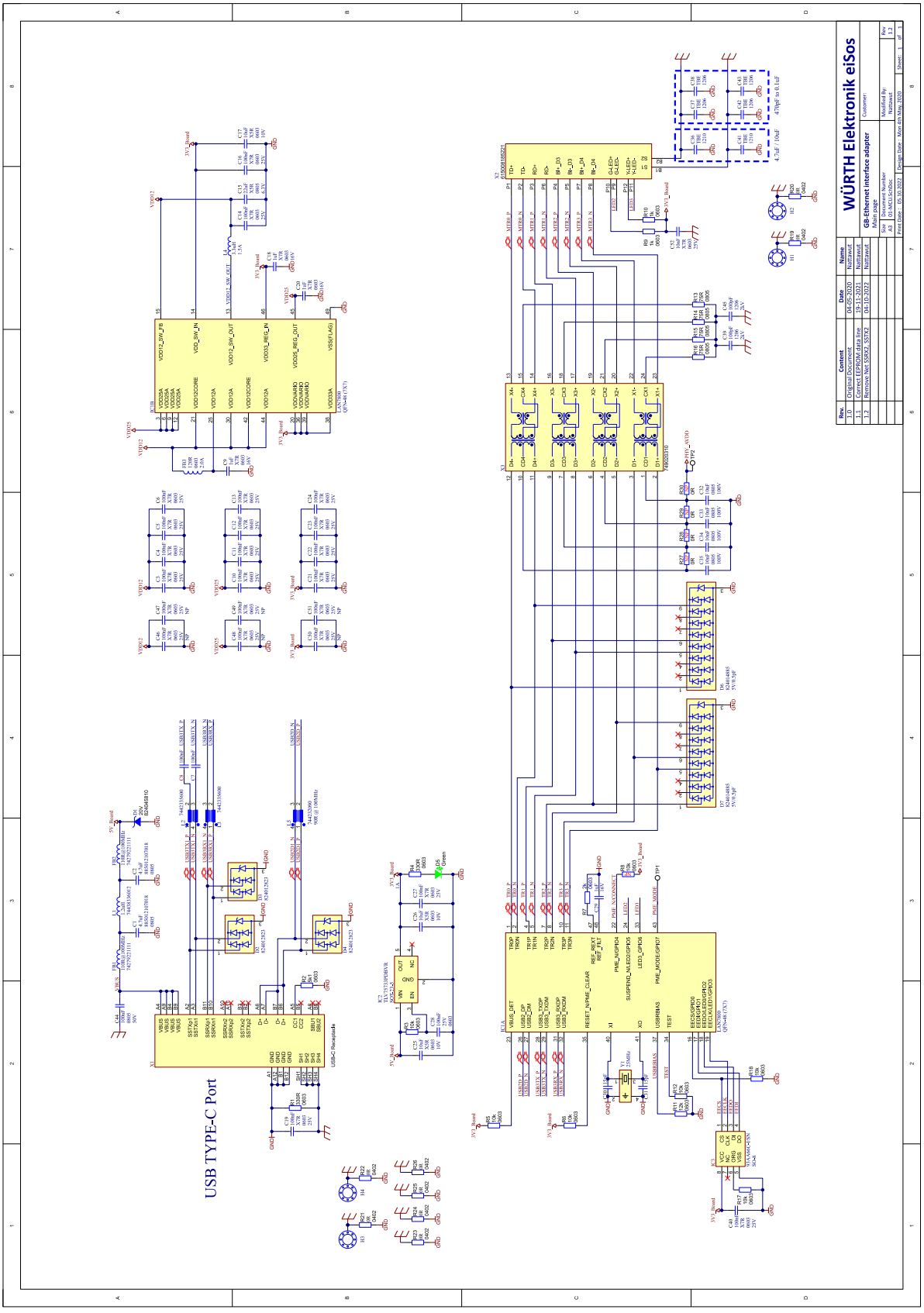


Figure 5: Overall schematic of the GB-Ethernet-USB adapter, V1.0, variant with discrete components at the Ethernet interface

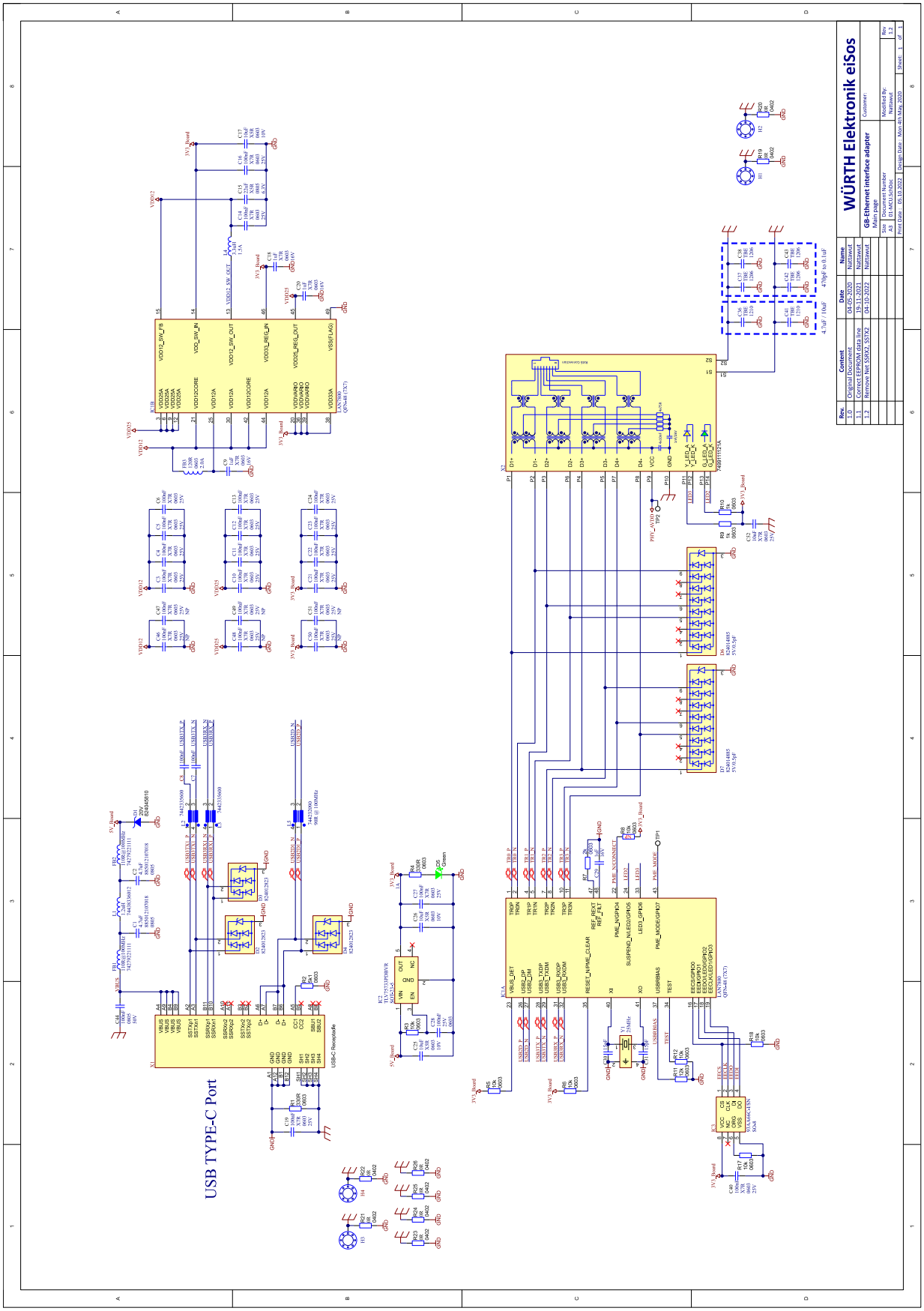


Figure 6: Overall schematic of the GB-Ethernet-USB adapter, V2.0, variant with integrated components at the Ethernet interface

3.3 Subcomponents

The following subcomponents are only briefly discussed here, since this document focuses on the 1 GB-Ethernet interface.

Controller

The LAN7800 is a 1 GB-Ethernet, high-performance USB 3.1 controller with integrated Ethernet PHY. An external 4 kbit EEPROM was connected for the onboard software. The circuit diagram is shown in Figure 7. The upper part of the controller in the figure is the signal section, clocked with a 25-MHz quartz; the lower part is the controller's relatively complex chip-internal power supply.

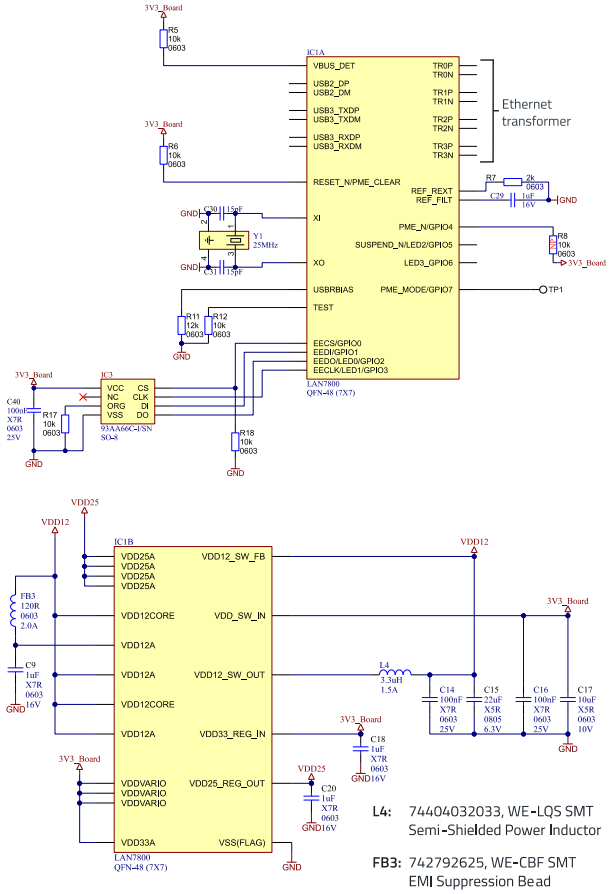


Figure 7: Circuit diagram of the controller, upper part: Signal section, lower part: onboard power supply

Power supply +5 V to +3.3 V

The controller requires a supply voltage of 3.3 V. This is generated with the TLV757P linear regulator in this case. The LDO (low dropout regulator) reduces the voltage from 5.0 V to 3.3 V. The 10 µF input and output electrolytic capacitors ensure stable operation, and the 100 nF X7R capacitor reduces high-frequency interference.

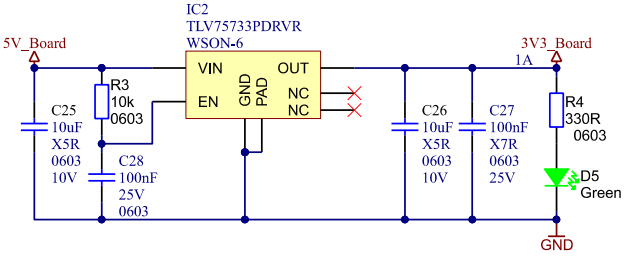


Figure 8: Circuit diagram of the DC-DC converter from +5 V to 3.3 V

USB 3.1 interface

Figure 9 shows the circuit diagram of the USB interface The data lines are connected with common-mode chokes against radio interference and with TVS diode arrays against transient overvoltages. The PCB ground (GND) is connected to the GND terminals of the cable at X1, but to the housing via a capacitor (C19) and a resistor (R1).

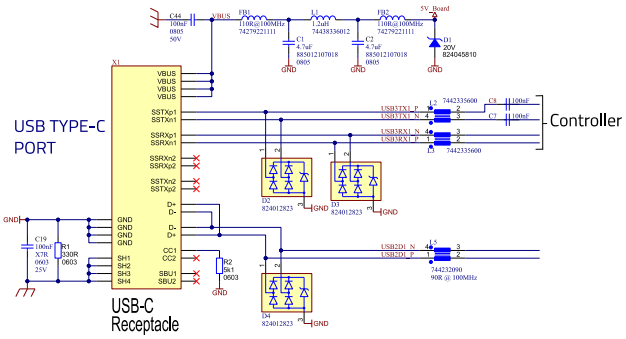


Figure 9: Circuit diagram of USB interface with power supply filter

If the capacitor C19 is fitted, the connection between GND and the housing/shielding connection is also high-frequency and low-impedance. If the circuit is installed in a metal housing, it may be advantageous for improving EMC (emission and immunity) to fit an SDM ferrite (e.g., 742792642) instead of C19. R1 is then omitted. The connection remains galvanic via the housing and the PCB mounting holes. The high-frequency reference point shifts from the electronics / controller, to the housing, however. This means that any interference there may be in the immediate vicinity of the controller at its ground connections is not conducted into the cable. The +5 V power supply at X1 is extensively filtered.

C44 blocks high-frequency interference directly against the housing, after which the supply voltage is broadband decoupled via FB1, L1 and FB2 with capacitors C1 and C2 configured as a Double-π- filter. D1 is a TVS diode that limits transient overvoltage from 25 V up to a peak current of 80 A. As this diode has a parasitic capacitance of 240 pF, FB2 forms an effective low-pass filter against high-frequency interference.

3.4 Ethernet interface

The Ethernet transformer (LAN transformer) is the interface between the device and the Ethernet cable. The transformer provides the safety-relevant galvanic isolation between device and cable while providing impedance matching to the internal logic on the one hand and to the balanced wire pairs, on the other. The transformer also protects the device from transient interference, suppresses common mode signals between the transceiver IC and the cable, both from the device to the outside as well as from the outside cable to the electronics in the device. The component must also transmit broadband data up to 1 Gbps, however, without significantly attenuating the signal transmitted and received. Additional components are necessary to achieve matching and satisfy EMC requirements. There are two approaches to building the interface:

1. The use of a ready-made module, which integrates the Ethernet jack, the transformer and the Bob Smith termination, is the V2.0 variant described above.
2. A setup with discrete technology, in this case V1.0 variant. All components must be adapted to each other in this case, but the solution offers more degrees of freedom while the selection of components as well as the configuration and the layout are left to the developer. Although a little more design work is required, the discrete version is less expensive and, for special requirements, isolation voltages of up to 6 kV can be achieved.

As there is no functional difference between the two variants, the circuitry of the GB-Ethernet interface is explained below using the V1.0 variant with discrete components.

3.5 Circuit description of the 1 GB Ethernet front end

The LAN transformer X3 in Figure 10 provides DC isolation between the electronics and the network cable. The minimum test voltage for the transformer between primary and secondary is 1,500 V_{RMS}.

WE-LAN AQ transformer 749020310

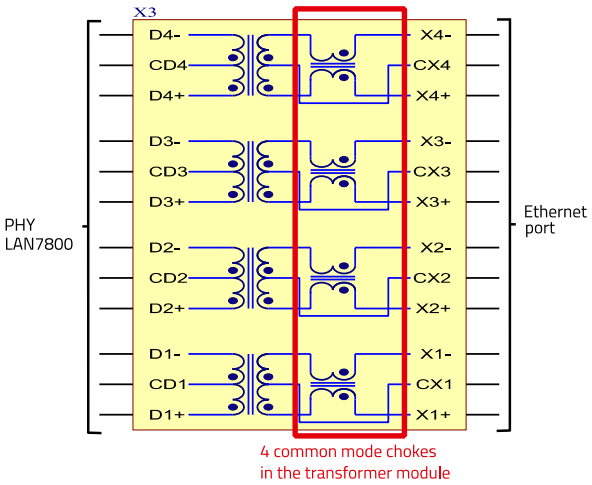


Figure 10: WE-LAN AQ transformer for galvanic isolation between the PHY and the Ethernet network

The center tap of the primary side winding, i.e., to the Ethernet port, has the "Bob Smith" termination mentioned above (Figure 11). For each wire pair, a 75 Ω resistor is connected to form a "star point", the whole circuit is then galvanically isolated and connected to the chassis ground by means of two parallel 100 pF capacitors; capacitors up to 2 nF are mentioned in the literature, which is a relatively high value in relation to the frequency range. The capacitors should have a dielectric strength of at least 2 kV.

The "Bob Smith" termination is used to reduce interference caused by common-mode current flows as well as susceptibility to interference from unused wire pairs on the RJ45 connector.

Bob Smith referenced an impedance of about 145 Ω per wire pair. Due to the wealth of cable types on the market, the differences in the base impedances of the various cable types, and the fact that the cables do not have a constant impedance over the length caused by twisting, common-mode chokes were also implemented (Figure 10). In the X3 module, for example, one transformer and one common-mode choke are connected together per channel. These chokes cannot correct impedance matching deviations, but they do significantly improve EMC.

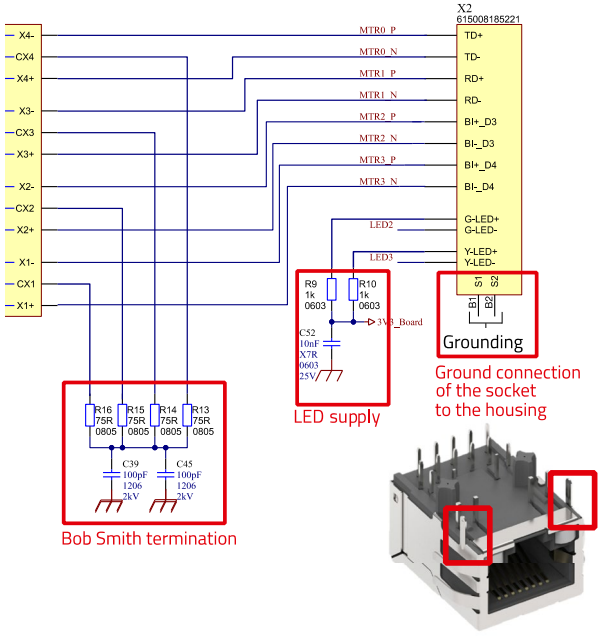


Figure 11: Primary interface zone between the Ethernet jack and transformer

R9, R10 and C52 in Figure 11 are provided to supply power to the LEDs integrated in the connection jack. The two connections B1 and B2 at the X2 Ethernet jack must be connected directly, i.e., with low impedance (!) to the chassis ground. This connection is crucial for the shield connection of the cable and thus for the "quality" of the shielding attenuation.

With C36 to C38 and C41 to C43 (Figure 12), the shielding of the Ethernet jack and therefore also the cable shield can be connected to the board ground (GND).

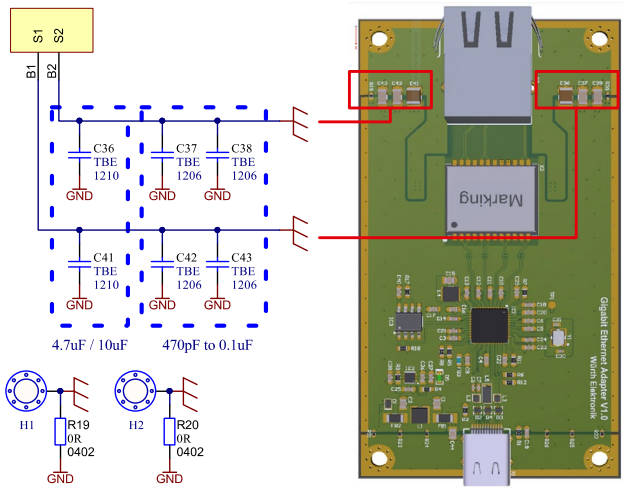


Figure 12: Capacitors for connecting between the board GND and the shield ground or housing

With sheet metal housing, it makes sense not to fit these capacitors and to connect the electronics GND directly to the housing with screw connections. For plastic housing, the capacitors should be fitted to connect the Ethernet cable shield to the reference ground. The 0 Ω R19 and R20 resistors serve the same purpose, but there is no galvanic isolation as would be realized with the capacitors. The alternative fitting options are provided here for "experimental" purposes, the Application Note ANP116 goes into this in more detail.

The capacitors C32 to C35 in Figure 13, on the secondary side of the transformers, connect the center taps of the transformers with the ground (GND) for HF.

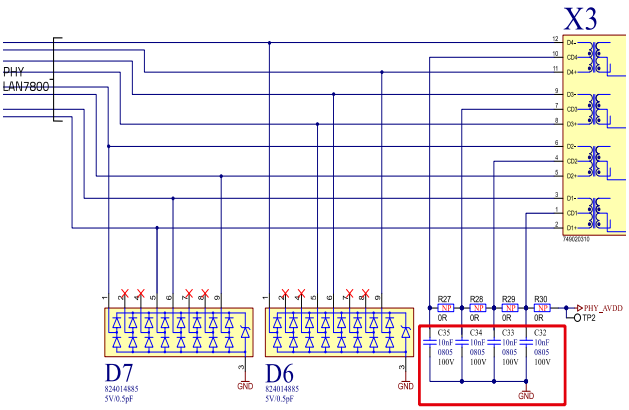
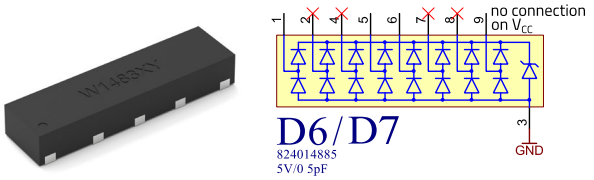


Figure 13: Secondary interface zone between the transformer and the PHY

To avoid DC equalization currents from the PHY, galvanic isolation using capacitors is necessary. Resistors R27 to R30 are provided based on the requirements of some PHY manufacturers (current-mode line driver option), but are usually not needed when the PHY is operating in standard voltage mode.

The TVS diode arrays D6 and D7 are indispensable, however, as they limit transient interference occurring on the interface side to the PHY to the circuit ground (GND). On the secondary side, i.e., after the transformers of the X3 module, the transient interference occurs in common mode, so a TVS diode must be connected to the reference ground at each transformer connection. However, the interference level is lower on the secondary side of the transformer than on the primary side. Low impedance connection of the diodes is important for the function of the TVS diodes, looped into the signal lines, on the one hand, and to ground, on the other. The TVS diode arrays WE-TVS (824014885) used here feature a particularly low parasitic capacitance. Besides the array's special Schottky diodes, the "absent" connection to the positive supply voltage also helps achieve low parasitic capacitance (Figure 14). The "C_{cross}" value of 0.08 pF is the capacitance with which the Ethernet signal is loaded. Nevertheless, it should not be forgotten that the parasitic

capacities of the entire design must be added: solder pads, vias, capacitances between components and the housing.



Properties		Test conditions	Value			Unit	
			min.	typ.	max.		
Channel Operating Voltage	V_{Ch}	I/O to GND			5	V	
(Reverse) Breakdown Voltage	V_{BR}	I/O to GND; I_{BR}=1mA	6		9	V	
Channel (Reverse) Leakage Current	$I_{Ch\ Leak}$	I/O to GND $V_{I/O}$=V_{Ch}; V_{GND}= 0V			1	µA	
Forward Voltage	V_F	GND to I/O; I_F=15mA		0.9	1.2	V	
(Channel) Input Capacitance	C_{Ch}	I/O to GND $V_{I/O}$=2.5V; V_{GND}=0V; f=1MHz		0.5	0.65	pF	I/O to GND
Channel to Channel Input Capacitance	C_{Cross}	between I/O pins $V_{I/O}$=2.5V; V_{GND}=0V; f=1MHz		0.03	0.08	pF	I/O to I/O
Channel ESD Clamping Voltage	$V_{Ch\ Clamp\ ESD}$	IEC 61000-4-2 +8kV (TLP=16A) Contact Mode; I/O to GND		10.5		V	
Polarity	Unidirectional						

Figure 14: TVS diode array WE-TVS (824014885) with its very low parasitic capacitance

3.6 Component placement and layout of the 1 GB Ethernet front end

Layout is an essential factor in the design of circuits with high-frequency signals, or signals with very short rise times. The layout of the GB-Ethernet design must also be HF-compatible.

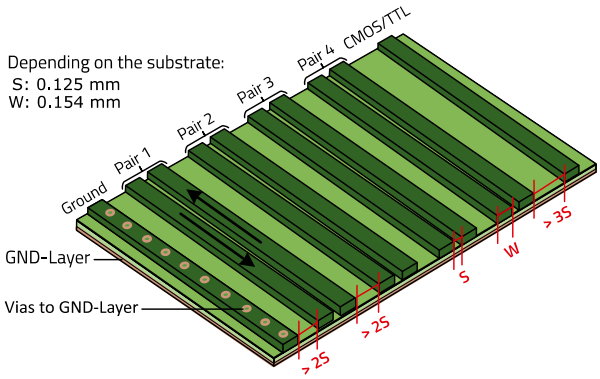


Figure 15: Schematic representation of the dimensions for the layout of the traces

With reference to Figure 15, the following points should be noted:

1. It goes without saying that a PCB with a minimum of 4 layers must be used.
2. The VCC and GND layers are on the inside.
3. Spacing from other traces to Ethernet traces to avoid coupling: > 3S
4. Spacing between the Ethernet signal traces and the GND islands in the same plane: > 2S
5. Spacing between adjacent Ethernet difference pairs: > 2S

Additional points to consider:

1. The blocking capacitors for the PHY must be placed directly beside the IC.
2. 4.7 µF / 0.1 µF / 1 nF capacitors on each VCC pin.
3. Inductance of the traces to the components L < 1.5 nH – 2 nH, i.e., connections shorter than 2 mm between capacitor and the IC pin.

An essential point is the maximum signal skew (propagation delay time) of the wires within a pair (intra-pair) and between the pairs (inter-pair). The maximum "skew" values can be found in the Ethernet specification (IEEE 802.3-2008 standard), general reference values:

1. Maximum length offset between the wire pairs (inter-pair): 50 mm (< 330 ps)
2. Maximum skew within a wire pair (intra-pair): < 1.6 ps corresponding to 250 µm

The conversion between temporal and path offset is achieved with the following relationship:

$$V_P = \frac{C}{\sqrt{\varepsilon_r}} \longrightarrow V_{P\,(FR4)} = \frac{299{,}792{,}458\,\frac{mm}{s}}{\sqrt{4.2}} = 146.28\,\frac{mm}{ns}$$

V_P: propagation speed (mm/ns)

C: speed of light

ε_r: dielectric permittivity of the PCB material

The following Figure 16- Figure 19 show the layout regions of the Ethernet interface; according to the figures, the explanation follows.

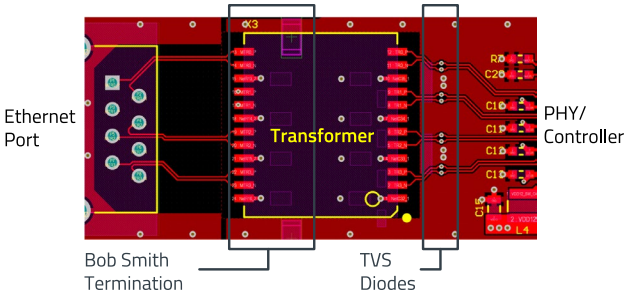


Figure 16: Top layer with positioning of the "Bob Smith" components and the TVS diodes

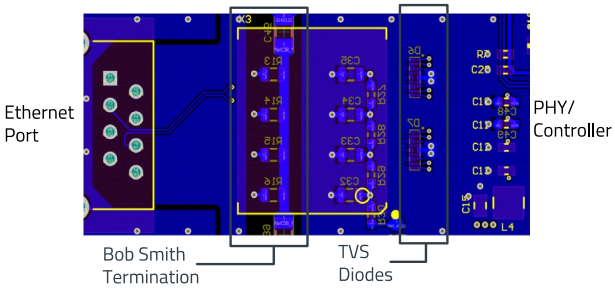


Figure 17: Bottom layer with positioning of the "Bob Smith" components and the TVS diodes

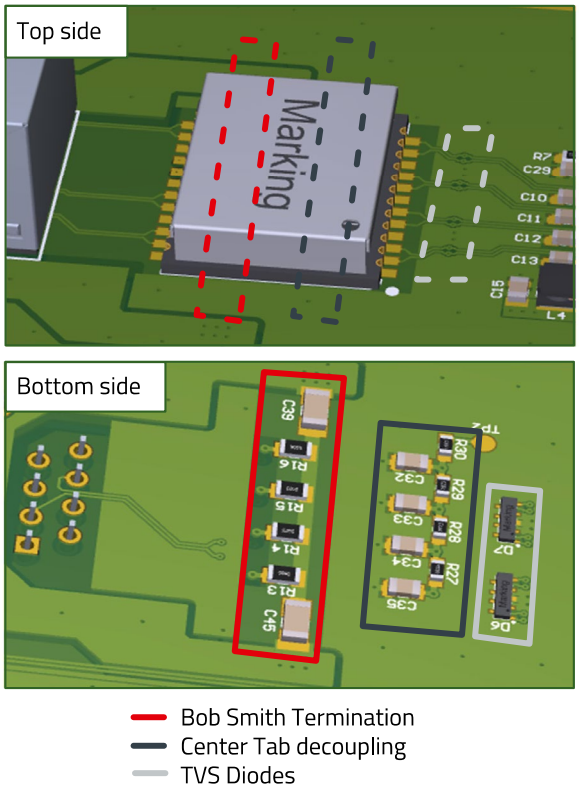


Figure 18: 3D view with positioning of the "Bob Smith" components and the TVS diodes

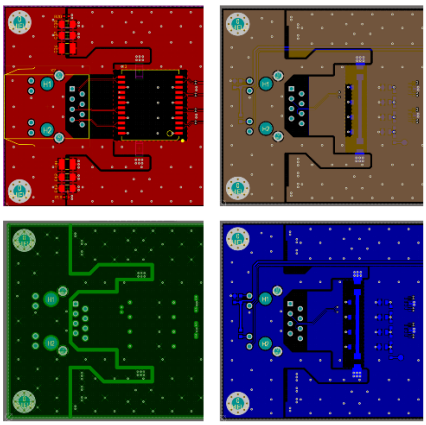


Figure 19: The four layers of the interface zone in the same section

Layout considerations, with reference to Figure 16 to Figure 19:

1. The TVS diode arrays must be connected directly into the signal path and to GND so as to avoid a voltage drop due to parasitic inductance. An extract of the layout Figure 16 is shown in Figure 20.

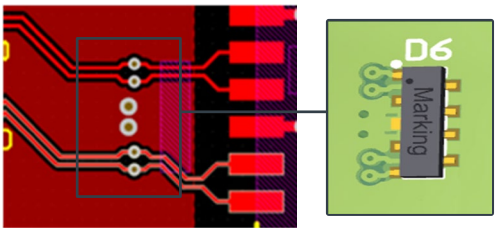


Figure 20: Layout extract, via pads of the TVS diode array routed into the signal path

2. The chassis/connector ground SGND is separated from the electronics GND in all four layers.
3. The SGND layers must not overlap with other layers, as otherwise capacitive coupling will occur.
4. Ground planes through-contacted with a pitch of approx. 4 mm (vias).
5. Symmetrical signal lines, differential impedance of 100 Ω to reference ground.
6. Symmetrical signal lines:
   - Width of the traces: 0.154 mm
   - Spacing between the traces: 0.125 m
   - Spacing of the signal to the reference plane (prepreg thickness): 0.2 mm

04. SUMMARY, LIST OF ESSENTIAL POINTS FOR THE DESIGN

1. Chassis/jack ground to electronics GND is separated in all four layers. This avoids that the surfaces of the chassis ground overlap with other layers in order to keep capacitive coupling as low as possible.
2. The ground planes are connected to each other with a pitch of approx. 4 mm by means of vias.
3. The signal lines coming from the Ethernet jack are symmetrical, with a differential impedance of 100 Ω routed to the reference ground. The conductor pairs have a trace width of 0.154 mm and are spaced 0.125 mm apart. Spacing of the signal to the reference plane (prepreg thickness): 0.2 mm
4. The Ethernet jack is positioned at the edge of the PCB to ensure a low-impedance connection to a metal housing, if necessary. The transformer (X3) is placed in close proximity in order to keep the electrical coupling influences or impairments caused by long conductor paths to a minimum.
5. As on the primary side, a differential impedance of 100 Ω to the reference ground must also be maintained

on the secondary side of the transformer module for the traces. The TVS arrays must be connected directly into the signal path and to GND so as to avoid a voltage drop due to parasitic inductance.

6. Each TRxP/TRxN signal group should be routed as a differential trace pair. This includes the entire length of the traces from the RJ45 connector to the PHY. The differential pairs should be as short as possible and have a differential impedance of 100 Ω i.e., each 50 Ω to ground.
7. Differential pairs should be routed as close to each other as possible. The smallest trace spacing (0.1 - 0.13 mm) is typically selected at the start of impedance calculation. Then the width of the trace is adjusted to achieve the required impedance. This ensures high coupling between the signal pairs.
8. Differential pairs should be routed away from all other traces to avoid coupling to other traces and therefore asymmetry. The spacing should be at least 4 mm. The intra-pair and inter-pair offset between the signal pairs should be less than 1.3 mm over the full length. To achieve optimum interference immunity, each pair should be routed as far apart as possible.
9. For optimal separation, GND planes can be inserted between differential pairs. A spacing of 3-5 times the dielectric spacing (spacing between the copper layers within the PCB) should be maintained from this ground plane to one of the traces.
10. The use of vias has to be minimized. If vias are used, they must be adapted such that the differential pairs remain symmetrical. Shifting of layers has to be minimized. The differential pairs must be referenced to the same power supply plane / ground plane. Routing must never be via different planes!
11. If the four differential pairs are routed from the PHY to the RJ45 jack, generally at least one pair requires a via to the external plane on the other side. In this case, it must be ensured that routing on the other side of the board (usually layer 4) is via a continuous reference plane with low impedance to ground.
12. All impedance terminations must always be referenced to the same reference plane as the differential lines. The resistive terminations, i.e., resistors, should have a 1.0% tolerance. All capacitive terminations, i.e., capacitors in the Ethernet front end, should have tight tolerances and high-quality dielectrics.

05. FINAL REMARKS

The 1 GB USB 3.1 – Interface Board was originally developed as an EMC test board to investigate the performance of different EMC concepts. The results of this may be found in Application Note ANP116. Numerous requests for design details of a 1 GB Ethernet interface have helped make this document available to our customers as a reference design. The details described here should allow you to build a replica of a 1 GB Ethernet interface without any problems. The data for Altium Designer®, as well as the Gerber data, are available on our homepage for unrestricted use.

IMPORTANT NOTICE

The Application Note is based on our knowledge and experience of typical requirements concerning these areas. It serves as general guidance and should not be construed as a commitment for the suitability for customer applications by Würth Elektronik eiSos GmbH & Co. KG. The information in the Application Note is subject to change without notice. This document and parts thereof must not be reproduced or copied without written permission, and contents thereof must not be imparted to a third party nor be used for any unauthorized purpose.

Würth Elektronik eiSos GmbH & Co. KG and its subsidiaries and affiliates (WE) are not liable for application assistance of any kind. Customers may use WE's assistance and product recommendations for their applications and design. The responsibility for the applicability and use of WE Products in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate and investigate, where appropriate, and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not.

The technical specifications are stated in the current data sheet of the products. Therefore the customers shall use the data sheets and are cautioned to verify that data sheets are current. The current data sheets can be downloaded at www.we-online.com. Customers shall strictly observe any product-specific notes, cautions and warnings. WE reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services.

WE DOES NOT WARRANT OR REPRESENT THAT ANY LICENSE, EITHER EXPRESS OR IMPLIED, IS GRANTED UNDER ANY PATENT RIGHT, COPYRIGHT, MASK WORK RIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHT RELATING TO ANY COMBINATION, MACHINE, OR PROCESS IN WHICH WE PRODUCTS OR SERVICES ARE USED. INFORMATION PUBLISHED BY WE REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE A LICENSE FROM WE TO USE SUCH PRODUCTS OR SERVICES OR A WARRANTY OR ENDORSEMENT THEREOF.

WE products are not authorized for use in safety-critical applications, or where a failure of the product is reasonably expected to cause severe personal injury or death. Moreover, WE products are neither designed nor intended for use in areas such as military, aerospace, aviation, nuclear control, submarine, transportation (automotive control, train control, ship control), transportation signal, disaster prevention, medical, public information network etc. Customers shall inform WE about the intent of such usage before design-in stage. In certain customer applications requiring a very high level of safety and in which the malfunction or failure of an electronic component could endanger human life or health, customers must ensure that they have all necessary expertise in the safety and regulatory ramifications of their applications. Customers acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of WE products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by WE.

CUSTOMERS SHALL INDEMNIFY WE AGAINST ANY DAMAGES ARISING OUT OF THE USE OF WE PRODUCTS IN SUCH SAFETY-CRITICAL APPLICATIONS.

USEFUL LINKS


Application Notes
www.we-online.com/appnotes


REDEXPERT Design Plattform
www.we-online.com/redexpert


Toolbox
www.we-online.com/toolbox


Product Catalog
www.we-online.com/products

CONTACT INFORMATION

appnotes@we-online.de
Tel. +49-7942-945-0

Würth Elektronik eiSos GmbH & Co. KG
Max-Eyth-Str. 1 · 74638 Waldenburg
Germany
www.we-online.com