

# APPLICATION NOTE

## ANS020 | Digital isolators



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### 1. INTRODUCTION

The electrotechnical infrastructure has become very complex in recent years, whether in the industrial environment or in building technology. The decentralized recording of physical parameters is "state of the art" and high-performance micro-controllers facilitate the processing of data. However, recording the data from the object is often a challenge and wireless transmission of the data is frequently not possible. The data must be recorded from the object in such a way that the probe does not influence the quantity being measured as much as possible, otherwise measurement errors will occur. This requires electrical decoupling, which must be realized in the circuitry. Furthermore, the wired transmission of the data must be potential-free and symmetrical so that the transmission is not disturbed by electromagnetic coupling and ground loops. In this application, the use of microcontrollers was deliberately avoided in order to demonstrate that a high-performance, interference-free design can be realized with little effort using analog circuit technology. The design is divided into two circuits, a transmitter and a receiver.

The transducer can record a DC voltage of  $\pm 30 V_{max}$  with a fluctuation period of one second. The current consumption has been kept low. With a power supply of +15 V,

it is  $<85 \text{ mA}$  for the transmitter and  $<25 \text{ mA}$  for the receiver. Both the transmitter and the receiver are galvanically isolated, at the transmitter between the measurement data acquisition and the signal transmission path and at the receiver between the signal transmission path and the data output. Special DC-DC power modules and digital isolators with galvanic isolation and particularly low parasitic coupling capacitance were used to realize this isolation in the circuitry. The signal is transmitted between the transmitter and receiver via a two-wire cable. Depending on the electromagnetic environmental influences, the distance can be several hundred meters

### 2. BASIC CIRCUIT DESIGN OF A POTENTIAL-FREE VOLTAGE SENSOR

#### 2.1 Basic Circuit Design-Transmitter

Figure 1 shows the block diagram of the transmitter.

The circuit is divided into six blocks:

- 1. Probe:** Transducer with voltage divider and amplifier for measuring positive and negative polarity.
- 2. Level shifter:** Level shifter for the voltage-frequency converter.

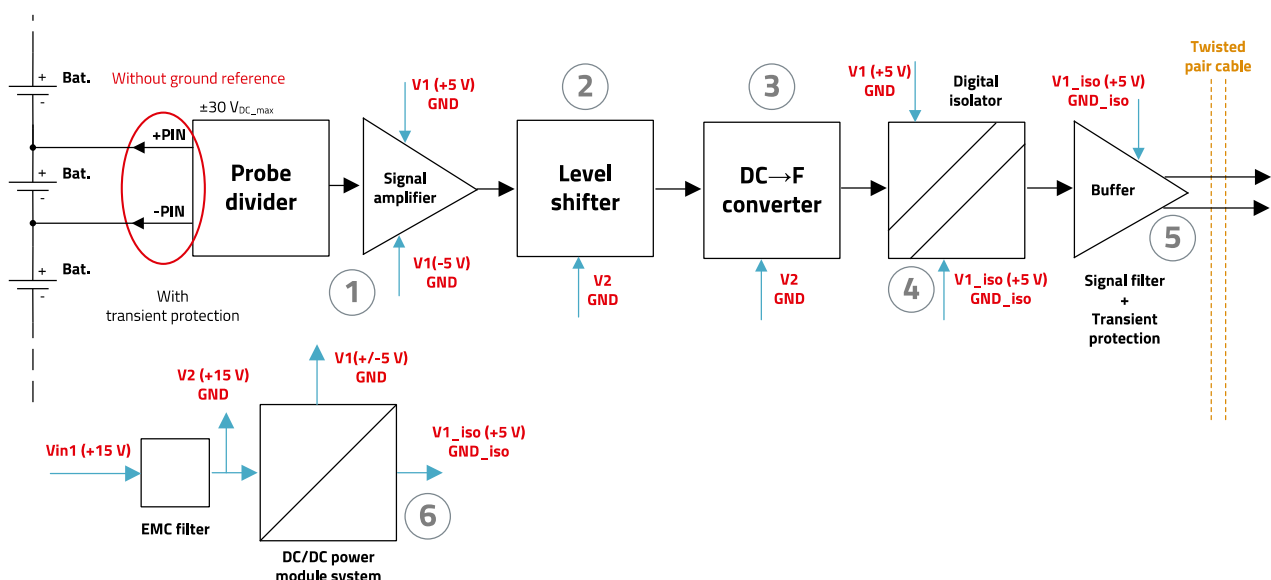


Figure 1: Block diagram of the transmitter for potential-free voltage measurements.

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3. **Voltage-to-frequency converter:** Digital output signal, frequency dependent on the input voltage.
4. **Digital isolator:** Galvanic isolation between measuring potential and interface.
5. **Interface buffer:** Low-impedance line driver with balanced output.
6. **Power supply:** DC/DC converter, galvanically isolated converters for the probe head section.

The block diagram shows that the design cannot be realized without EMC circuitry measures. To ensure functional reliability, transient protection and filters are provided both on the probe side and at the driver output; low-pass filters are also provided before and after the DC-DC power modules to effectively attenuate RF coupling.

### 2.2 Basic Circuit Design-Receiver

Figure 2 shows the receiver's block diagram. The circuit is divided into five blocks:

1. **Input buffer:** Signal pick-up, signal conditioning with balanced input. The link indicator shows whether there is a detectable connection to the transmitter.
2. **Digital isolator:** Galvanic isolation between input signal and secondary signal processing / output interface. Additional galvanically isolated voltage for the input-side buffer.

3. **Frequency-to-voltage converter:** Generates an output voltage from a digital signal. The voltage level depends on the frequency of the input signal.
4. **Interface buffer with polarity indicator:** Level converter for the output signal. The output signal has a positive polarity, the polarity indicator shows the polarity of the input signal.
5. **Power supply:** DC/DC converter for the secondary-side supply

Numerous EMC measures are also provided in the receiver section. The signal input coming from the twisted pair cable is equipped with transient protection and a common mode filter to effectively attenuate interference coming from the cable. The power supplies around the DC-DC converters are equipped with low-pass filters on both the input and output sides in order to significantly reduce both external electromagnetic interference and electromagnetic emissions from the DC-DC converters within the switching unit. This ensures a high signal-to-noise ratio and a high level of functional reliability.

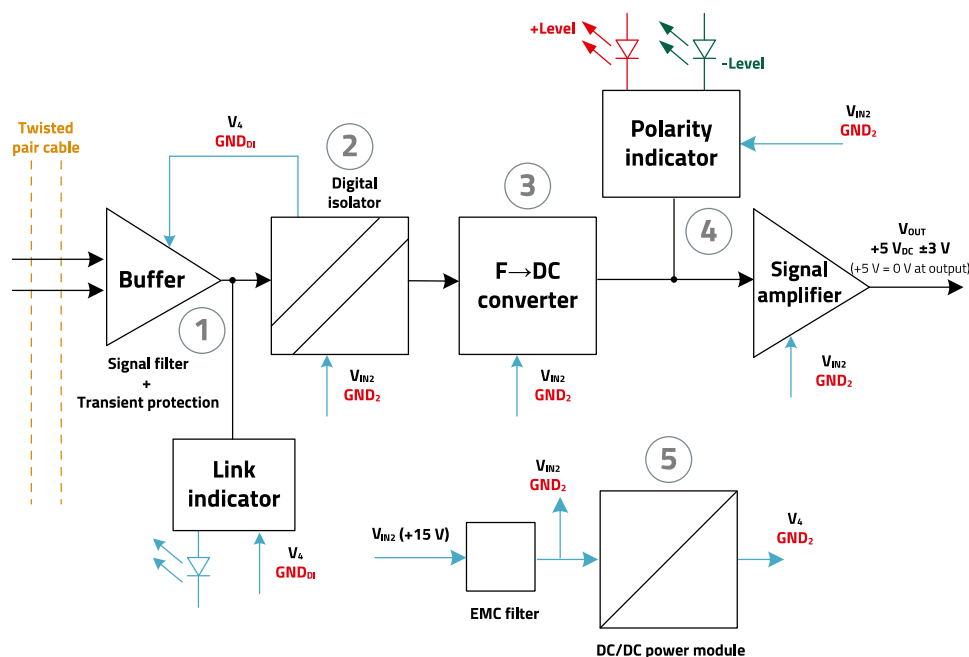


Figure 2: Block diagram of the receiver for potential-free voltage measurement.

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### 3. KEY COMPONENT DIGITAL ISOLATOR AND ITS SPECIFIC PARAMETERS

Interference-free data communication and personal safety are two major challenges for electronics in this type of industrial environment. Strong electromagnetic fields, overvoltages, transient voltages and high EMC interference are the order of the day. If, for example, the communication line is laid unfavorably close to a control line of a frequency inverter, the pulses are capacitively coupled and the signals in the communication line oscillate with the pulse pattern of the frequency inverter. This interference can quickly reach a level where significant malfunctions occur and even the safety of people can be jeopardized.

If, for example, the temperature of a motor is measured with a thermocouple, voltages in the millivolt range are generated. If these voltages are now transmitted over a cable length of several meters to a central control unit that refers to a different earth potential, the measurement signal is distorted by the potential differences.

#### 3.1 Functions of an Isolator

Clustering the described phenomena, the following four challenges emerge:

- A safety barrier between hazardous voltages and a user
- Separation of ground loops between spatial circuits
- Minimization of common-mode interference
- Interference-free data transmission

Figure 3 shows the situation of the data transmission system graphically. In order to meet the requirements of shielding dangerous voltages from the user and still guarantee interference-free data transmission, galvanic isolation must be used to separate the zones electrically, i.e. potentially from

each other, so that they can work separately and thus without interference.

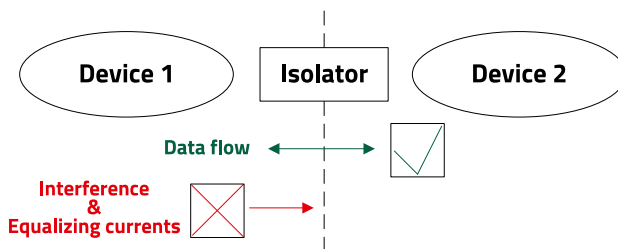


Figure 3: Basic concept of an isolated system to separate different potentials

The data flow runs via an isolator, but interference and potential equalization currents are held back by the galvanic insulation of the isolator.

#### 3.2 Capacitive Digital Isolator

The digital isolator (block-diagram Figure 4) consists of an oscillator and a modulator on the primary side. On the secondary side are a demodulator and a buffer.

The primary-side components are galvanically separated from the secondary-side components by a capacitor structure with an isolation barrier made of SiO<sub>2</sub>.

Signal transmission through the isolation barrier is realized by a modulation method known as on/off keying. The oscillator integrated in the chip is used to modulate the Schmitt-triggered input signal. The modulator generates a differential signal that is transmitted via the capacitively isolated lines.

The demodulator is located on the secondary side and is used to amplify, filter and reconstruct the input signal. The signal delay and distortion are minimal. Finally, the signal from the

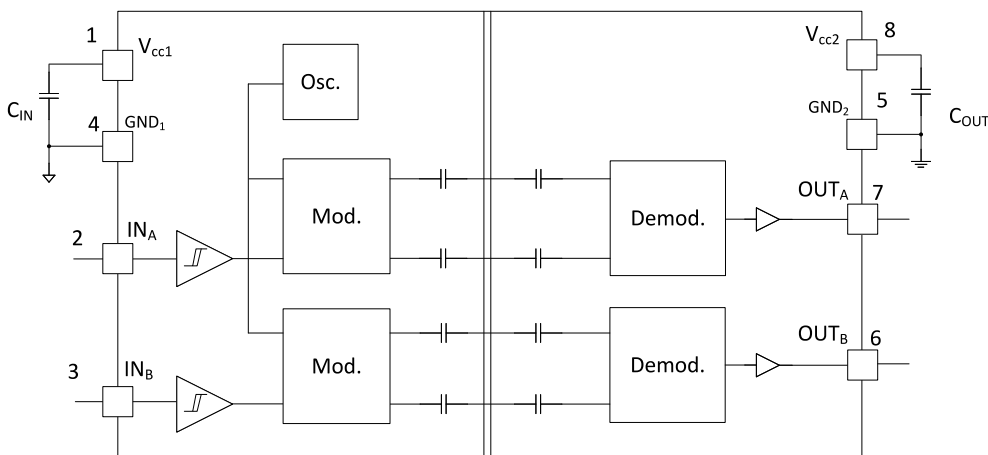


Figure 4: Block diagram of the CDIS 18012x15411x digital isolator.

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output of demodulator is passed through a buffer to the output; the buffer amplifies the signal to the required level.

Digital isolators are manufactured using standard CMOS technology and therefore use materials and processes that are well-known and tested. The capacitors of the transmitter side and the receiver side are deposited on a lead frame. The capacitors themselves, shown in gray in Figure 5, are formed between the two horizontal contacts, shown in red.

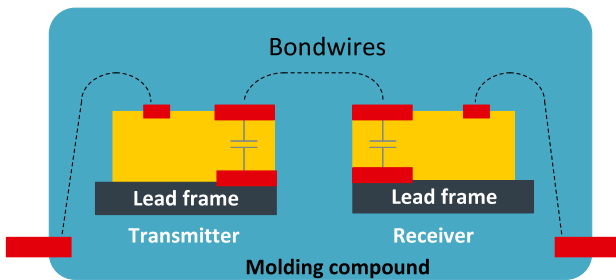


Figure 5: Basic structure of a capacitive digital isolator IC.

The dielectric material between the capacitor plates serves as a galvanic isolation barrier. The insulation thickness achieved by the process is in the range of a few tens of micrometers. In digital isolators, SiO<sub>2</sub> is used as the insulating material in the capacitor because its much higher dielectric strength of 500 MV/m means that it requires considerably less space for the isolating gap. Other common insulation materials, such as polyimide, have a dielectric strength of only 300 MV/m. The two capacitors are electrically connected with a bonding wire so that the two capacitors are connected in series, as shown in the block diagram in Figure 4. To protect the entire structure, the die and leadframe are molded using a standard IC assembly process.

### 4. CIRCUIT DESIGN OF THE TRANSMITTER

The input for DC signal measurement is a Wheatstone bridge with four resistors, see Figure 6. This is followed by an optional capacitor with 150 nF (C1) for damping AC voltage components.

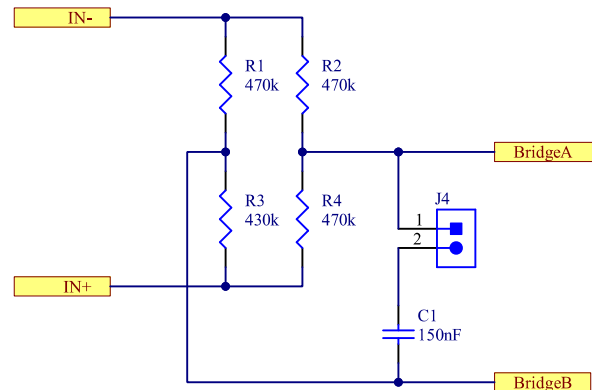


Figure 6: Wheatstone bridge as voltage divider at the input of the transmitter.

IC1A to IC1C in Figure 7 form an instrumentation amplifier whose amplification factor is set with P1. The input-side 1 M $\Omega$ -resistors (R9 & R13) are necessary for the stable operating point of the instrumentation amplifier and load the measuring signal with their resistance via the Wheatstone bridge. This results in an input impedance of approx. 450 k $\Omega$ .

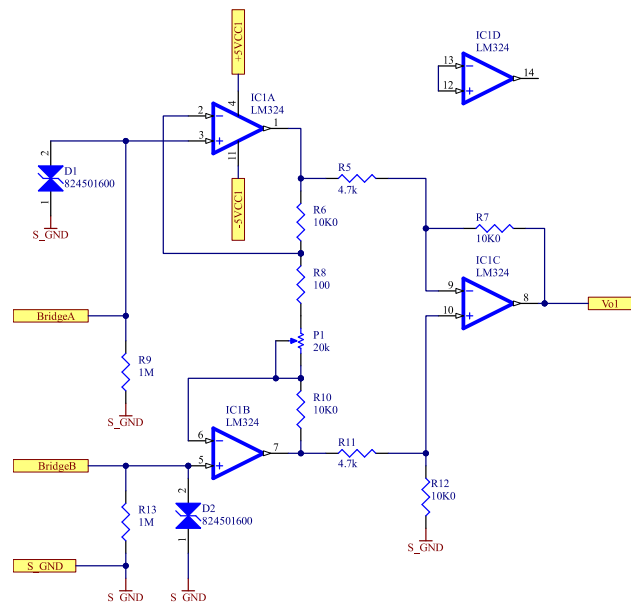


Figure 7: Discrete instrumentation amplifier for level amplification.

The bidirectional TVS diodes D1 and D2 clamp the input voltage at the instrumentation amplifier to a maximum of 10.3 V ( $V_{clamp}$  at  $I_{peak}$ ), but the current is limited by the voltage limitation via the Wheatstone bridge to such an extent that

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the clamping voltage is only slightly above the breakdown voltage of 7 V.

The maximum differential input voltage at one of the operational amplifiers is  $\pm 32$  V, thus ensuring reliable transient protection. The circuit is designed so that a maximum voltage of  $\pm 30$  V can be applied to the measurement input in order to control the instrumentation amplifier with a maximum of  $\pm 3.5$  V at its output. The level should be equalized to  $\pm 3.0$  V with P1.

As the signal can also have a negative polarity, it cannot be processed by the subsequent voltage-frequency converter.

The level converter (level shifter) with IC2A and IC2B in Figure 8 converts the signal to a level range of 0 V to +10 V, whereby:

- -30 V at the DC measurement input  $\rightarrow$  0 V at the level shifter output,
- 0 V at the DC measurement input  $\rightarrow$  +5 V at the level shifter output,
- +30 V at the DC measurement input  $\rightarrow$  +10 V at the level shifter output.

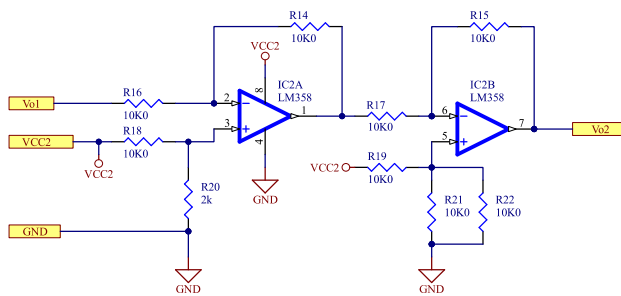


Figure 8: Level converter for level adjustment.

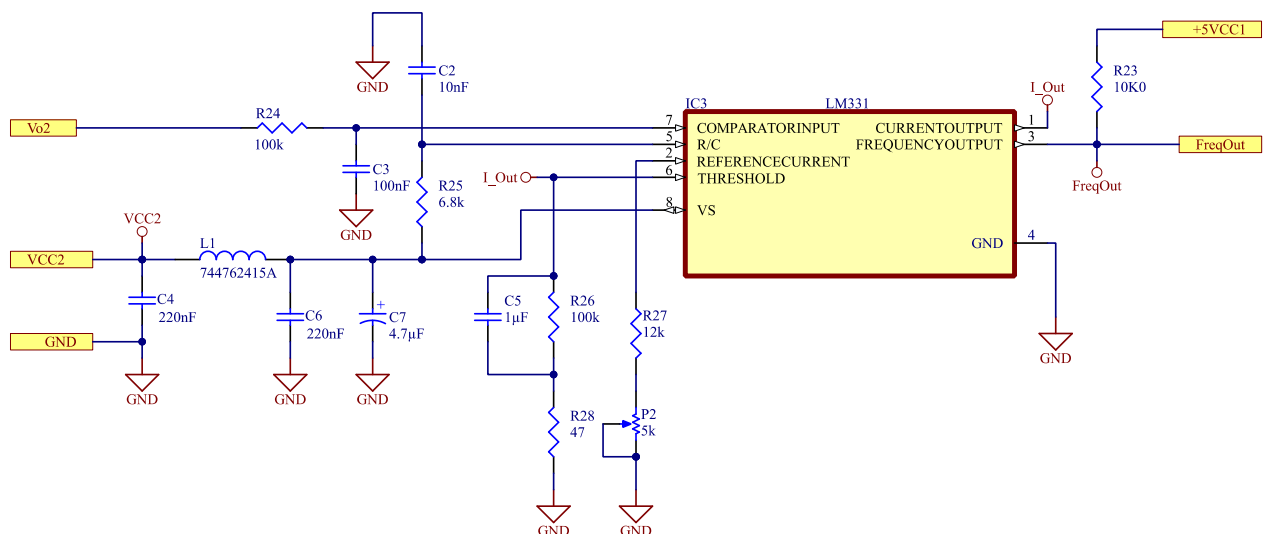


Figure 9: Voltage to frequency converter.

The voltage-frequency converter (IC3) follows the level shifter converts the DC voltage into a square-wave signal (Figure 9).

The wiring of the component results in the following relationship:

- -30 V at the DC measurement input  $\rightarrow$  8 kHz at the output of the IC3,
- 0 V at the DC measurement input  $\rightarrow$  5 kHz at the output of the IC3,
- +30 V at the DC measurement input  $\rightarrow$  2 kHz at the output of the IC3.

The frequency can be fine-tuned using P2 on the IC3. The output voltage of the voltage-frequency converter depends on the supply voltage of the pull-up resistor (R23) on pin 3 of the component and is set to +5 V here.

The square-wave signal with a level of 0/+5 V passes from the voltage/frequency converter to the digital isolator (IC4).

The digital isolator selected here is the [WPME-CDIS 18012015411L](#) module. Only one channel of the 2-channel module is required here, the second channel is connected to earth on the input side so that no unwanted interference is coupled in.

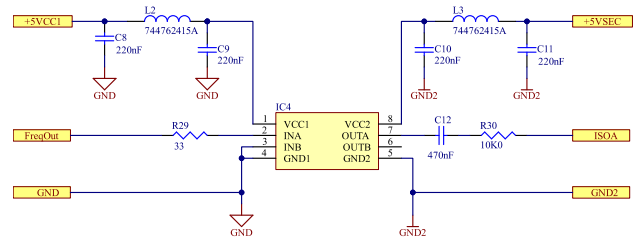


Figure 10: Digital isolator for galvanic isolation.

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The digital isolator is supplied on both the primary and secondary sides via an electrically isolated power module (Figure 10). This ensures that the galvanic decoupling generated by the digital isolator is also ensured via the power supply on the primary and secondary sides. This results in a higher level of decoupling, even if the +15 V supply is not galvanically isolated on the primary side. This decoupling also leads to a reduction in the modulation signals generated by a digital isolator and thus allows a higher signal-to-noise ratio for the operational amplifiers. The signal reaches the buffer amplifier IC5 from the secondary side of the digital isolator (Figure 11).

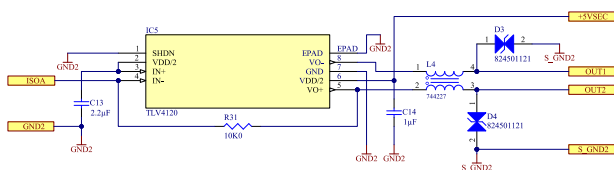


Figure 11: Output stage

The op-amp provides a low-impedance differential output for the twisted-pair line to the receiver. The transmission signal is decoupled against high-frequency common mode interference via the choke L4, while the output is protected against transient overvoltage with the bidirectional TVS diodes D3 and D4. The stray inductance of L4 and the parasitic capacitance of D3 and D4 form a low-pass filter against common mode noise. The signal level at the output is:

- Input voltage: +30 V → transmitter output voltage, at 120 Ω impedance: 8.3 V at 8.5 kHz,
- Input voltage: -30 V → transmitter output voltage, at 120 Ω impedance: 6.4 V at 2.2 KHz.

The transmitter is supplied with a voltage of +15 V, the current consumption is <85 mA. The +15 V input is HF-technically decoupled with a π-filter; depending on the application in the system, additional transient protection with a TVS diode may be necessary. A suitable component is the [WE-TVS 824045810](#).

On the primary side of the digital isolator, the +5 V voltage can alternatively be tapped directly from the 5 V DC-DC Power Module (U1) [FDSM](#) series. If galvanic isolation is also required on the primary side, the 15 V supply should also be galvanically isolated.

The π-filter around the L5 choke attenuates RF interference and already has an insertion loss of over 64 dB at 1 MHz. Figure 13 shows the calculation result from [REDEXPERT](#).

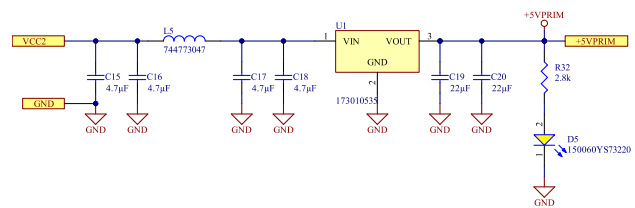


Figure 12: DC/DC primary side.

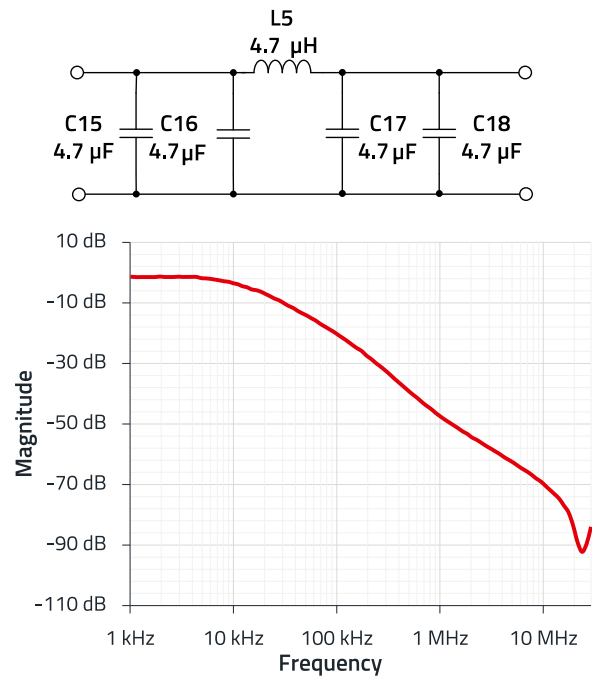


Figure 13: Insertion loss of the power supply filter simulated with [REDEXPERT](#).

Both the voltage-frequency converter IC3 and the digital isolator [WPME-CDIS](#) (IC4) contain oscillators and switching stages that can cause harmonic interference. For this reason, each of these components has an additional low-pass filter connected to its supply connections.

The SMD ferrite choke [WE-RFI 744762415A](#) (L2 & L3) was used here, which allows broadband decoupling up to the 1 GHz range thanks to its high resonance frequency (maximum impedance at approx. 70 MHz). However, this requires a HF-compliant layout and the use of suitable capacitors (here: 220 nF / 50 V, [WCAP-CSGP, 885012206125](#)). The three galvanically isolated DC-DC power modules (shown in Figure 1) do not change the input voltage of +5 V, but "merely" isolate it. The decisive factor here is a parasitic capacitance of typically <10 pF, so that decoupling is achieved over the widest possible frequency range and common-mode interference is avoided as far as possible.

### 5. CIRCUIT DESIGN OF THE RECEIVER

The differential transmission signal reaches the receiver circuit via the cable section, depending on the length and therefore also the frequency-dependent attenuation. Two TVS diodes are placed directly at the input of the interface to attenuate transient overvoltages. The following capacitors block any DC voltage offset that may occur. The common-mode choke attenuates HF interference and forms a low-pass filter with the parasitic capacitances of the TVS diodes. The two diodes connected in an anti-parallel clamp the differential input voltage to approx.  $\pm 0.7\text{ V}$ , the rest drops across the  $10\text{ k}\Omega$ -resistors.

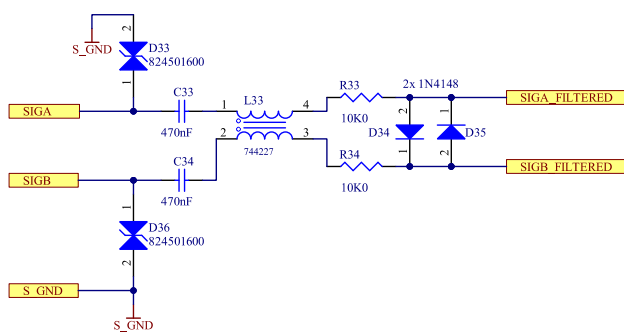


Figure 14: Input filter of the receiver.

The differential amplifier IC1a amplifies the signal to such an extent that it appears as a square-wave signal at the output. To make the circuit easier to understand, it was simulated in LT-Spice.

Figure 16 and Figure 15 show the simulation circuit diagram with the results. It can be clearly seen that the output voltage V(C) at the operational amplifier, i.e. the input voltage V(A,B) to the digital isolator, is almost independent of the input voltage.

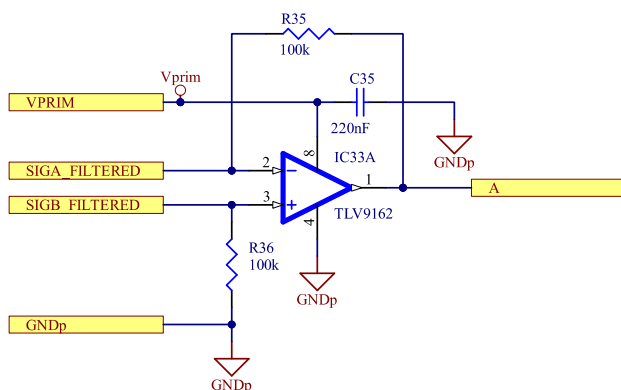


Figure 15: Signal amplifier of the receiver.

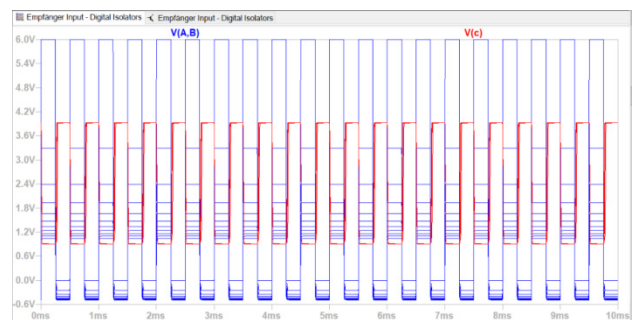
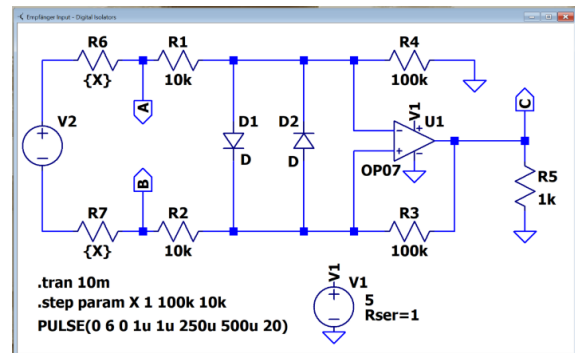


Figure 16: Simulation of the amplifier input stage with LT-Spice - circuit diagram.

The source voltage (V2) was assumed in the simulation to be  $6\text{ V}$  at a frequency of  $2\text{ kHz}$ , i.e. the input signal at a measurement voltage of  $\sim 3\text{ V}$ . The cable resistance was varied from  $2\ \Omega$  to  $200\text{ k}\Omega$ , the output voltage level remains constant at  $3\text{ V}$  ( $0.9\text{ V}_{\text{low}}$  to  $3.9\text{ V}_{\text{high}}$ ). In practice, it will not be possible to achieve the  $200\text{ k}\Omega$  cable resistance, as the impedance of the cable and electromagnetic environmental influences must be taken into account with increasing frequency, but distances of several hundred meters are feasible.

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The amplitude-stabilized signal is sent from the operational amplifier IC33A to the:

- Digital Isolator IC34.

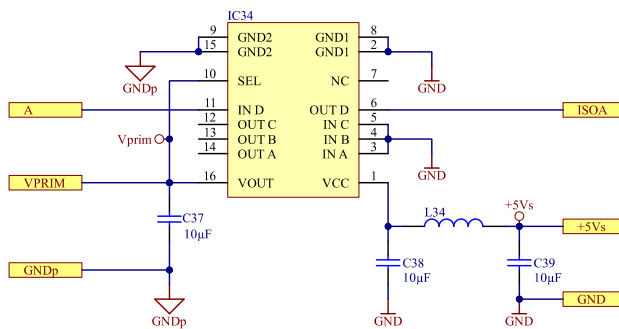


Figure 17: Digital isolator for galvanic isolation.

- "Link OK" amplifier or detector.

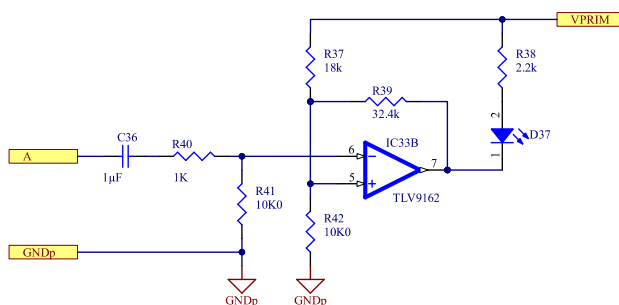


Figure 18: Link detector (LED on = link ok).

The "Link OK" amplifier IC33B (second OpAmp of the TLV9162) is connected as an inverting Schmitt trigger with offset and switches the blue LED to GND as soon as a signal is output at IC33A - this lights up the blue LED.

The digital isolator IC34 ([WPME-CDIP 18024115401L](#)) has an integrated galvanically isolated DC-DC converter, which is used to supply the input operational amplifier IC33A with

voltage. This means that the module not only galvanically isolates the signal, but also the supply voltage between the input amplifier and further signal processing. As with the transmitter, the input-side power supply at the digital isolator is RF-technically decoupled via an LC filter. The digital signal is routed via a low-pass filter (L36 & C43) at PIN6 of the IC35 in order to reduce signal noise (Figure 19).

The dimensioning of the components depends on the signal bandwidth to be transmitted. Figure 19 shows the effect of the filter; in terms of circuit technology, this allows a lower phase noise to be achieved when converting the AC voltage signal into a DC voltage signal. The noise reduction is 200 mV, the cut-off frequency of the filter is approx. 800 kHz, so that any influence on the useful signal in this application can be virtually ruled out.

The signal passes from the filter of the digital isolator to the frequency-to-voltage converter IC35.

The trim potentiometer is used to fine-tune the output voltage and should be adjusted so that the output voltage is between 2.0 V and 8.0 V, depending on the measurement voltage at the transmitter, as described in section 4. The frequency converter is also provided with a filter for the +15 V supply voltage so that its switching signals do not couple into the power supply.

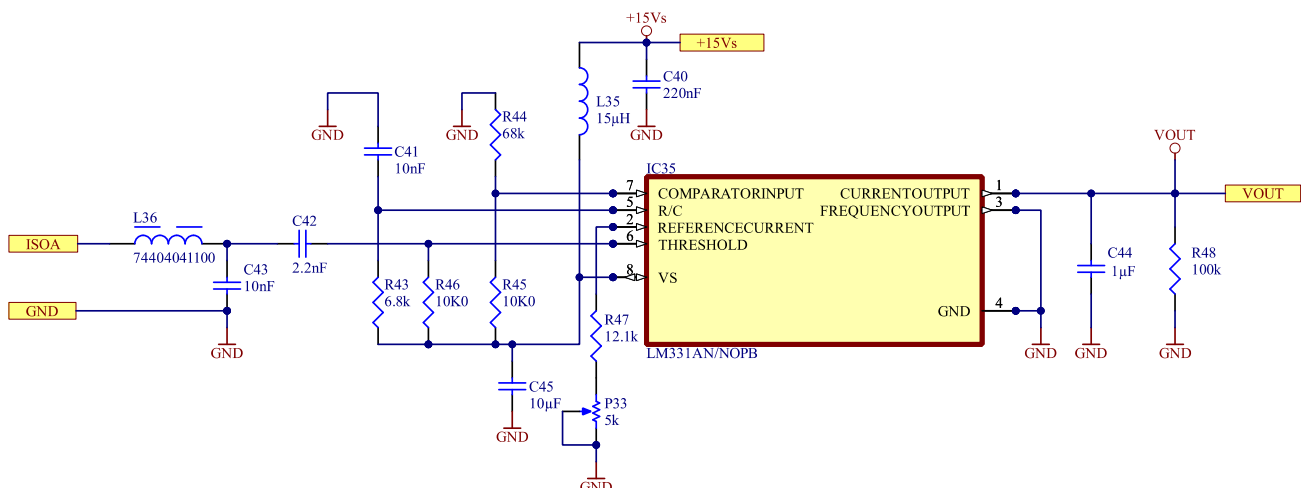


Figure 19: Frequency-voltage converter on the receiver.



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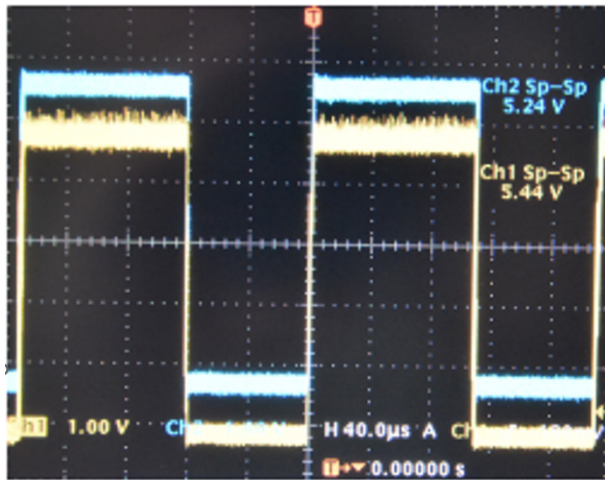


Figure 20: Filter for attenuating the signal noise for the F → U converter.

The 1 μF/100 kΩ - RC element at the output of the converter smooths the pulse-width modulated switching signals corresponding to the input frequency into a DC voltage. Depending on the combination of values, there are dependencies between response time, accuracy and residual ripple. For a more precise definition of the components, please refer to the manufacturer's datasheet.

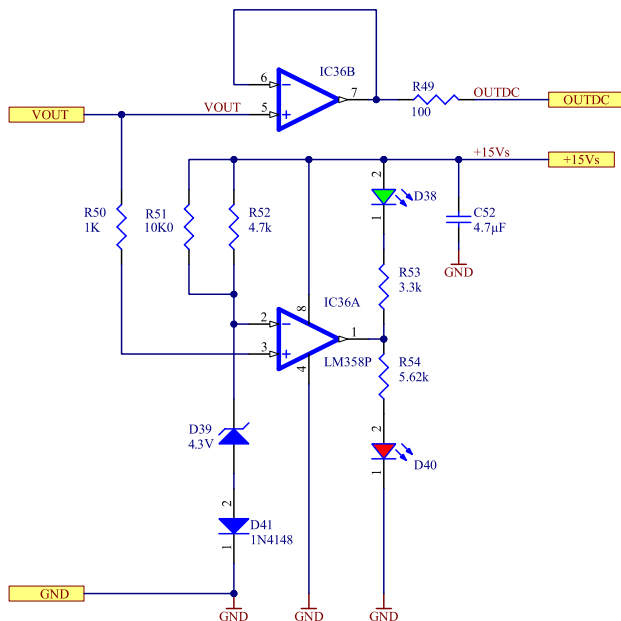
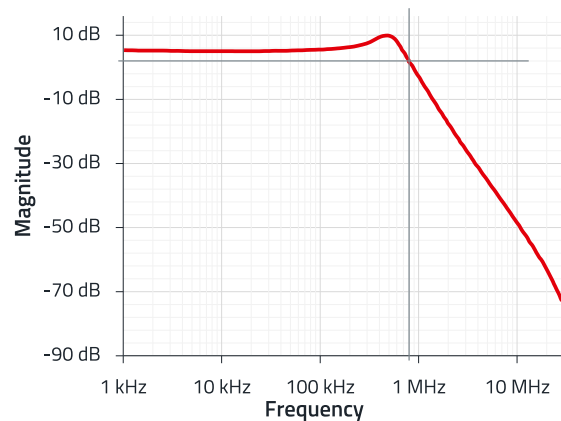


Figure 21: Polarity indicator for displaying the polarity of the measured voltage on the transmitter.



The polarity indicator (IC36A) at the output of the converter, shown in Figure 21, has the following function (Table 1):

Measuring voltage at transmitter	Output voltage at receiver	LED indicator
<0 ... -30 V	<5 ... 2 V	green
>0 ... +30 V	>5 ... 8 V	red

Table 1: LED indicator on the receiver depending on the input voltage on the transmitter.

This allows the polarity of the measured signal to be detected. Furthermore, the signal from the frequency-to-voltage converter is also fed to an output driver, at the output of which the level transmitted and converted equivalent to the measured voltage is available. The signal can be divided again for further processing on an AD converter, and the polarity display can be fed to a microcontroller for polarity detection. The voltage supply of the receiver is +15 V at <25 mA. As the digital isolator provides the galvanically isolated power supply to the operational amplifier on the input side, no further power supply is required. As with the transmitter, the supply voltage is routed via a π-filter and fed directly to the frequency-voltage converter on the one hand and reduced to +5 V via the DC-DC regulator [Magi<sup>3</sup>C-FDSM](#) on the other in order to supply the remaining electronics.

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### 6. TECHNICAL DATA

In summary, the application has the following performance data:

- Power supply transmitter: +15 V, <85 mA
- Power supply receiver: +15V, <25 mA

Figure 22 shows the relationship between the measured voltage and the voltage that is then displayed at the output.

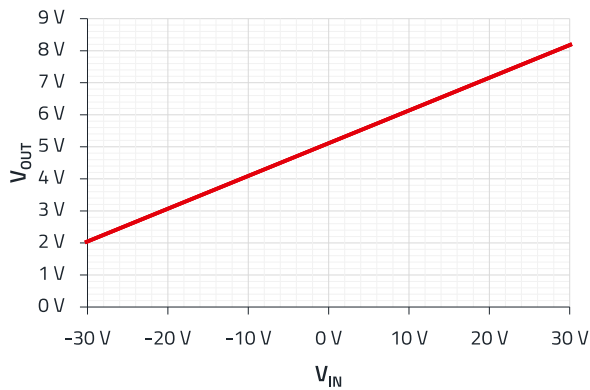


Figure 22: Diagram, input voltage over output voltage.

The transmission characteristic is almost linear over the entire input voltage range from -30 V to +30 V. The structure shown, consisting of a transmitter and a receiver board connected via a twisted pair cable, is therefore a suitable solution for galvanically isolated data acquisition and transmission.

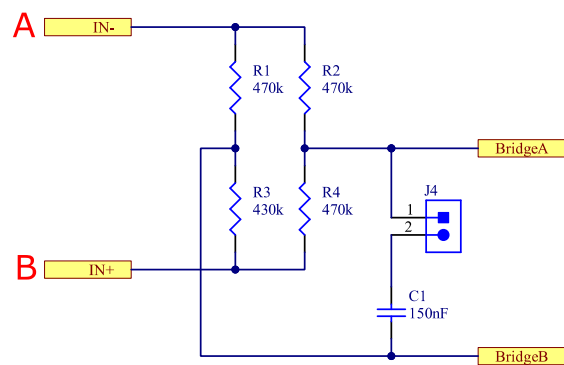
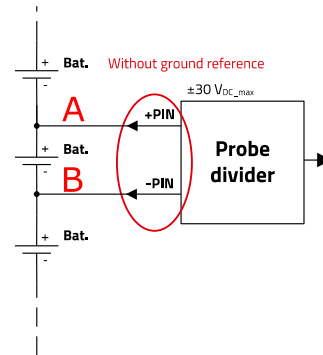


Figure 23: Measurement points A and B in Figure 1 and Figure 6 for Table 2

$U_{IN}$ [V]	$U_{OUT}$ [V]	LED	note	$U_{IN}$ [V]	$U_{OUT}$ [V]	LED	note
0	5.1	green	A: Minus, B: Plus	0	5.1	green	A: Plus, B: Minus
1	5.2	red		-1	5	green	
2	5.3	red		-2	4.9	green	
3	5.4	red		-3	4.8	green	
4	5.5	red		-4	4.7	green	
5	5.6	red		-5	4.6	green	
6	5.7	red		-6	4.5	green	
7	5.8	red		-7	4.4	green	
8	5.9	red		-8	4.3	green	
10	6.1	red		-9	4.2	green	
12	6.3	red		-10	4.1	green	
14	6.5	red		-12	3.9	green	
17	6.8	red		-14	3.7	green	
20	7.1	red		-17	3.4	green	
23	7.4	red		-20	3.1	green	
25	7.6	red		-23	2.8	green	
28	7.9	red		-25	2.6	green	
30	8.1	red		-28	2.3	green	
				-30	2.1	green	

Table 2: Output voltage as a function of the input voltage.(see Figure 23 for reference)

### A APPENDIX

#### A.1 References

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# APPLICATION NOTE

## ANS020 | Digital isolators

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# APPLICATION NOTE

ANS020 | Digital isolators

## REVISION HISTORY

Document Version	Release Date	Changes
ANS020a	2024/11/05	Initial release of the application note

**Note:** The current version of the document and the release date are indicated in the footer of each page of this document.