

3.5V - 60V Input / 0.3A Output / 0.85V - 6V Output

DESCRIPTION

The VDMM 171936001 Magl³C Power Module provides a fully integrated DC/DC converter including the switching regulator with integrated MOSFETs, compensation and shielded inductor in one package.

The 171936001 offers high efficiency and delivers up to 0.3A of output current. It operates with an input voltage from 3.5V to 60V. This power module is tailor suited for space constrained applications that need a high power density.

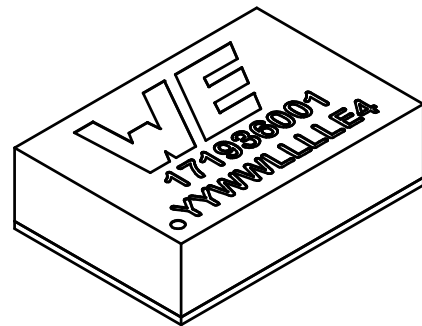
The selectable forced PWM or PFM/PWM mode allows for optimizing light load efficiency and output voltage ripple.

The 171936001 is available in an LGA-12 package (8 x 5.5 x 2.3mm).

This module has integrated protection circuitry that guards against thermal overstress with thermal shutdown. It protects against electrical damage using overvoltage, overcurrent, short-circuit and undervoltage protections.

TYPICAL APPLICATIONS

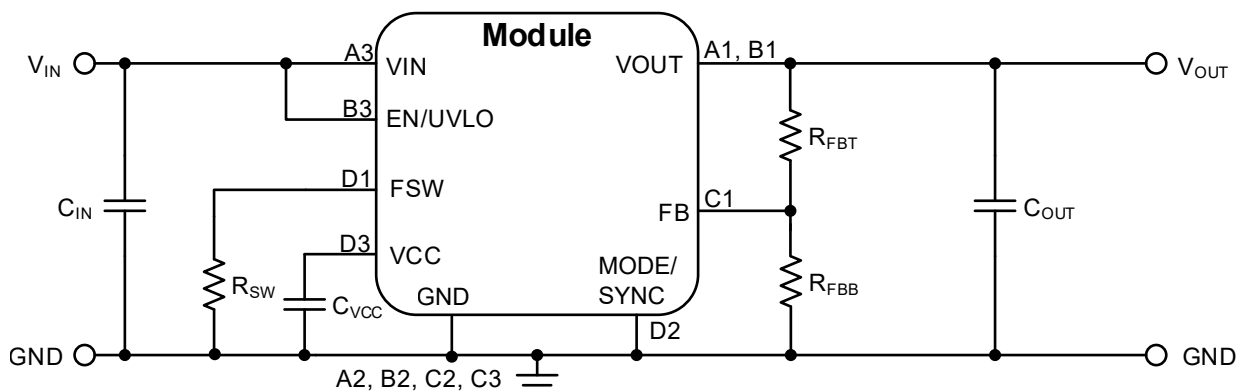
- Point-of-Load DC-DC applications
- General purpose applications
- Industrial, test & measurement, medical applications
- System power supplies
- DSPs, FPGAs, MCUs and MPUs supply
- I/O interface power supply



FEATURES

- Peak efficiency up to 86%
- Input voltage range: 3.5V to 60V
- Typical quiescent current: 3µA
- Output voltage range: 0.85V to 6V
- Current capability up to 0.3A
- Current mode control
- Synchronous operation
- Adjustable switching frequency: 0.2 to 1MHz
- Sync function for custom switching frequencies
- PFM/PWM mode
- Embedded soft-start
- Selectable spread spectrum
- Undervoltage lockout
- Cycle-by-cycle current limit
- Short-circuit protection
- Thermal shutdown
- Ambient temperature up to 105°C
- Junction temp. range: -40°C to 125°C
- RoHS und REACH compliant
- Complies with EN55032 / CISPR32 class B conducted and radiated emissions standard

TYPICAL CIRCUIT DIAGRAM

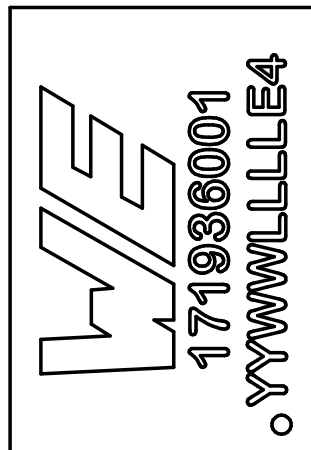


CONTENTS

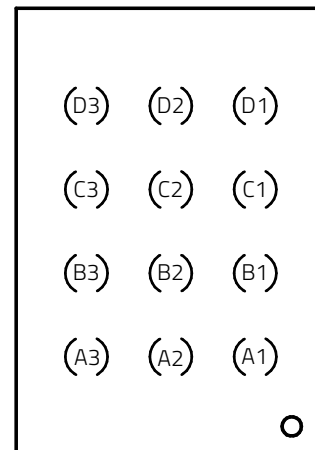
1	PINOUT	4
2	ORDERING INFORMATION	5
3	SALES INFORMATION	5
4	ABSOLUTE MAXIMUM RATINGS	6
5	OPERATING CONDITIONS	6
6	THERMAL SPECIFICATIONS	6
7	ELECTRICAL SPECIFICATIONS	7
8	RoHS, REACH	8
9	PACKAGE SPECIFICATIONS	8
10	NOTES	8
11	TYPICAL PERFORMANCE CURVES	9
11.1	Radiated and Conducted Emissions (With EMI Input Filter)	9
11.1.1	Radiated Emissions EN55032 (CISPR-32) Class B Complaint Test Setup	9
11.1.2	Conducted Emissions EN55032 (CISPR-32) Class B Complaint Test Setup	9
11.1.3	Radiated Emissions (Fixed Frequency)	10
11.1.4	Conducted Emissions (Fixed Frequency)	10
11.2	DC Performance Curves	11
11.2.1	Efficiency 24Vin FPWM	11
11.2.2	Efficiency 48Vin FPWM	11
11.2.3	Efficiency 24Vin PFM	12
11.2.4	Efficiency 48Vin PFM	12
11.2.5	Thermal Derating 48Vin	13
11.2.6	Load Regulation 3.3Vout FPWM	14
11.2.7	Load Regulation 5Vout FPWM	14
11.2.8	Load Regulation 3.3Vout PFM	15
11.2.9	Load Regulation 5Vout PFM	15
11.2.10	Line Regulation 3.3Vout FPWM	16
11.2.11	Line Regulation 5Vout FPWM	16
11.2.12	Line Regulation 3.3Vout PFM	17
11.2.13	Line Regulation 5Vout PFM	17
12	BLOCK DIAGRAM	18
13	CIRCUIT DESCRIPTION	18
14	DESIGN FLOW	19
14.1	STEP 1 Setting the Output Voltage (V_{OUT})	20
14.2	STEP 2 Select the Input Capacitor (C_{IN})	20
14.3	STEP 3 Select the Output Capacitor (C_{OUT})	20
14.4	STEP 4 Select the V_{CC} Capacitor (C_{VCC})	22
14.5	STEP 5 Select the Switching Frequency (f_{SW})	22
15	MODES OF OPERATION	23
16	OUTPUT VOLTAGE RIPPLE	24
16.1	FPWM Operation	24
16.2	PFM Operation	24

17 PROTECTION FEATURES	25
17.1 Overcurrent Protection (OCP) and Short Circuit Protection (SCP)	25
17.2 Output Overvoltage Protection (OVP)	26
17.3 Over Temperature Protection (OTP)	26
17.4 Soft-Start	27
17.5 Enable and Integrated/Adjustable UVLO	28
17.6 External Clock Synchronization (Sync)	29
18 DESIGN EXAMPLE	30
18.1 Layout	30
18.2 Schematic	31
18.3 Bill of Materials	31
19 HANDLING RECOMMENDATIONS	32
20 SOLDER PROFILE	32
21 PHYSICAL DIMENSIONS	33
21.1 Component	33
21.2 Example Landpattern	34
21.3 Packaging	35
22 DOCUMENT HISTORY	37
23 LIST OF FIGURES	38
24 LIST OF TABLES	39
25 CAUTIONS AND WARNINGS	40
26 IMPORTANT NOTES	41

1 PINOUT



Top View



Top Through View

Figure 1: Pinout.

Table 1: Pin description.

SYMBOL	NUMBER	TYPE	DESCRIPTION
FSW	D1	Input	Switching frequency selection pin. Connect an external resistor to select the switching frequency. Connecting the resistor to VCC enables spread spectrum for EMI improvement. Connecting the resistor to GND disables spread spectrum and keeps the frequency fixed.
FB	C1	Input	Feedback pin to the internal error amplifier. This pin must be connected to the external resistor divider to adjust the output voltage.
VCC	D3	Power	VCC pin. This pin is attached to the output of the internal LDO. Connect a ceramic capacitor of 470nF to VCC and GND.
VIN	A3	Power	Input voltage pins. Place the input capacitor as close as possible to VIN and GND. It is recommended to use 2x 1 μ F / 100V capacitors. It is recommended to use smaller packages such as 1210.
VOUT	A1, B1	Power	Output voltage pins. Place output capacitors as close as possible to VOUT and GND. For thermal performance use copper plane(s) at these pins.
MODE/SYNC	D2	Input	Mode selection pin. Connect this pin to GND to enable auto PFM/PWM mode or connect it to VCC to enable forced PWM mode. This pin can be used as sync pin to run the power module with external clock.
EN/UVLO	B3	Input	Enable pin. Pull this pin down to GND to disable the module, leave this pin floating or apply a voltage higher than 1.2V to enable the module.
GND	C2, C3	Power	Ground pins. For proper operation of the module, connect GND pad of the input capacitor with short, direct and wide plane to these pins. Place the GND input capacitor pad as close as possible to these pins.
GND	A2, B2	Power	Ground pins. Internally connected to C2 and C3. For heat dissipation of the module, it is recommended to connect suitable ground plane with proper number of vias to improve thermal performance.

2 ORDERING INFORMATION

Table 2: Ordering information.

ORDER CODE	SPECIFICATIONS	PACKAGE	PACKAGING UNIT
171936001	0.3A / 0.85V-6V Vout	LGA-12	13" Reel (1000 pieces)
178936001	0.3A / 0.85V-6V Vout	Eval Board	1 piece

3 SALES INFORMATION

Table 3: Sales information.

SALES CONTACT
Würth Elektronik eiSos GmbH & Co. KG EMC and Inductive Solutions Max-Eyth-Str. 1 74638 Waldenburg Germany Tel. +49 (0) 7942 945 0 www.we-online.com/powermodules Technical support: powermodules@we-online.com

4 ABSOLUTE MAXIMUM RATINGS

Caution:

Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

Table 4: Absolute maximum ratings.

SYMBOL	PARAMETER	LIMIT		UNIT
		MIN ⁽¹⁾	MAX ⁽¹⁾	
V _{IN}	Input pin voltage	-0.3	63	V
V _{OUT}	Output pin voltage	-0.3	V _{IN} +0.3	V
FB	Feedback pin voltage	-0.3	5.5	V
EN	Enable pin voltage	-0.3	V _{IN} +0.3	V
VCC	VCC pin voltage	-0.3	V _{IN} +0.3, max. 3.6	V
FSW	Switching frequency selection pin voltage	-0.3	V _{CC} +0.3	V
T _{storage}	Assembled, non-operating storage temperature	-40	125	°C
V _{ESD}	ESD voltage (HBM), all pins (C=100pF R=1.5kΩ) ⁽⁴⁾	-2	2	kV

5 OPERATING CONDITIONS

Operating conditions are conditions under which the device is intended to be functional. All values are referenced to GND. MIN and MAX limits are valid for the recommended ambient temperature range of -40 °C to 105 °C. Typical values represents statistically the utmost probable values at the following conditions: V_{IN} = 48V, V_{OUT} = 5V, C_{IN} = 2x 1μF ceramic, C_{OUT} = 4.7μF ceramic, T_A = 25 °C unless otherwise noted.

Table 5: Operating conditions.

SYMBOL	PARAMETER	MIN ⁽¹⁾	TYP ⁽³⁾	MAX ⁽¹⁾	UNIT	
V _{IN}	Input voltage	3.5	-	60	V	
V _{OUT}	Output voltage	0.85	-	6	V	
T _a	Ambient temperature range	-40	-	105 ⁽²⁾	°C	
T _j	Junction temperature range	-40	-	125	°C	
I _{OUT}	Output current ⁽⁵⁾	-	-	0.3	A	
C _{OUT MAX}	Maximum output capacitance	V _{OUT} = 5V	-	-	10	μF
		V _{OUT} = 3.3V	-	-	15	μF

6 THERMAL SPECIFICATIONS

Typical values represents statistically the utmost probable values at the following conditions: V_{IN} = 48V, V_{OUT} = 5V, C_{IN} = 2x 1μF ceramic, C_{OUT} = 4.7μF ceramic, T_A = 25 °C unless otherwise noted.

Table 6: Thermal specifications.

SYMBOL	PARAMETER	TYP ⁽³⁾	UNIT
Θ _{JA}	Junction-to-ambient thermal resistance ⁽²⁾	40	K/W
Θ _{JC}	Junction-to-case (top) thermal resistance ⁽²⁾	23	K/W
T _{SD}	Thermal shutdown, rising	165	°C
	Thermal shutdown, hysteresis	30	°C

7 ELECTRICAL SPECIFICATIONS


MIN and MAX limits are valid for the recommended ambient temperature range of -40°C to 105°C . Typical values represents statistically the utmost probable values at the following conditions: $V_{\text{IN}} = 48\text{V}$, $V_{\text{OUT}} = 5\text{V}$, $C_{\text{IN}} = 2 \times 1\mu\text{F}$ ceramic, $C_{\text{OUT}} = 4.7\mu\text{F}$ ceramic, $T_{\text{A}} = 25^{\circ}\text{C}$ unless otherwise noted.

Table 7: Electrical specifications part 1.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽³⁾	MAX ⁽¹⁾	UNIT
I_{OC}	Overcurrent limit	Slope contribution at 20%	—	0.47	—	A
I_{RC}	Reverse current limit	When OVP is detected	—	-0.15	—	A
$T_{\text{ON_MIN}}$	Minimum on-time		—	60	—	ns
Enable						
V_{EN}	Enable threshold	Rising	1.1	1.2	1.3	V
		Hysteresis	—	0.2	—	V
Ext. Clock Sync						
$V_{\text{CLK_H}}$	Ext. clock signal high voltage		2	—	5	V
$V_{\text{CLK_L}}$	Ext. clock signal low voltage		0	—	1.3	V
$V_{\text{CLK_SEL}}$	Ext. clock signal selection level	High level	2	—	5	V
		Low level	0	—	1.3	V
f_{CLK}	Ext. clock frequency		200	—	1000	kHz
VCC Regulator						
V_{CC}	LDO output voltage		2.9	3.3	3.6	V
Input Quiescent, No Load and Shutdown Current						
I_{SD}	Shutdown current from V_{IN}	$V_{\text{EN}} = \text{GND}$	—	2.3	—	μA
I_{Q}	Quiescent current from V_{IN}	$V_{\text{OUT}} \leq 3.2\text{V}$, no switching, FPWM	—	1300	—	μA
		$V_{\text{OUT}} > 3.2\text{V}$, no switching, FPWM	—	170	—	μA
		$V_{\text{OUT}} \leq 3.2\text{V}$, no switching, PFM	—	35	—	μA
		$V_{\text{OUT}} > 3.2\text{V}$, no switching, PFM	—	3	—	μA
$I_{\text{IN-NL}}$	No load input current	$V_{\text{IN}} = 48\text{V}$, $V_{\text{OUT}} = 5\text{V}$, FPWM	—	1.7	—	mA
		$V_{\text{IN}} = 48\text{V}$, $V_{\text{OUT}} = 5\text{V}$, PFM	—	8	—	μA
Output Voltage						
V_{FB}	Voltage reference	$T_{\text{J}} = -40^{\circ}\text{C} \leq T_{\text{J}} \leq 125^{\circ}\text{C}$	0.84	0.85	0.86	V
V_{OVP}	Output overvoltage protection		—	120	—	%
$V_{\text{OVP_HYS}}$	Output overvoltage hysteresis		—	2	—	%
Soft-Start						
t_{SS}	Soft-start time	Rising edge to V_{OUT} (nom.)	1.3	2	2.7	ms
Switching Frequency						
f_{SW}	Switching frequency		200	—	1000	kHz
Efficiency						
η	Efficiency	$V_{\text{IN}} = 24\text{V}$, $V_{\text{OUT}} = 5\text{V}$, $I_{\text{OUT}} = 0.3\text{A}$	—	79	—	%
		$V_{\text{IN}} = 48\text{V}$, $V_{\text{OUT}} = 5\text{V}$, $I_{\text{OUT}} = 0.3\text{A}$	—	76	—	%

8 RoHS, REACH

Table 8: RoHS, REACH.

RoHS directive		Directive 2011/65/EU of the European Parliament and the Council of June 8th, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.
REACH directive		Directive 1907/2006/EU of the European Parliament and the Council of June 1st, 2007 regarding the Registration, Evaluation, Authorization and Restriction of Chemicals (REACH).

9 PACKAGE SPECIFICATIONS

Table 9: Package specifications.

ITEM	PARAMETER	TYP ⁽³⁾	UNIT
Lead Finish	ENEPIG	-	-
Weight	-	0.27	g

10 NOTES

- (1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.
- (2) Measured without heatsink. Natural convection (0 - 20LFM / 0- 0.1m/s) on a 80 x 80mm two layer board, with 35µm (1 ounce) copper.
- (3) Typical numbers are valid at 25°C ambient temperature and represent statistically the utmost probable values assuming a Gaussian distribution.
- (4) The human body model is a 100pF capacitor discharged through a 1.5Ωk resistor into each pin. Test method is per JESD-22-114.
- (5) Dependent on ambient temperature; see [THERMAL DERATING](#).

11 TYPICAL PERFORMANCE CURVES

If not otherwise specified, the following conditions apply: $T_A = 25^\circ\text{C}$.

11.1 Radiated and Conducted Emissions (With EMI Input Filter)

The 171936001 power module was tested in several EMC configurations to give more realistic information about implementation in the applications. The test setup is based on CISPR16 with the limit values of CISPR32. All measurements were performed on the layout shown in [DESIGN EXAMPLE](#) and using the components listed there.

11.1.1 Radiated Emissions EN55032 (CISPR-32) Class B Complaint Test Setup

- Measured in a Fully Anechoic Room (FAR) at 3m antenna distance.
- Input wire length: 160cm (80cm horizontal + 80cm vertical)
- Output wire length: 100cm

11.1.2 Conducted Emissions EN55032 (CISPR-32) Class B Complaint Test Setup

- Measurement input wire length: 80cm
- Output wire length: 100cm

11.1.3 Radiated Emissions

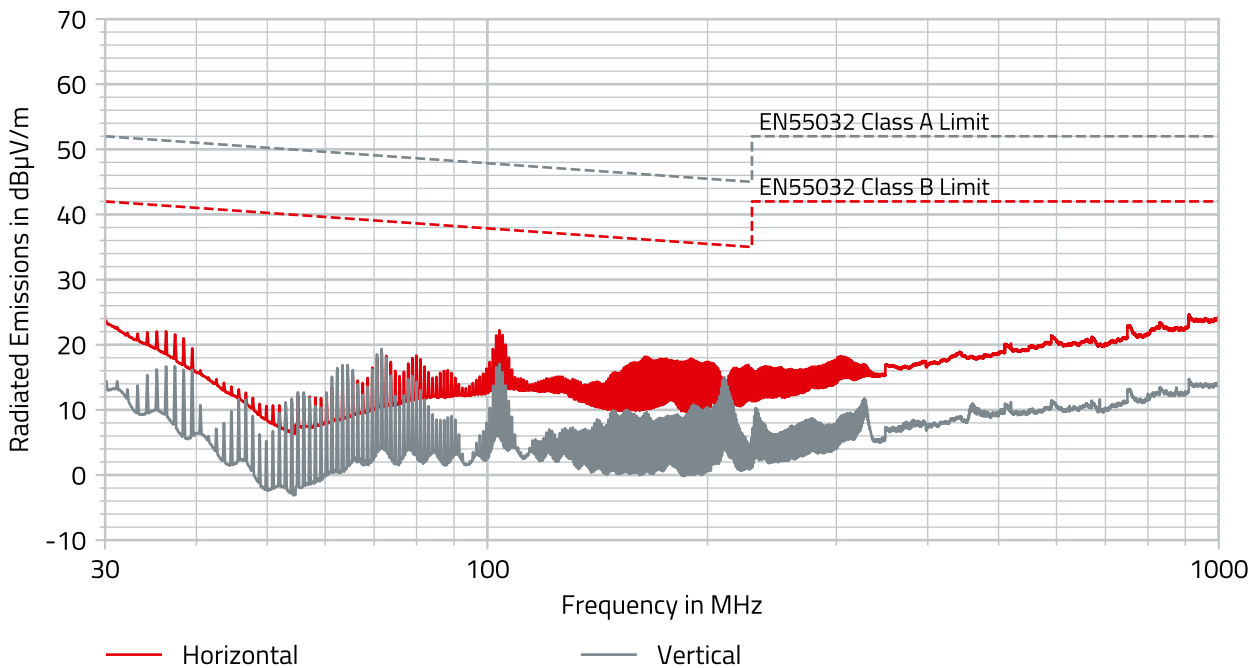


Figure 2: Radiated emissions 171936001 (3m antenna distance) $V_{IN} = 48V$, $V_{OUT} = 5V$, $I_{OUT} = 0.3A$ with input filter. R_{SW} is connected to GND.

11.1.4 Conducted Emissions

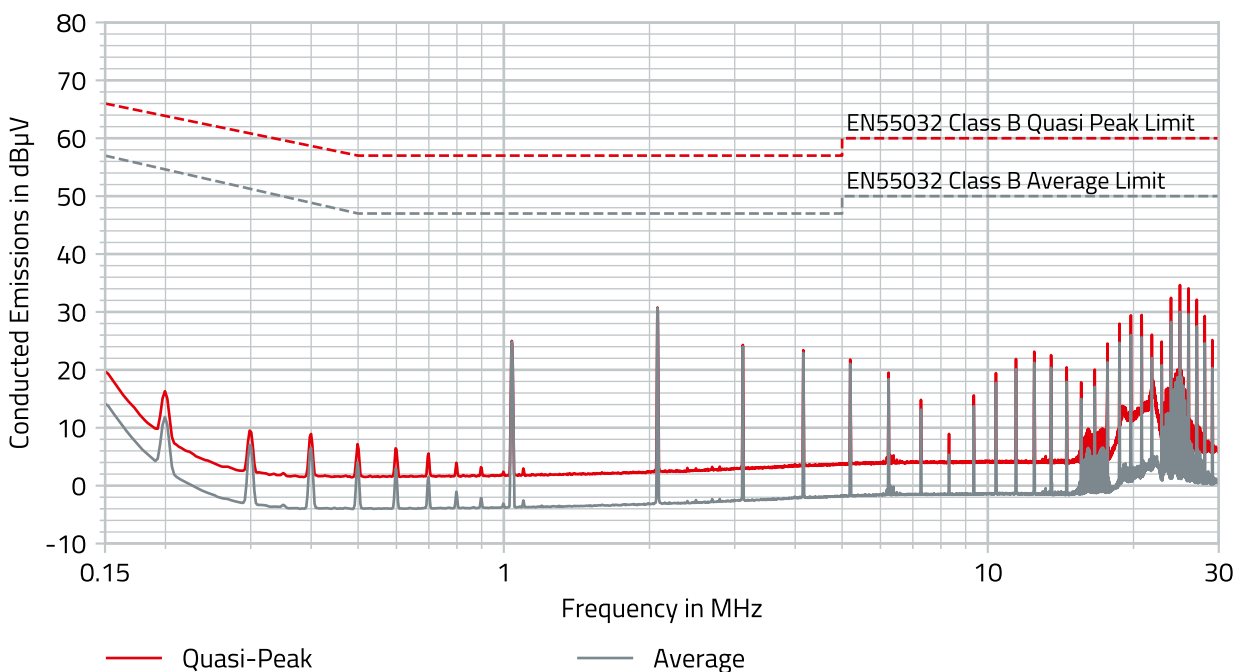


Figure 3: Conducted emissions 171936001 $V_{IN} = 48V$, $V_{OUT} = 5V$, $I_{OUT} = 0.3A$ with input filter. R_{SW} is connected to GND.

11.2 DC Performance Curves

11.2.1 Efficiency 24V_{IN} FPWM

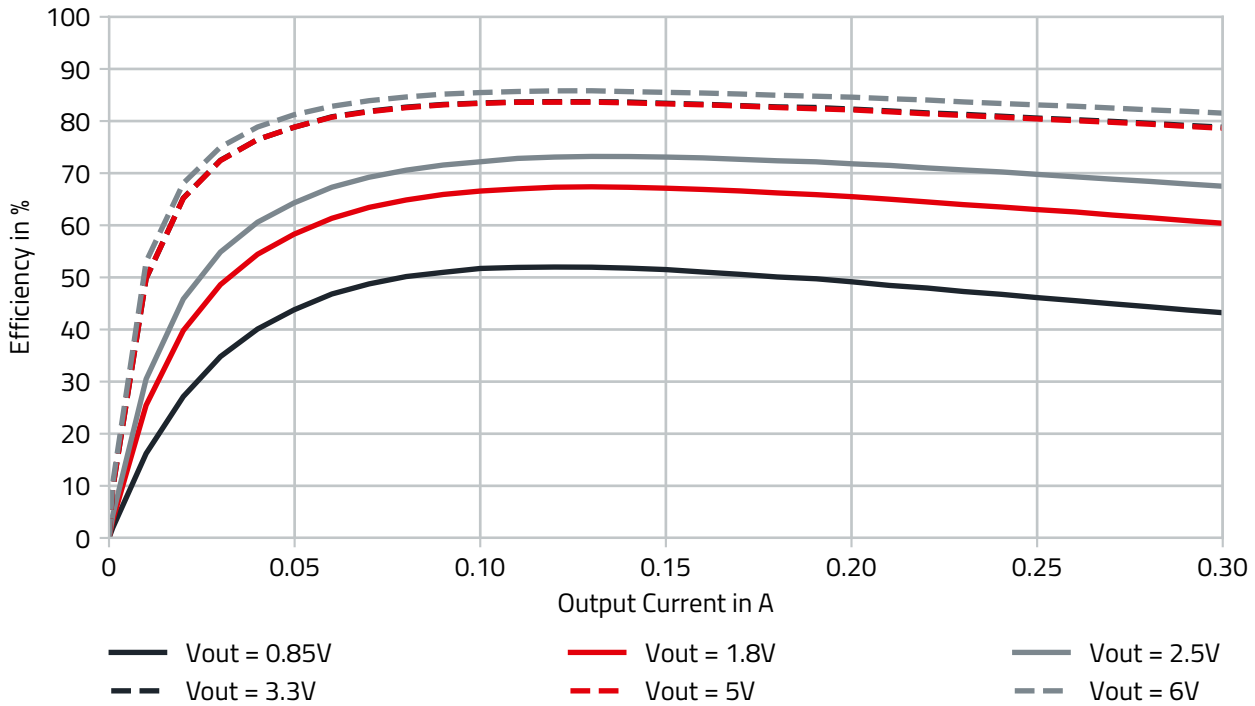


Figure 4: 171936001 efficiency V_{IN} = 24V, FPWM mode.

11.2.2 Efficiency 48V_{IN} FPWM

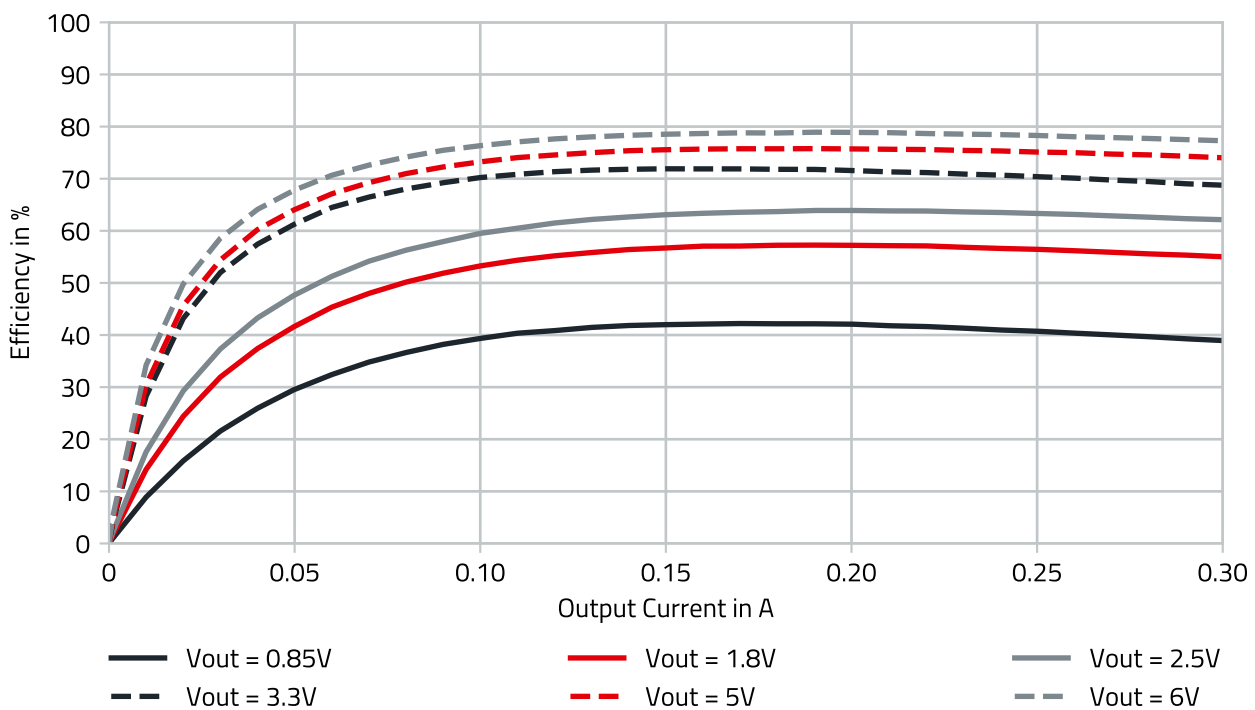


Figure 5: 171936001 efficiency V_{IN} = 48V, FPWM mode.

11.2.3 Efficiency 24V_{IN} PFM

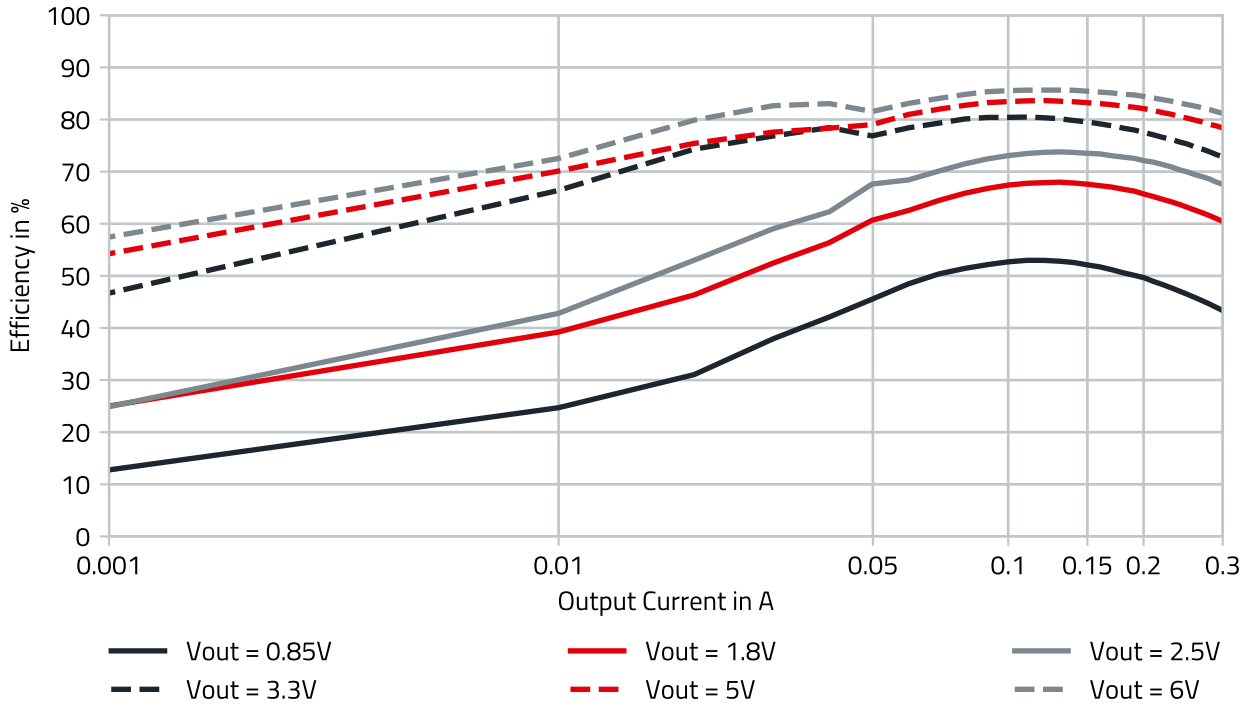


Figure 6: 171936001 efficiency V_{IN} = 24V, PFM mode.

11.2.4 Efficiency 48V_{IN} PFM

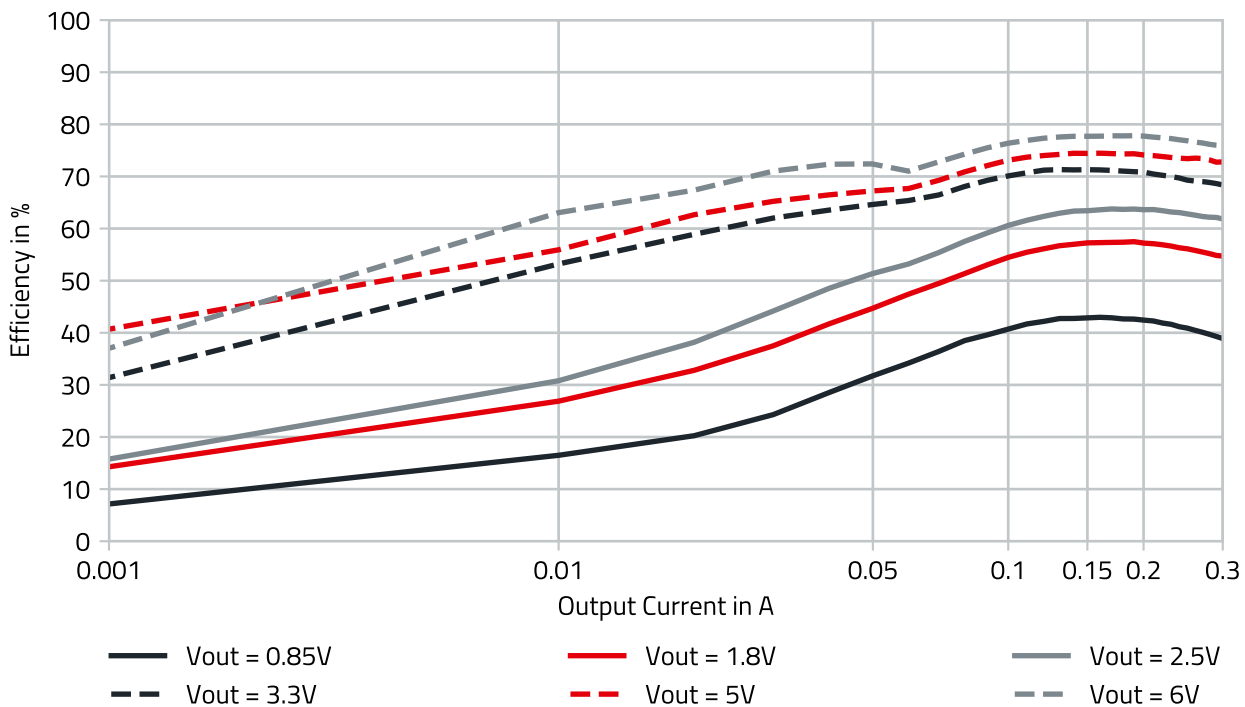
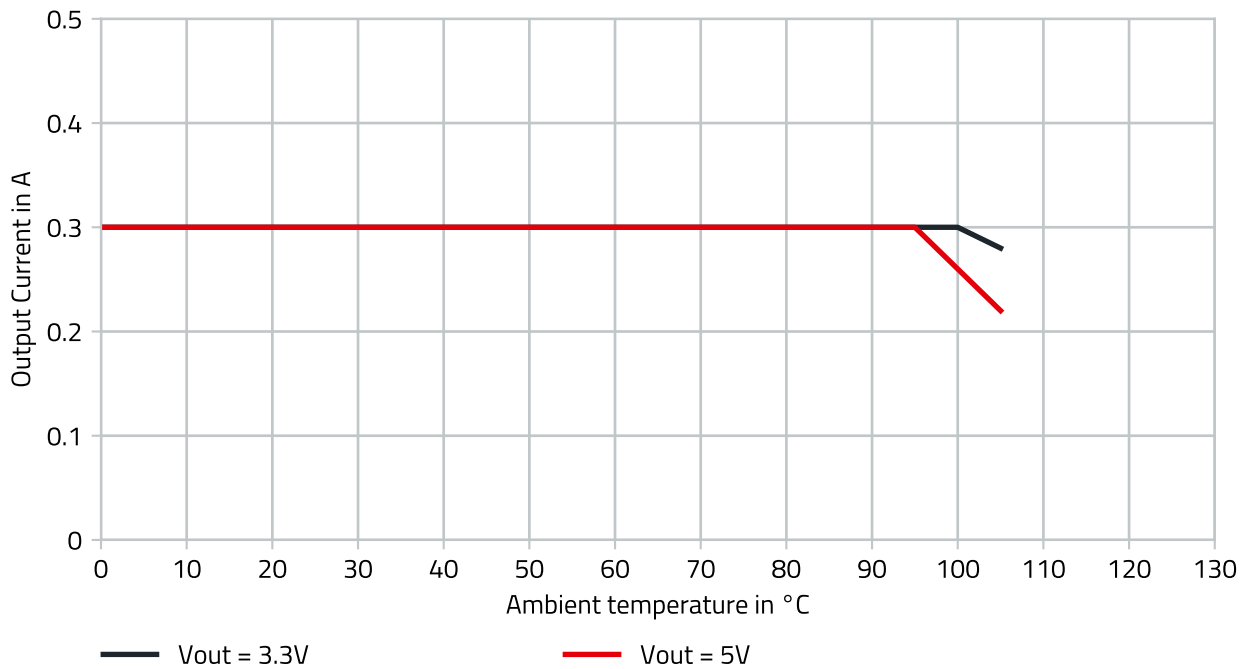


Figure 7: 171936001 efficiency V_{IN} = 48V, PFM mode.

11.2.5 Thermal Derating 48V_{IN}Figure 8: 171936001 output current thermal derating V_{IN} = 48V.

Note: Thermal derating graphs were measured on the 178936001 Evaluation Board (80 x 80mm two layer board, with 35µm (1 ounce) copper). Please see T_A limits in [OPERATING CONDITIONS](#).

11.2.6 Load Regulation 3.3V_{OUT} FPWM

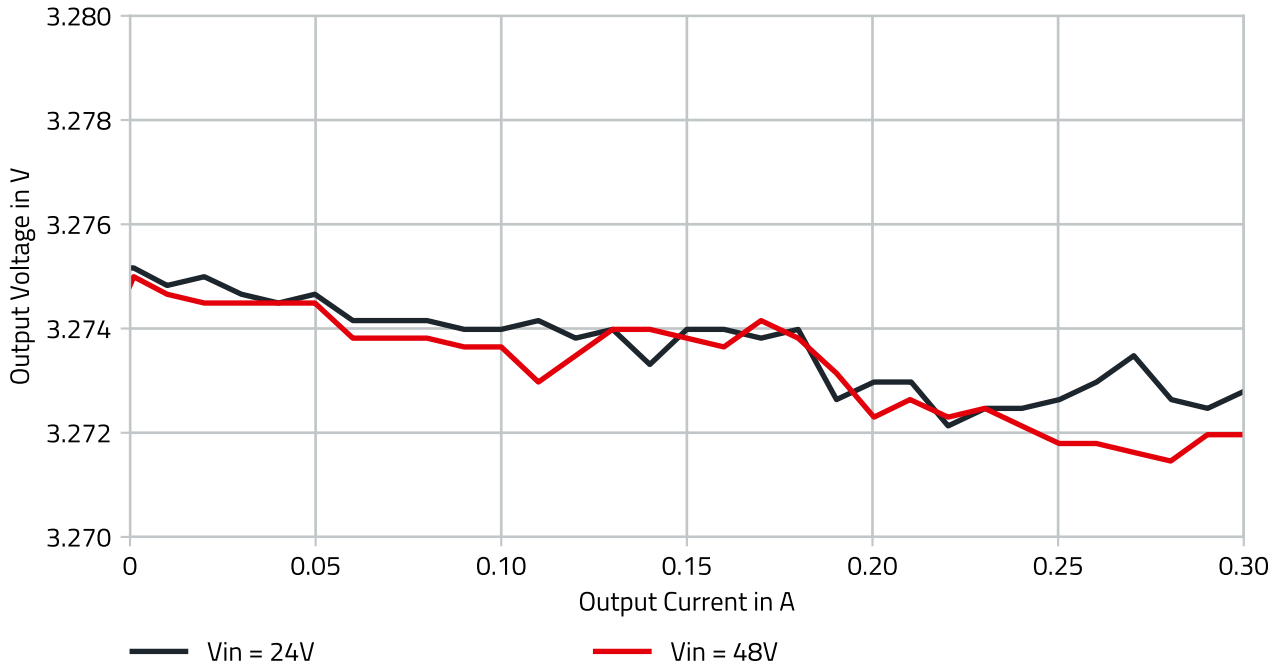


Figure 9: 171936001 load regulation $V_{OUT} = 3.3V$, FPWM mode.

11.2.7 Load Regulation 5V_{OUT} FPWM

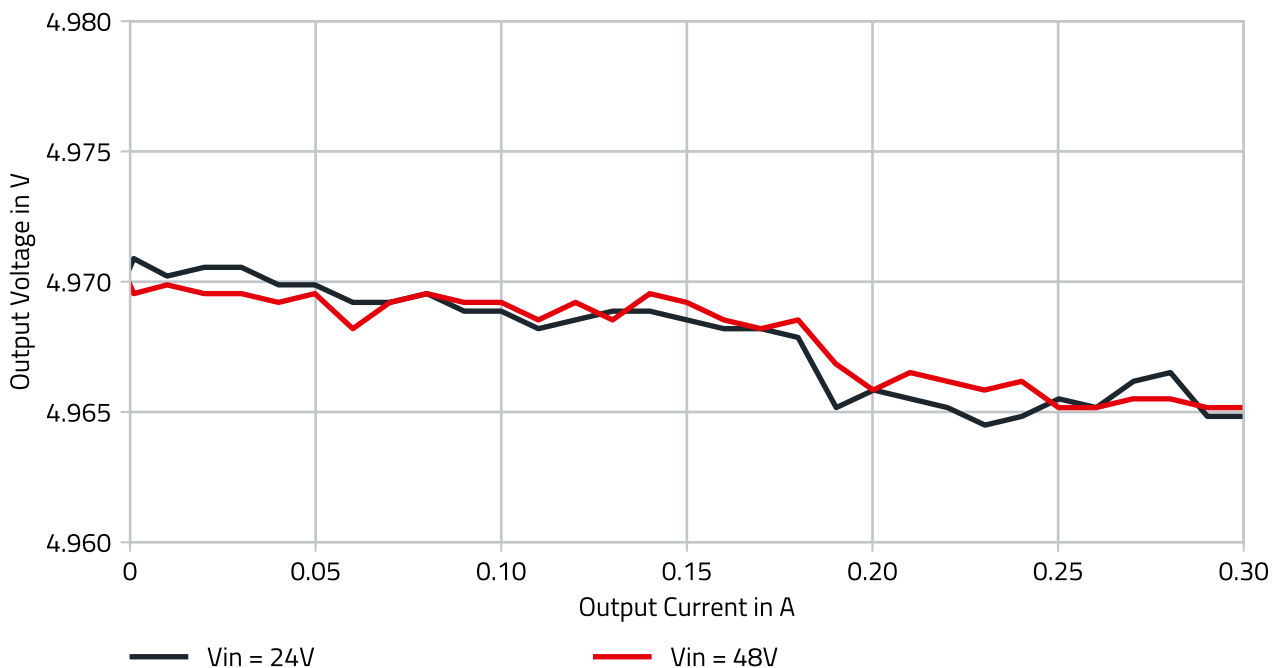


Figure 10: 171936001 load regulation $V_{OUT} = 5V$, FPWM mode.

11.2.8 Load Regulation 3.3V_{OUT} PFM

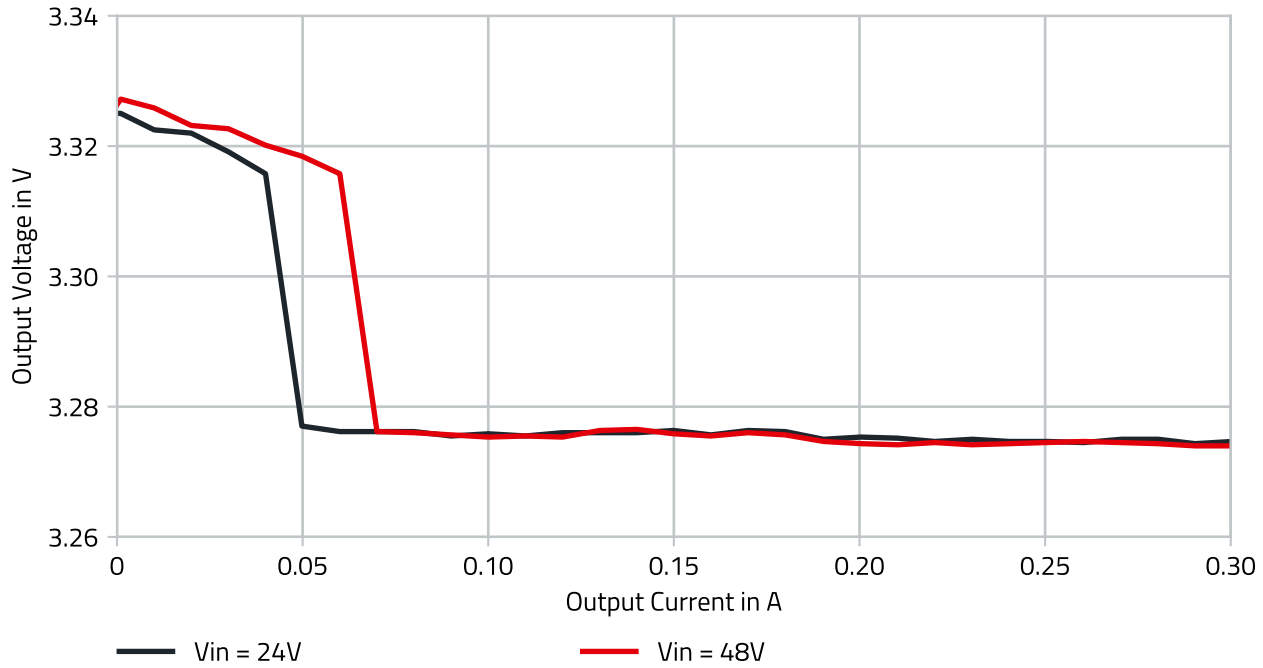


Figure 11: 171936001 load regulation $V_{OUT} = 3.3V$, PFM mode.

11.2.9 Load Regulation 5V_{OUT} PFM

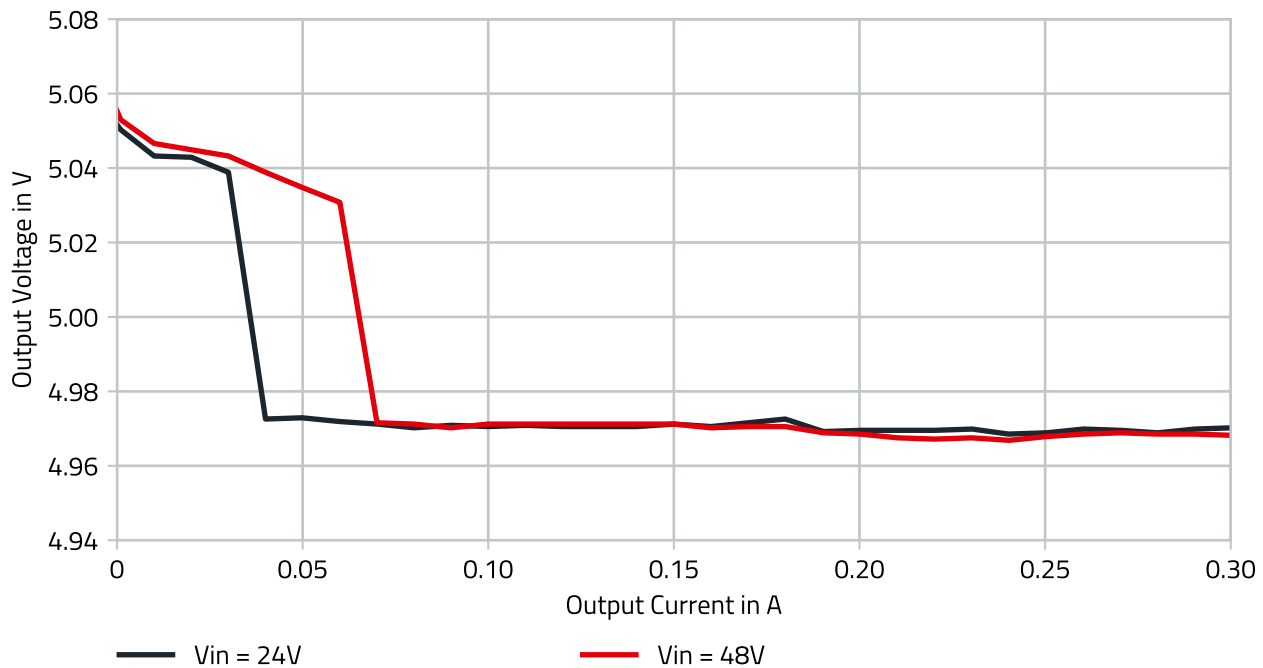


Figure 12: 171936001 load regulation $V_{OUT} = 5V$, PFM mode.

11.2.10 Line Regulation 3.3V_{OUT} FPWM

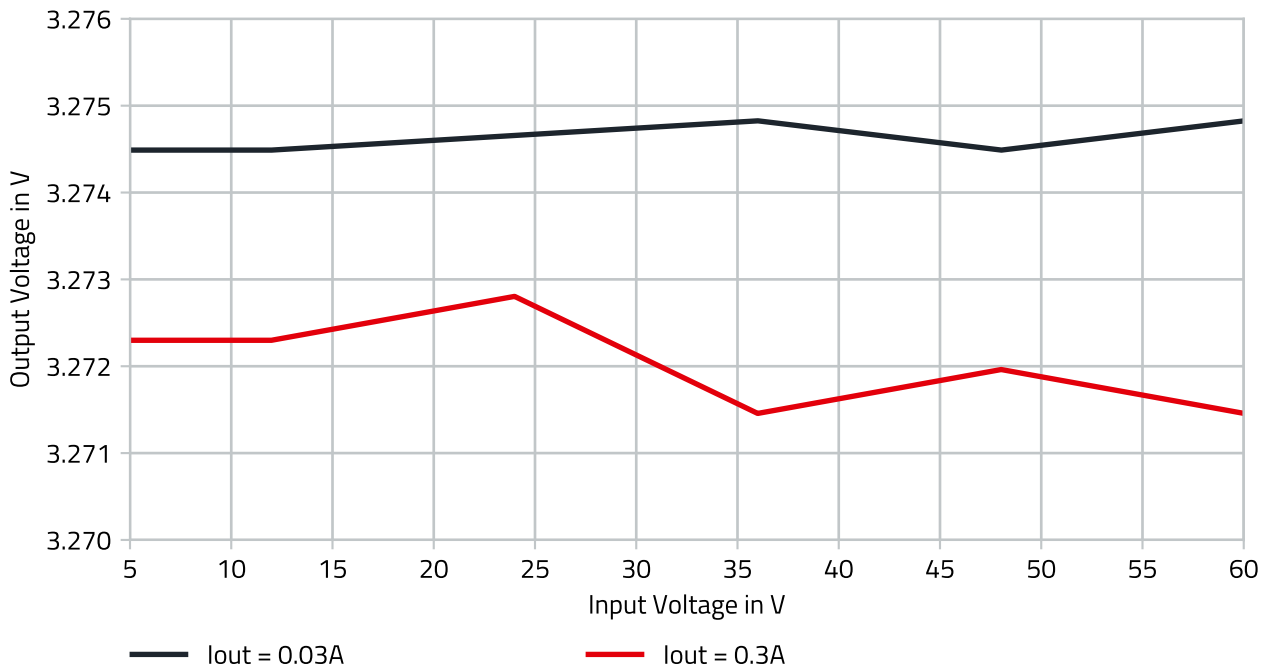


Figure 13: 171936001 line regulation V_{OUT} = 3.3V, FPWM mode.

11.2.11 Line Regulation 5V_{OUT} FPWM

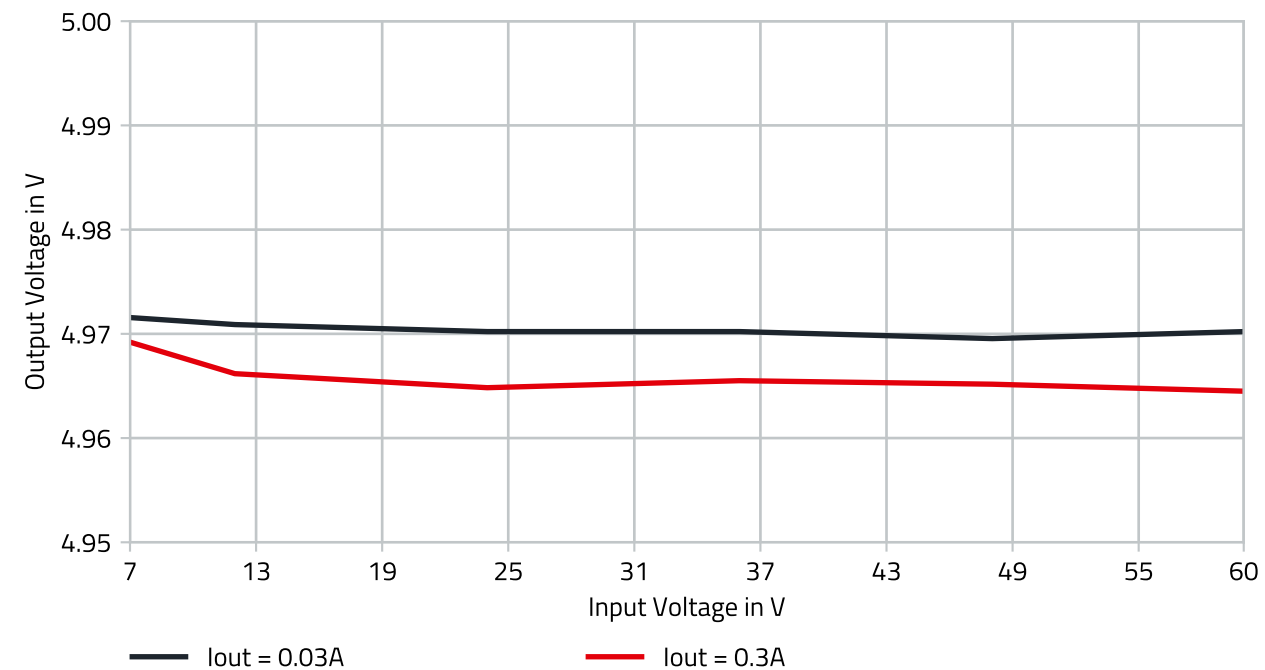


Figure 14: 171936001 line regulation V_{OUT} = 5V, FPWM mode.

11.2.12 Line Regulation 3.3V_{OUT} PFM

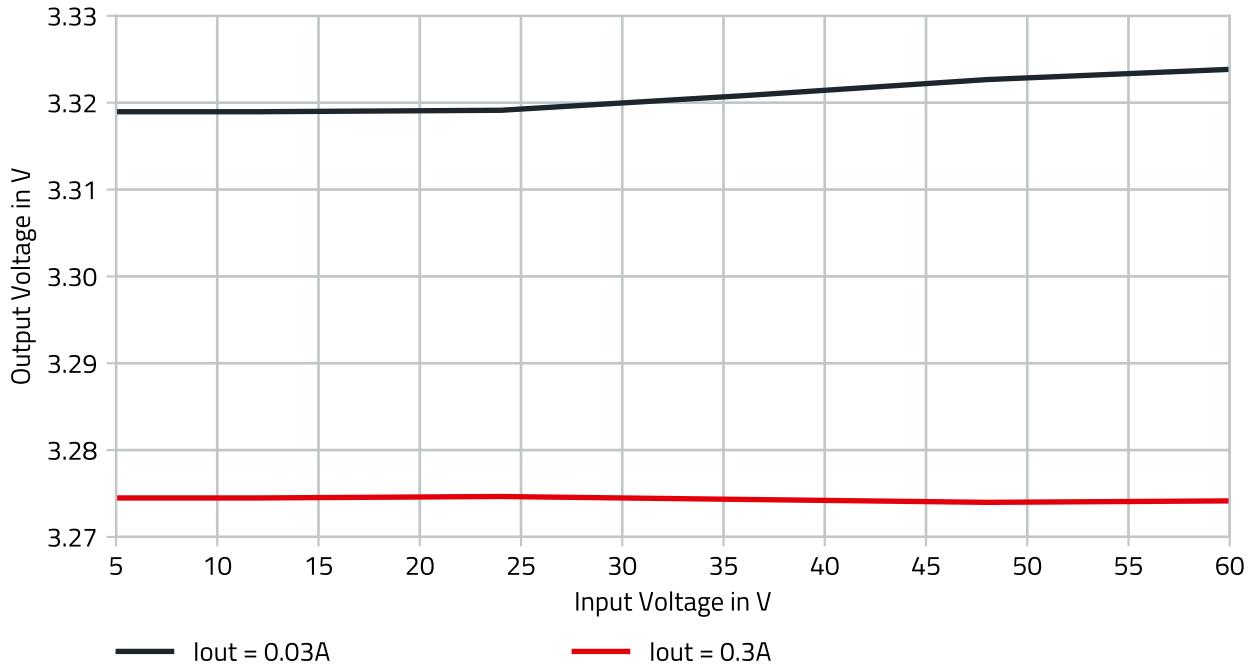


Figure 15: 171936001 line regulation $V_{OUT} = 3.3V$, PFM mode.

11.2.13 Line Regulation 5V_{OUT} PFM

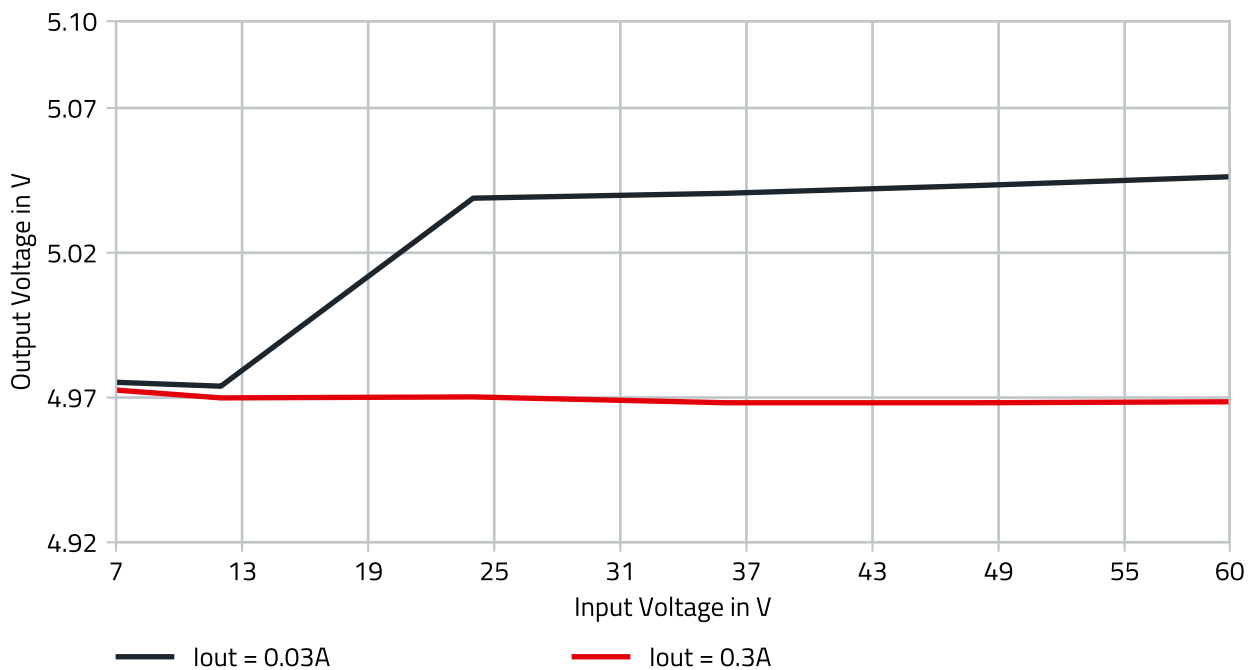


Figure 16: 171936001 line regulation $V_{OUT} = 5V$, PFM mode.

12 BLOCK DIAGRAM

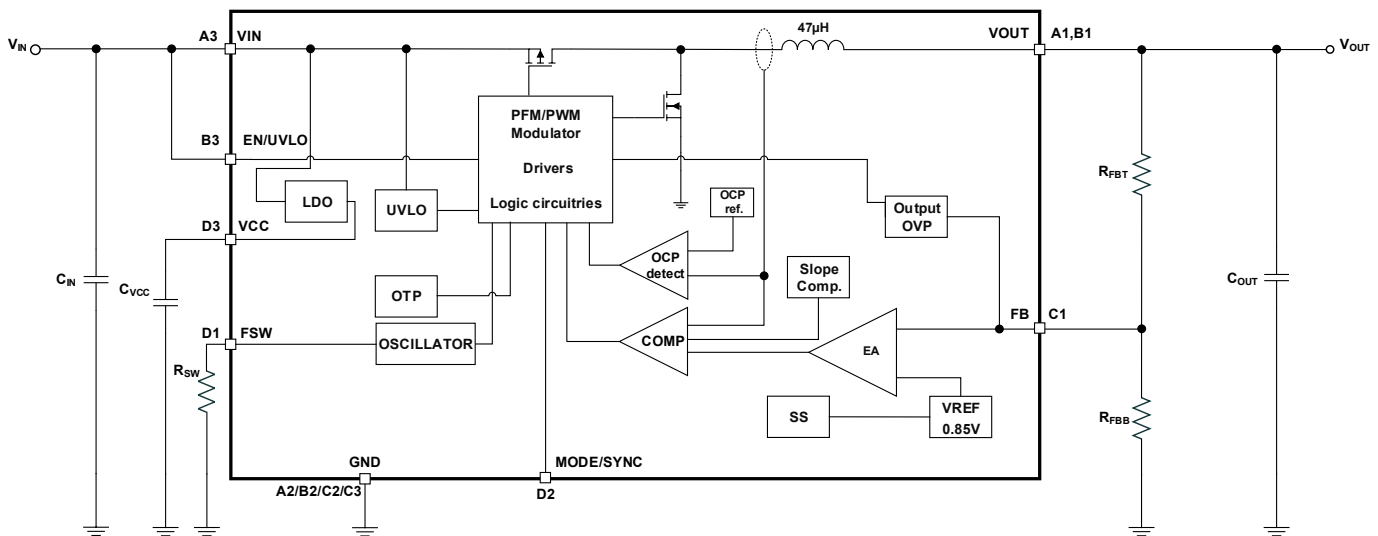


Figure 17: 171936001 block diagram.

13 CIRCUIT DESCRIPTION

The WPME-VDMM 171936001 power module is a DC-DC power supply including the switching regulator with integrated MOSFETs, controller and compensation, as well as the shielded inductor integrated in one package. The control scheme is based on a current mode (CM) regulation loop.

The V_{OUT} of the regulator is divided by the feedback resistor network R_{FBT} and R_{FBB} and fed into the FB pin. The error amplifier compares this signal with the internal 0.85V reference. The error signal is amplified and controls the on-time of a fixed frequency pulse width generator. This signal drives the power MOSFETs.

The current mode architecture features a constant frequency during load steps. Only the on-time is modulated. It is internally compensated and stable with low ESR output capacitors and requires no external compensation network.

This architecture supports fast transient response and very small output voltage ripples ($< 10mV_{p-p}$) are achieved.

14 DESIGN FLOW

The following simple steps will show how to select the external components to design the 171936001 into an application.

Essential Steps

1. Set output voltage
2. Select input capacitor
3. Select output capacitor
4. Select V_{CC} capacitor
5. Set switching frequency

Optional Steps

6. Set the UVLO level (see subsection [Enable and Integrated/Adjustable UVLO](#))

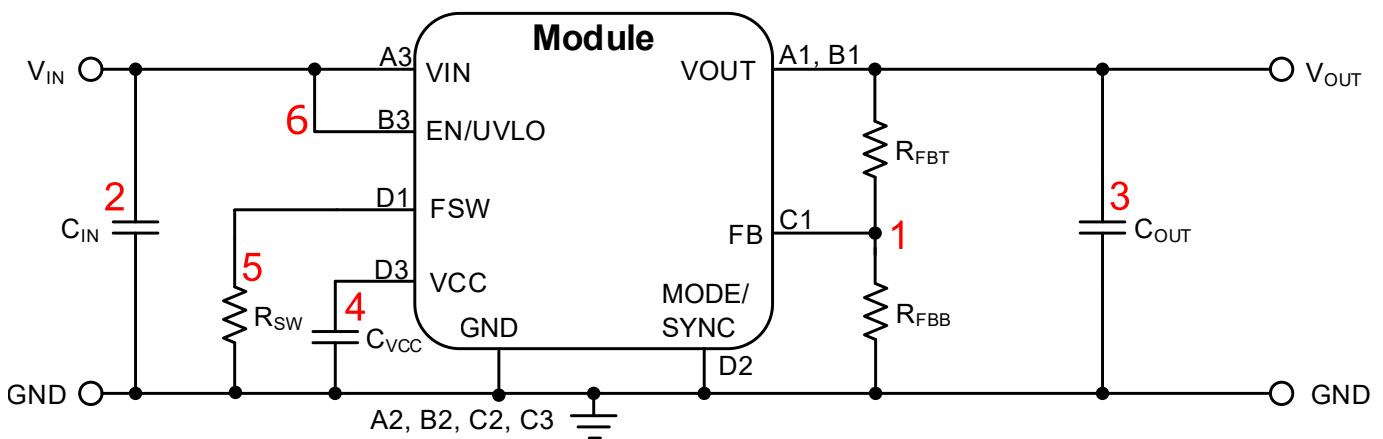


Figure 18: Design flow schematic.

14.1 STEP 1 Setting the Output Voltage (V_{OUT})

The output voltage is selected with an external resistor divider between V_{OUT} and GND (see circuit below). The voltage across the lower resistor of the divider is provided to the FB pin and compared with a reference voltage of 0.85V (V_{REF}). The output voltage adjustment range is from 0.85V to 6V. The output voltage can be calculated according to the following formula:

$$V_{OUT} = V_{REF} \cdot \left(\frac{R_{FBT}}{R_{FBB}} + 1 \right) \quad (1)$$

One resistor must be chosen and then the other resistor can be calculated. For example, if $R_{FBT} = 510k\Omega$ then the resistance value of the lower resistor in the feedback network is indicated in the table below for common output voltages.

Table 10: 171936001 output voltage selection.

V_{OUT} (V)	0.85	1.2	1.8	2.5	3.3	5.0
R_{FBB} (E96) (k Ω)	Open	1200	453	261	178	105

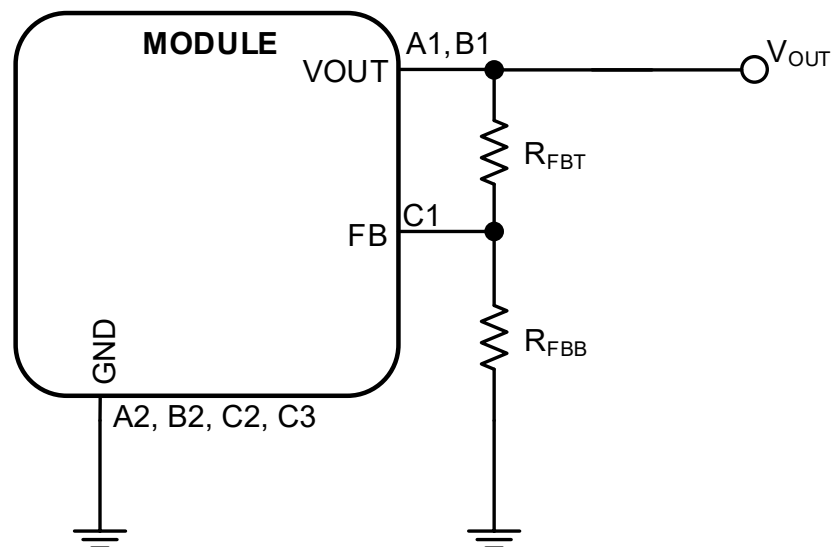


Figure 19: Output voltage selection schematic.

14.2 STEP 2 Select the Input Capacitor (C_{IN})

The energy at the input of the power module is stored in the input capacitor. An MLCC (multi-layer ceramic capacitor) input capacitors (2x 1 μ F) is required externally to provide cycle-by-cycle switching current and to support load transients. The external input capacitor must be placed directly at the VIN pin and connected with wide and short plane/trace, as shown in the design example (see subsection [Layout](#)). Attention must be paid to the voltage, frequency, temperature derating and thermal class of the selected capacitor. The Würth Elektronik 885012209069 MLCC has been experimentally verified to work with this power module. For proper operation GND connection of C_{IN} should be as close as possible to GND pins C2 and C3. If bigger capacitor packages are used attention should be paid to the parasitic inductance.

14.3 STEP 3 Select the Output Capacitor (C_{OUT})

The output capacitor should be selected in order to minimize the output voltage ripple and to provide a stable voltage at the output. It also affects the loop stability. Different output capacitors are recommended depending on the output voltage and switching frequency selected for an application. Attention must be paid to the voltage, frequency and temperature derating and thermal class of the selected capacitor.

In general, the output voltage ripple can be calculated using the following equation:

$$V_{\text{OUT,ripple}} = \Delta I_L \cdot ESR + \Delta I_L \cdot \left(\frac{1}{8 \cdot f_{\text{SW}} \cdot C_{\text{OUT}}} \right) \quad (2)$$

where ΔI_L is the inductor current ripple and can be calculated with the following equation:

$$\Delta I_L = \frac{V_{\text{OUT}} \cdot (V_{\text{IN}} - V_{\text{OUT}})}{f_{\text{SW}} \cdot L \cdot V_{\text{IN}}} \quad (3)$$

The following table shows common output voltage values and their corresponding recommended output capacitance. These capacitance values have all been experimentally verified for their corresponding output voltages. Use of different output capacitors for a given output voltage requires the designer to verify the selected capacitor(s) for functionality. These capacitors can all be found within the Würth Elektronik capacitor portfolio, specifically the WCAP-CSGP and WCAP-PSLP families.

Table 11: 171936001 output capacitor selection.

$V_{\text{OUT}} \text{ (V)}$	0.85	1.2	1.8	2.5	3.3	5.0
C_{OUT}	82 μF polymer capacitor + 3x 4.7 μF MLCC (6.3V)	82 μF polymer capacitor + 3x 4.7 μF MLCC (6.3V)	15 μF polymer capacitor + 3x 4.7 μF MLCC (6.3V)	3x 4.7 μF MLCC (10V)	2x 4.7 μF MLCC (10V)	4.7 μF MLCC (10V)

Using the recommended output capacitors, the transient response of the power module can appear as follows:

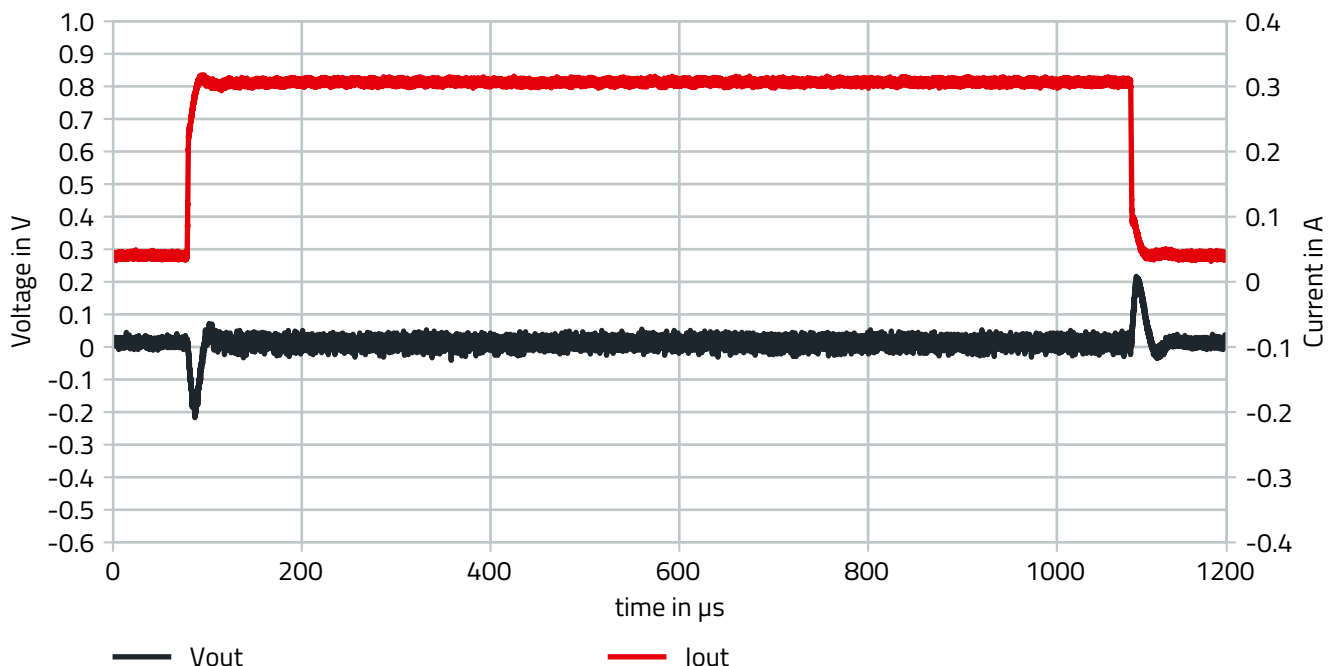


Figure 20: 171936001 transient response $V_{\text{IN}} = 48\text{V}$, $V_{\text{OUT}} = 5\text{V}$, $I_{\text{OUT}} = 0.03\text{A}$ to 0.3A , $C_{\text{OUT}} = 4.7\mu\text{F}$, FPWM mode.

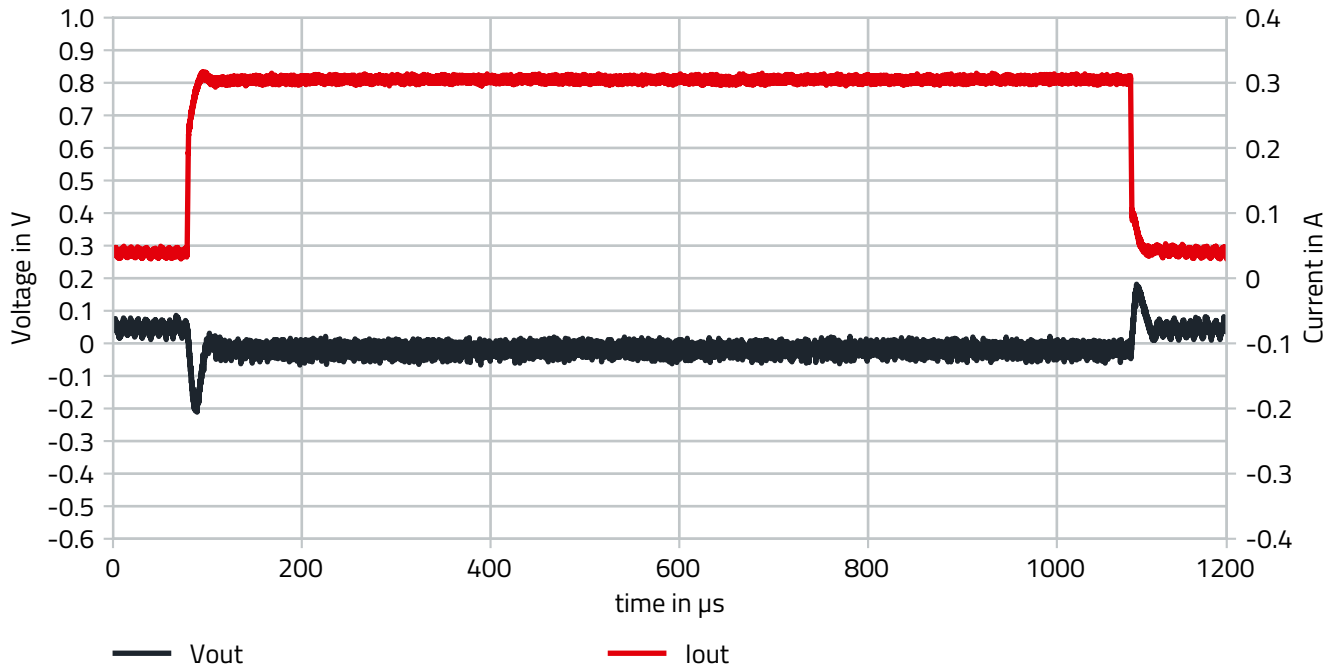


Figure 21: 171936001 transient response $V_{IN} = 48V$, $V_{OUT} = 5V$, $I_{OUT} = 0.03A$ to $0.3A$, $C_{OUT} = 4.7\mu F$, PFM mode.

14.4 STEP 4 Select the V_{CC} Capacitor (C_{VCC})

The 171936001 Magl³C Module requires a capacitor (C_{VCC}) to be placed at the VCC pin to support the internal LDO integrated inside of the module. To ensure stable operation and optimum performance across the entire functional range, a $0.47\mu F$ capacitor is recommended. The Würth Elektronik 885012207049 capacitor has been experimentally evaluated for performance and is the recommended choice.

14.5 STEP 5 Select the Switching Frequency (f_{SW})

The switching frequency must be selected according to the output voltage for the best performance in loop regulation and transient response. This is done by choosing a resistor value from the table below based on the application conditions. This resistor can either be tied directly to GND for a fixed switching frequency, indicated in the table below, or it can be tied to VCC, allowing for spread spectrum operation. Spread spectrum operation will allow for a change in switching frequency typically of $\pm 5\%$. The peaks of the switching spectrum will be reduced and spread, reducing the filter necessary to comply with EN55032 Radiated and Conducted Standards. The difference in EMI behavior can be seen in the EMI section of the data sheet .

Table 12: 171936001 switching frequency selection.

V_{OUT} (V)	0.85	1.2	1.8	2.5	3.3	5
Switching Frequency (kHz)	200	200	400	500	700	1000
R_{SW} (k Ω)	1.8	1.8	3.3	5.6	10	0

When R_{SW} is indicated as 0 k Ω , FSW should be tied directly to GND or VCC.

For high conversion ratios, when the input voltage gets very close to the full input voltage, the minimum on-time will be violated. In order to maintain a proper operation of the power module, the minimum on-time is masked and pulses are skipped, even under FPWM operation. Sticking to the recommended switching frequency results in minimizing the range where masking the on-time and pulse skipping takes place. These values have been experimentally validated for optimum performance with the given output voltages. Deviation from the recommendations is taken at the user's own risk and should be experimentally evaluated in the designated application to ensure proper functionality.

15 MODES OF OPERATION

The 171936001 power module has two different modes of operation and the transition takes place automatically depending on the load current value. Under light load conditions, the module operates in PFM mode where the Module runs at a lower switching frequency to reduce the current consumption, which leads to achieving a higher efficiency. The PFM control is achieved by creating a single pulse to turn on the high side switch while monitoring the inductor current. The high side switch is kept on until the inductor current hits a preset value of 80mA (typ.).

After reaching this value, the high side switch is turned off and the low side switch turns on. The inductor current decreases until it reaches zero. When the inductor current reaches zero, both switches are turned off (idle time) and the output capacitor solely supplies the load with energy. While the energy is supplied to the load, the output voltage starts to drop. The Module monitors the output voltage value and when it hits a certain limit, while the two switches are off, another pulse is initiated and the cycle repeats. When the load current increases, the idle time decreases and the switching frequency increases until the nominal switching frequency is reached and the Module transitions to PWM mode.

The module will only transfer to PFM mode if the MODE/SYNC pin is connected to GND otherwise by connecting the MODE/SYNC pin to VCC the module is forced to stay in PWM operation even under light load condition.

At higher values of V_{in} the minimum on time can be violated. When this happens the power module will skip pulse even during FPWM to keep the output voltage in regulation.

16 OUTPUT VOLTAGE RIPPLE

If the power module is working in PWM mode, the output voltage ripple is very low and is determined by the switching frequency, which is set by the resistor R_{SW} . If the load current is low enough to be in the PFM mode of operation then the output voltage ripple will be higher with a frequency lower than the nominal switching frequency (see pictures below). The module will only transfer to PFM mode if the MODE/SNYC pin is connected to GND otherwise by connecting the MODE/SNYC pin to VCC the module is forced to stay in PWM operation even under light load condition.

16.1 FPWM Operation

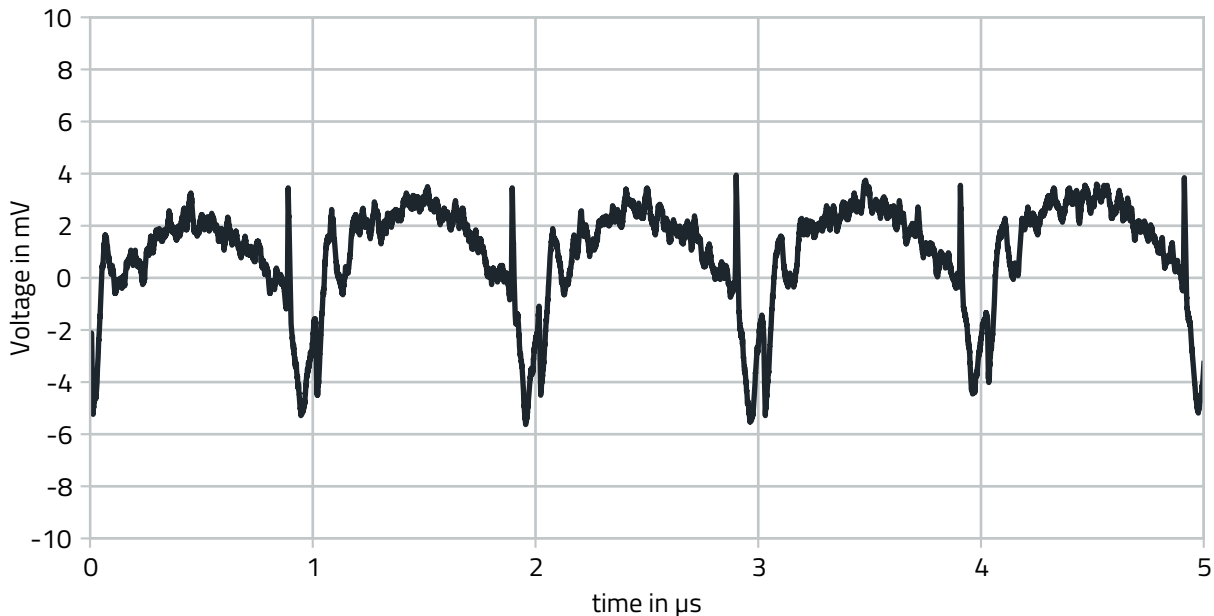


Figure 22: 171936001 output voltage ripple $V_{IN} = 48V$, $V_{OUT} = 5V$, $I_{OUT} = 0.3A$, $C_{OUT} = 4.7\mu F$, FPWM mode.

16.2 PFM Operation

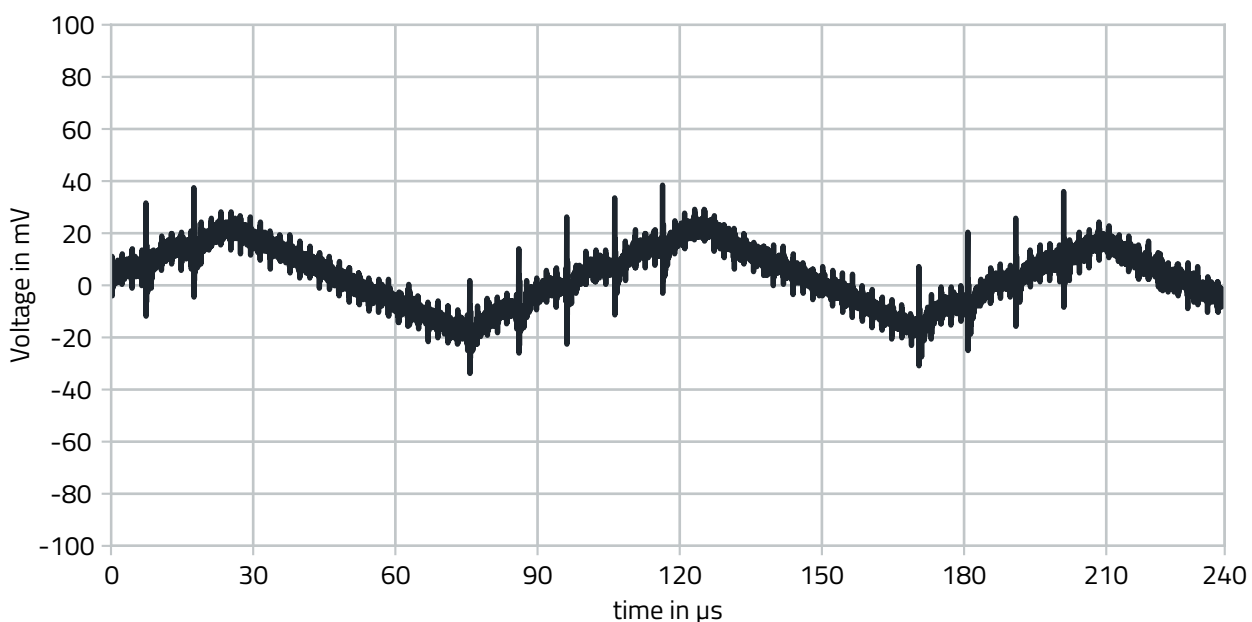


Figure 23: 171936001 output voltage ripple $V_{IN} = 48V$, $V_{OUT} = 5V$, $I_{OUT} = 0.03A$, $C_{OUT} = 4.7\mu F$, PFM mode.

17 PROTECTION FEATURES

17.1 Overcurrent Protection (OCP) and Short Circuit Protection (SCP)

The MagI³C 171936001 power module implements a cycle-by-cycle current limit (see I_{OCP} in [ELECTRICAL SPECIFICATION](#)), which is realized through the peak current mode control architecture of the power module. The peak current of the high side switch and the valley current of the low side switch are both monitored. Additionally, limiting the valley current during an overcurrent scenario reduces the thermal stresses generated inside of the power module by reducing the rms current value.

By monitoring both switch currents the user can be confident that the power module will be well protected against overcurrent and short circuit scenarios even in the most extreme conditions of operation, such as very high or low duty cycles. Under very low duty cycle conditions, the peak current can exceed the overcurrent preset value. When this occurs, the low side switch is turned on until the current drops below the preset valley current value. This behavior may result in pulse skipping, temporarily decreasing the effective switching frequency in order to better protect the power module during overcurrent scenarios.

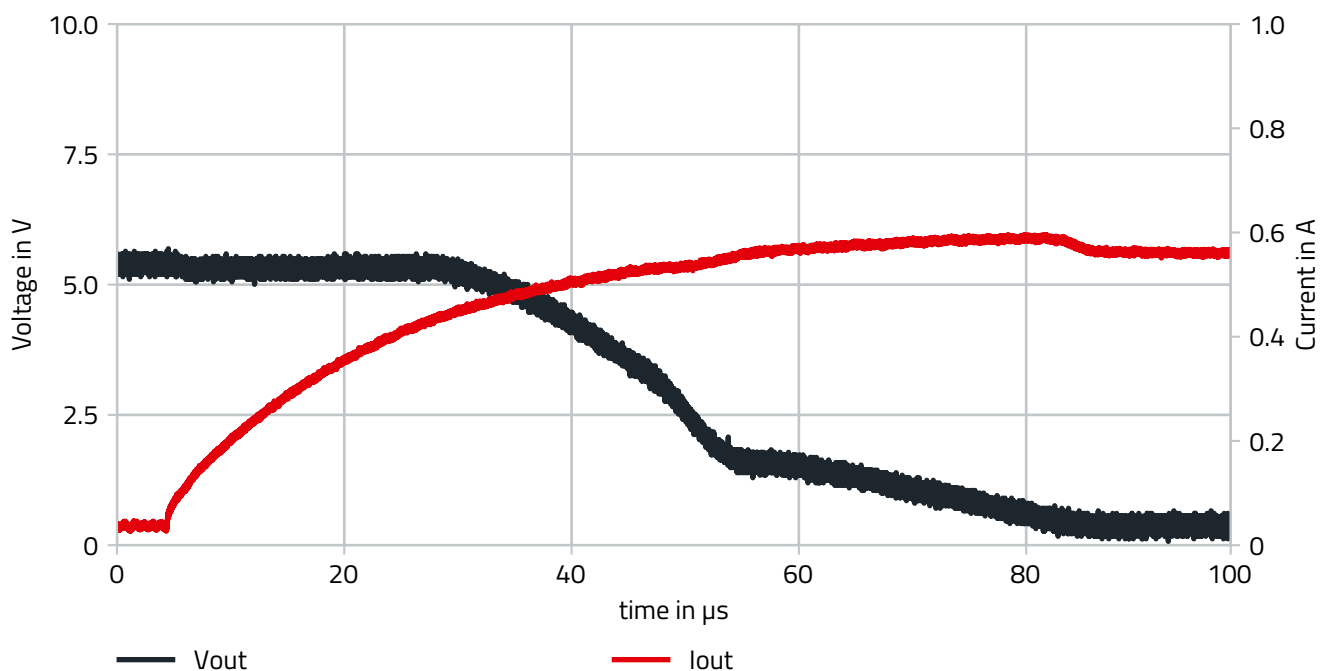


Figure 24: 171936001 overcurrent protection $V_{IN} = 48V$, $V_{OUT} = 5V$, $I_{OUT} = 0A$ to $0.47A$.

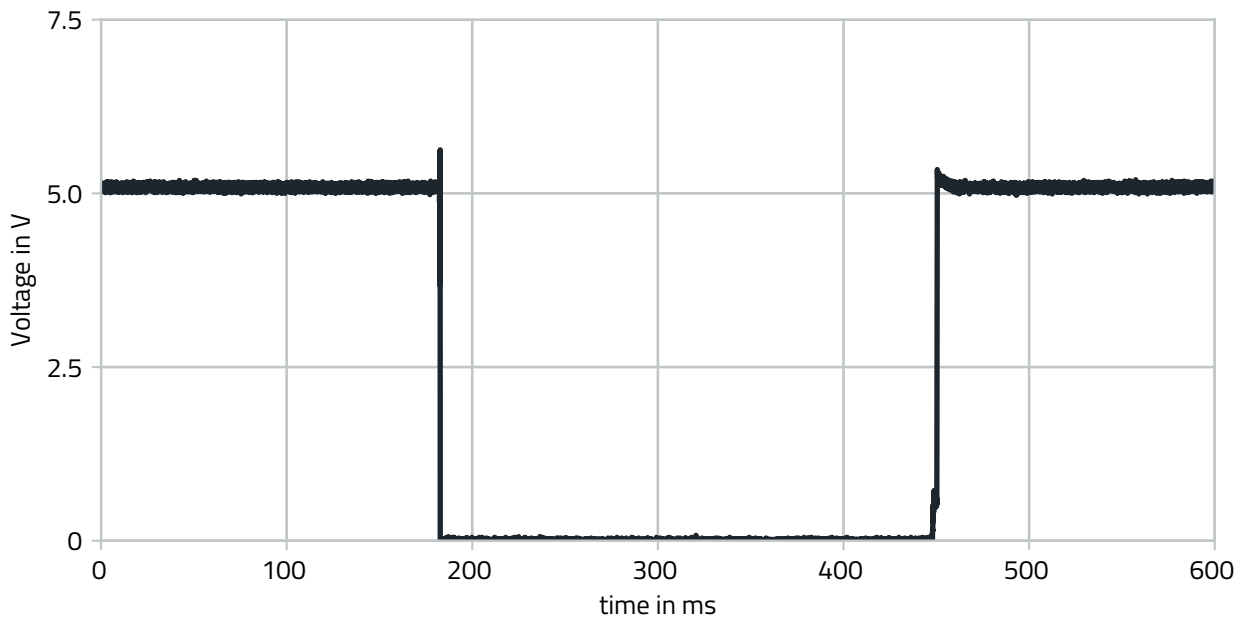


Figure 25: 171936001 short circuit protection $V_{IN} = 48V$, $V_{OUT} = 5V$.

17.2 Output Overvoltage Protection (OVP)

The Magl³C Module implements overvoltage protection. When the output voltage exceeds the desired value by typ. 20% the low side switch is turned on allowing discharging the output voltage. While the output voltage is discharged the low side switch current is monitored to prevent overstressing the low side switch. When the output voltage gets back to the desired value the normal switching behavior continues.

17.3 Over Temperature Protection (OTP)

Thermal protection helps prevent catastrophic failures due to accidental device overheating. The junction temperature of the Magl³C Module should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal thermal shutdown circuit, which activates when the junction temperature reaches 165°C (typ). Under the thermal shutdown condition both MOSFETs remain off, causing the output voltage to drop. When the junction temperature falls below 135°C (typ) the internal soft-start is released, V_{OUT} rises smoothly, and normal operation resumes.

17.4 Soft-Start

The MagI³C power module implements an internal soft-start in order to limit the inrush current and avoid output voltage overshoot during start-up. The typical duration of the soft-start is around 2ms (see Figure 27 below).

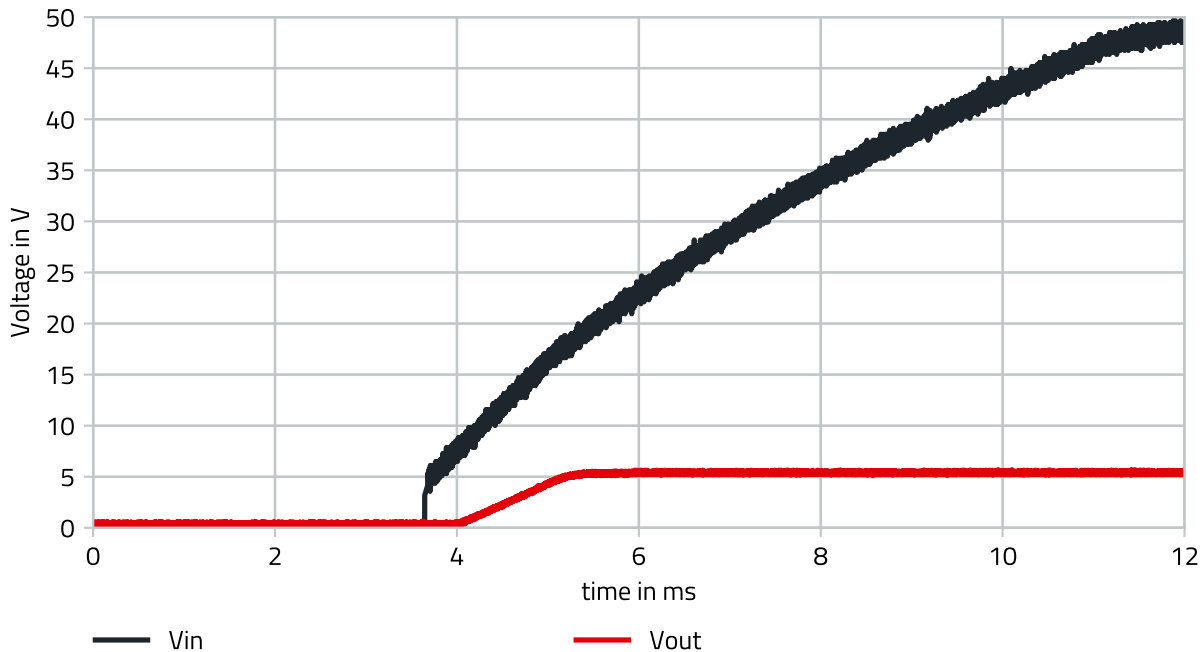


Figure 26: 171936001 soft-start $V_{IN} = 24V$, $V_{OUT} = 5V$.

The MagI³C power module supports prebiased start-up, where the output capacitor is precharged. The module does not sink current from the output during soft-start, regardless if the power module operates under PFM/PWM or FPWM mode. In case of a prebiased output, switching activities stop until the increasing internal reference exceeds the prebiased output voltage. At this point, the switching activity is enabled to complete the output capacitor charge up to the programmed value.

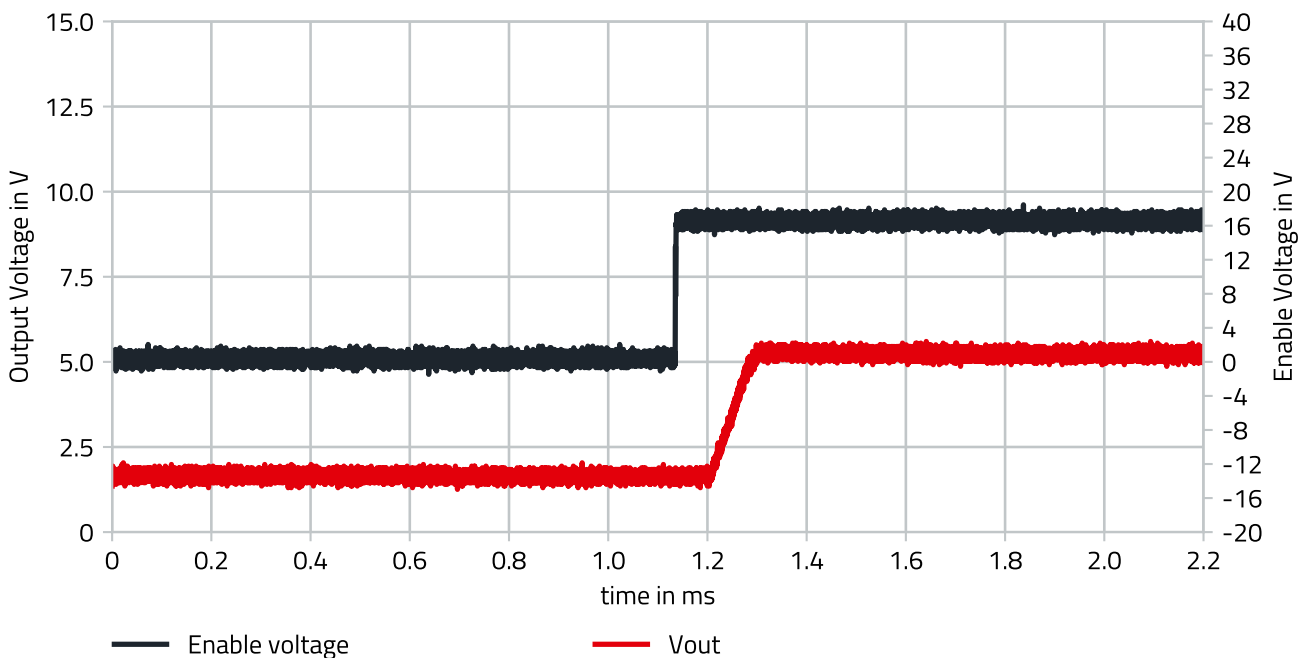


Figure 27: 171936001 prebiased start-up $V_{PREBIAS} = 2.3V$, $V_{OUT} = 5V$.

17.5 Enable and Integrated/Adjustable UVLO

The MagI³C power module is enabled by setting the EN pin high. When the EN voltage reaches 1.2V typ. the power module begins switching and the internal soft-start regulates the output voltage rise until the desired output voltage is met, allowing normal operation to take place.

The device incorporates an internal input undervoltage lockout (UVLO) to protect from unexpected behavior at input voltages below the recommended values. The thresholds of the internal UVLO are indicated in the [ELECTRICAL SPECIFICATIONS](#). An additional UVLO threshold of the power module can be externally set by adding a resistor between VIN and EN and a second resistor between EN and GND. This voltage divider should be chosen so that the desired minimum input voltage corresponds to 1.2V at EN.

The two resistors should be chosen based on the following ratio:

$$\frac{R_{\text{ENT}}}{R_{\text{ENB}}} = \frac{V_{\text{UVLO (EXT.)}}}{1.2} - 1 \quad (4)$$

$V_{\text{UVLO (EXT.)}}$ = User-programmable input voltage threshold to enable and disable the power module

This is often used in battery-powered systems to prevent deep discharge of the system battery. It is also useful in system designs with output rail sequencing or to prevent early turn-on of the supply as the main input voltage rail rises at power-up. Most systems will benefit by using the precision Enable threshold to establish a system undervoltage lockout based on specific application parameters.

In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the MagI³C power module output rail. The recommended approach is to choose an input UVLO level that is higher than the target regulated output voltage for the stage.

17.6 External Clock Synchronization (Sync)

The 171936001 MagI³C power module allows synchronization of the power module's switching frequency with an external clock source as a reference. This feature is beneficial when the user requires a switching frequency other than those offered by default by the power module, for instance to better optimize performance factors such as EMI for a specific application.

To realize this feature an external clock is directly connected to the MODE/SYNC pin. If the external clock is interrupted for 14 μ s the internal clock determined by the external resistor to select the switching frequency activates. The external clock is specified in the [ELECTRICAL SPECIFICATIONS](#) section.

It is recommended to use the default switching frequency, through the resistor R_{FSW} , closest to the external source frequency. The value of R_{ENT} is calculated to choose the UVLO value as explained in the Enable/Adjustable UVLO section above. The minimum on-time and the maximum duty cycle for the external clock source are specified in the [ELECTRICAL SPECIFICATIONS](#).

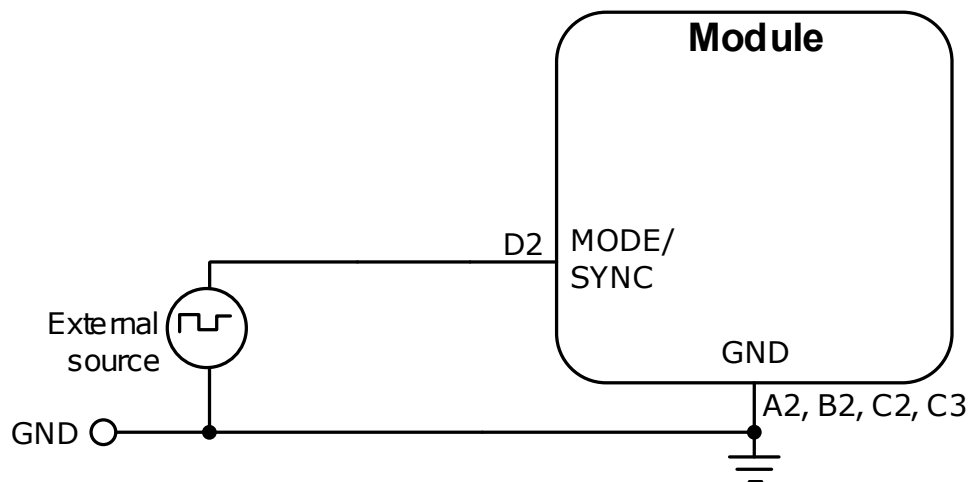


Figure 28: 171936001 sync to external signal schematic.

18 DESIGN EXAMPLE

The design example shows a possible solution for 48V to 5V with a maximum output current of 0.3A operating in PFM/PWM mode. All of the necessary components to fulfill the requirements of the CISPR 32 EMI conducted- and radiated emissions tests are included in the design example. It passes the conducted emissions class B with 0.8m input and 1m output lines. Filter components may be omitted depending on the requirements of the final application. Further, the EMI filter is needed in case the input voltage supplying the application is expected to have very fast transitions which may have negative impact on the operation of the power module.

18.1 Layout

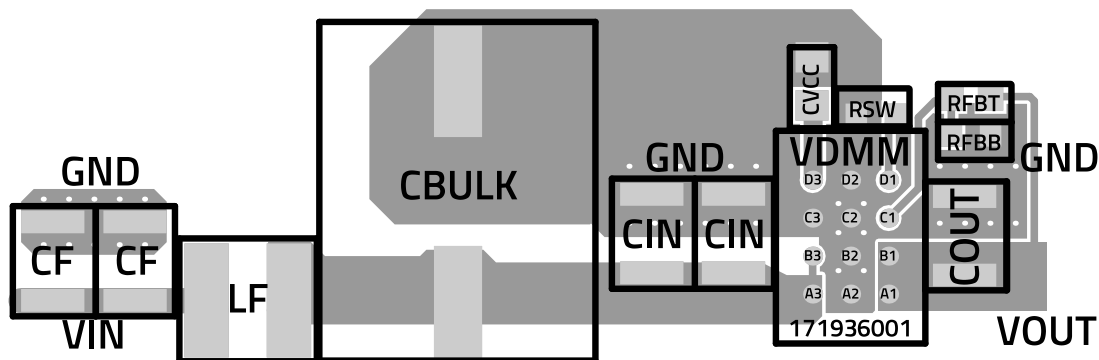


Figure 29: 171936001 layout recommendation.

The image above shows the top routed layer for a recommended two layer layout. The bottom layer is used as GND plane and filled with copper. It shows a possible layout for the 171936001 MagI³C power module, where the spread spectrum feature for improved EMI performance is disabled. Nevertheless, some recommendations should be followed when designing the layout:

1. The input and output capacitors should be placed as close as possible to the VIN and VOUT pins of the device.
2. The GND connection of the input capacitors should be placed as close as possible to GND pins C2 and C3.
3. The feedback resistor divider should be placed as close as possible to the FB pin.
4. Avoid placing vias in any of the pads for the module.
5. Connect Vin pads of the input capacitor with wide and short plane/trace.
6. Use as wide GND plane possible to ensure stable operation of the power module.
7. Use an uninterrupted GND plane on bottom layer, connected with adequate number of vias to top layer to improve thermal performance and EMI behavior.
8. To avoid direct coupling of the DC/DC converter's E- and H-fields into connectors, the susceptible components and traces must be placed as far away from the module as possible.

18.2 Schematic

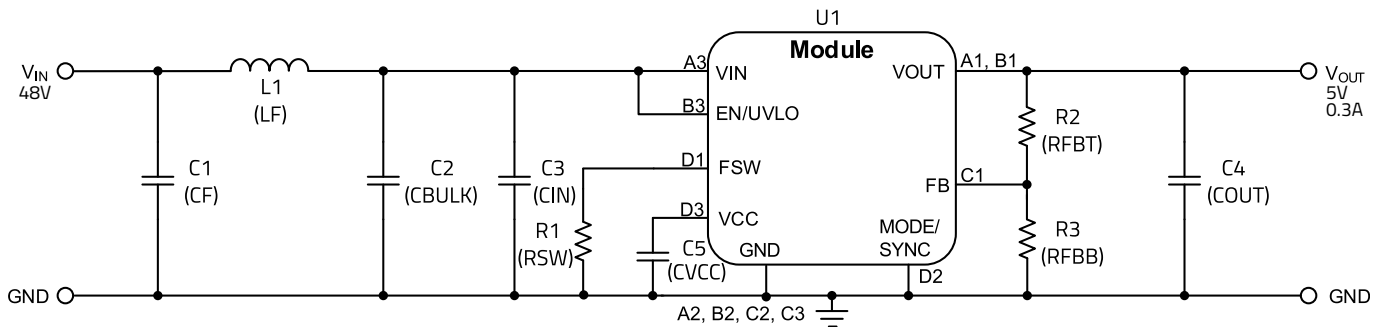


Figure 30: 171936001 design example schematic.

18.3 Bill of Materials

Table 13: 171936001 design example bill of materials.

Designator	Description	Function	Quantity	Order Code	Manufacturer
U1	MagI ³ C power module	Power supply	1	171936001	WE
L1	Filter inductor, 2.2μH, PD2 family, I _{SAT} = 3.38A, I _R = 2.5A	Input filter	1	744773022	WE
C1	Ceramic chip capacitor 1μF, 100V, X7R, 1210	Input filter	2	885012209069	WE
C2	Aluminum polymer capacitor 12μF, 100V	Input filter	1	875115957002	WE
C3	Ceramic chip capacitor 1μF, 100V, X7R, 1210	Electrical performance	2	885012209069	WE
C4	Ceramic chip capacitor 4.7μF, 16V, X7R, 1210	Electrical performance	1	885012209013	WE
C5	Ceramic chip capacitor 0.47μF, 16V, X7R, 0805	Electrical performance	1	885012207049	WE
R1	0Ω	Electrical performance	1	—	—
R2	510kΩ	Electrical performance	1	—	—
R3	105kΩ	Electrical performance	1	—	—

19 HANDLING RECOMMENDATIONS

1. The power module is classified as MSL3 (JEDEC Moisture Sensitivity Level 3) and requires special handling due to moisture sensitivity (JEDEC J-STD033D).
2. The parts are delivered in a sealed bag (Moisture Barrier Bag = MBB) and should be processed within one year.
3. When opening the moisture barrier bag, check the Humidity Indicator Card (HIC) for color status. Bake parts prior to soldering in case indicator color has changed according to the notes on the card.
4. Parts must be processed after 168 hour (7 days) of floor life. Once this time has been exceeded, bake parts prior to soldering per JEDEC J-STD033D recommendation.
5. Maximum number of solder cycles is two.
6. For minimum risk, solder the module in the last solder cycle of the PCB production.
7. For soldering process please consider lead material NiPdAu and lead finish ENEPIG.
8. It is recommended to use a standard SAC Alloy such as SAC 305, type 3 or higher.
9. The profile below is valid for convection reflow only.
10. Other soldering methods (e.g. vapor phase) are not verified and have to be validated by the customer at their own risk.

20 SOLDER PROFILE

Table 14: Reflow solder profile.

Profile Feature	Symbol	Value
Preheat temperature minimum	T_{s_min}	150°C
Preheat temperature maximum	T_{s_max}	200°C
Preheat time from T_{s_min} to T_{s_max}	t_s	60-120 seconds
Liquidous temperature	T_L	217°C
Time maintained above T_L	t_L	60-150 seconds
Classification temperature	T_C	260°C
Peak package body temperature	T_P	$T_P \leq T_C$
Time within 5°C of actual peak temperature	t_p	$t_p \leq 30$ seconds
Ramp-up Rate (T_L to T_P)		3°C/second maximum
Ramp-down rate (T_P to T_L)		6°C/second maximum
Time 25°C to peak temperature		8 minutes maximum

Please refer to JEDEC J-STD020E for further information pertaining to reflow soldering of electronic components.

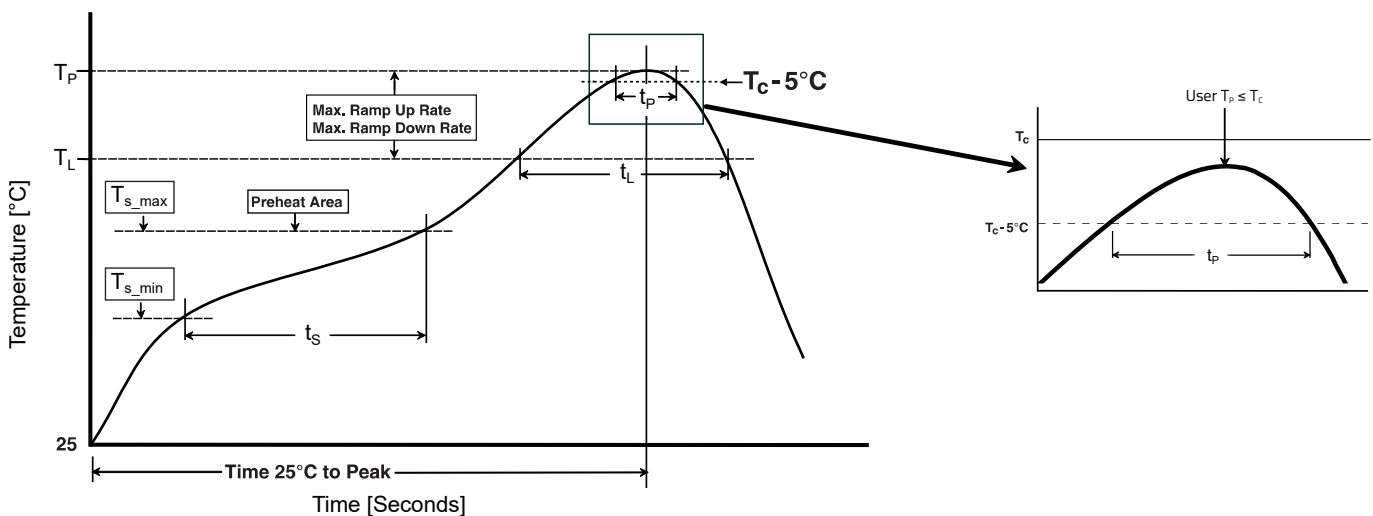


Figure 31: Solder profile.

21 PHYSICAL DIMENSIONS

21.1 Component

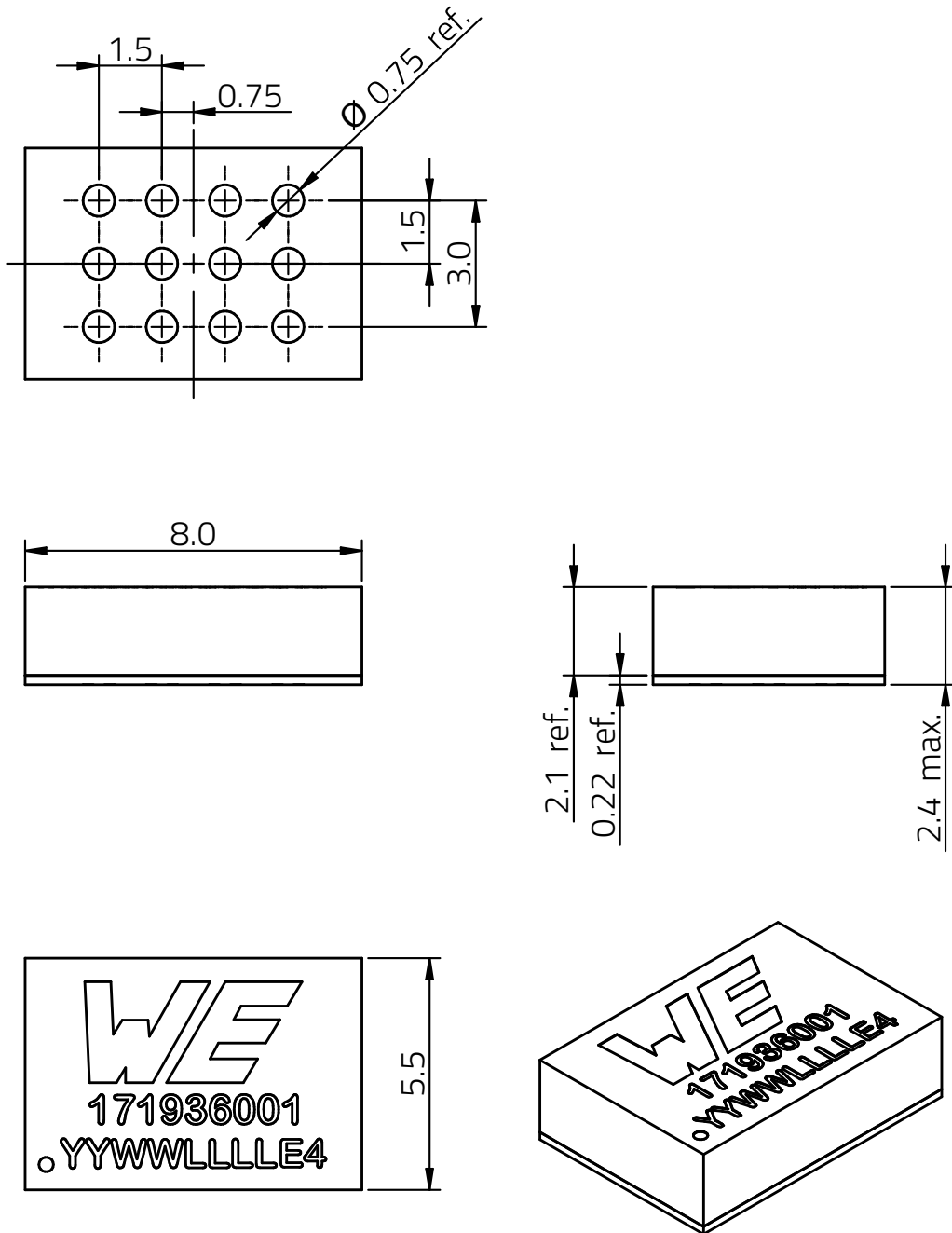


Figure 32: Physical dimensions.

All dimensions in mm
Tolerances ± 0.1 mm unless otherwise specified

21.2 Example Landpattern

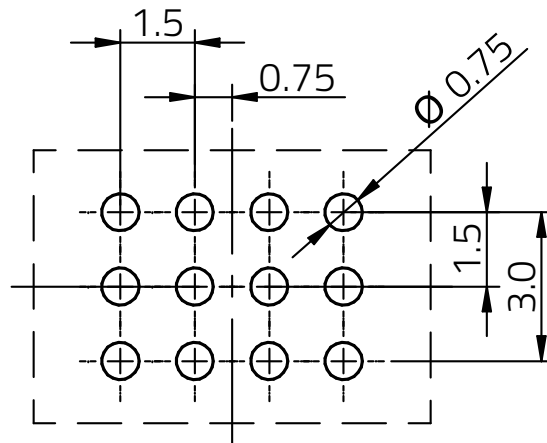


Figure 33: Example landpattern design.

All dimensions in mm
Stencil thickness of 100µm

21.3 Packaging

Tape

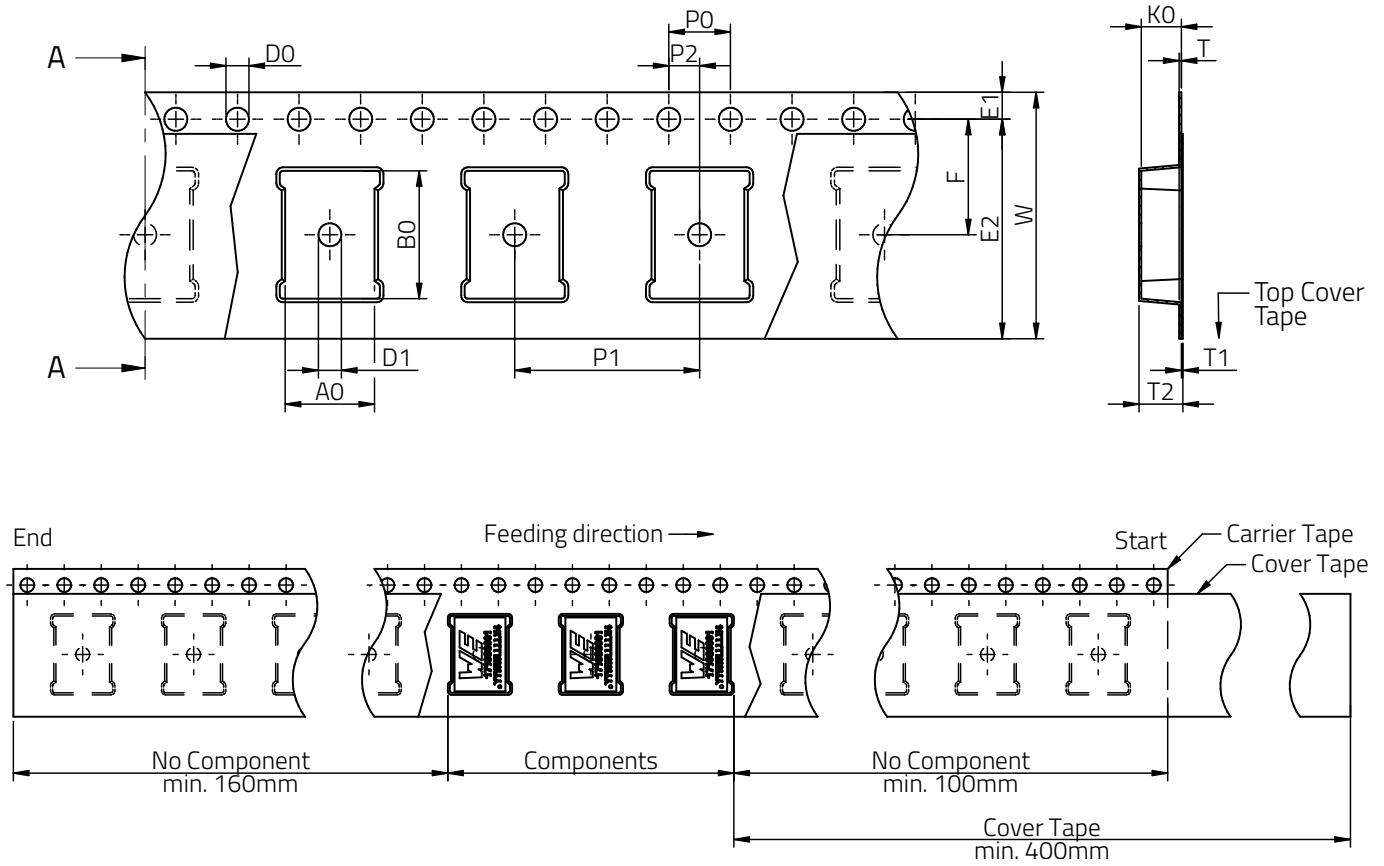


Figure 34: Tape.

Table 15: Tape dimensions.

Tape Type	A0	B0	W	T	T1	T2	K0	P0	P1	P2	D0	D1	E1	E2	F	Material
	typ.	typ.	+0.3/ -0.1	ref.	ref.	typ.	typ.	±0.1	±0.1	±0.1	+0.1/ -0.0	min.	±0.1	min.	±0.1	
2a	5.8	8.3	16.00		0.10	2.80	2.60	4.00	12.00	2.00	1.50	1.50	1.75	14.25	7.50	Polystyrene

All dimensions in mm

Reel

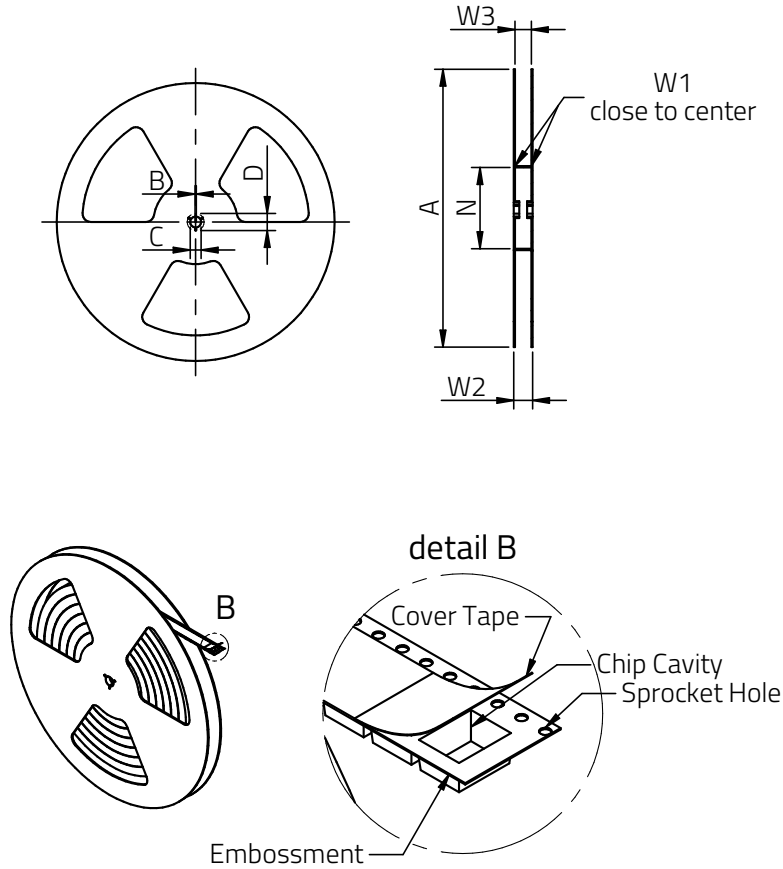


Figure 35: Reel.

Table 16: Reel dimensions.

A	B	C	D	N	W1	W2	W3	W3	Material
±2.0	min.	min.	min.	min.	±2.0	max.	min.	max.	
330.00	1.50	12.80	20.20	60.00	16.40	22.40	15.90	19.40	Polystyrene

All dimensions in mm

22 DOCUMENT HISTORY

Table 17: Document history.

Revision	Date	Description	Comment
1.0	July 2024	Initial data sheet release	

23 LIST OF FIGURES

1	Pinout.	4
2	Radiated emissions.	10
3	Conducted emissions.	10
4	Efficiency $V_{IN} = 24V$, FPWM mode.	11
5	Efficiency $V_{IN} = 48V$, FPWM mode.	11
6	Efficiency $V_{IN} = 24V$, PFM mode.	12
7	Efficiency $V_{IN} = 48V$, PFM mode.	12
8	Output current thermal derating $V_{IN} = 48V$	13
9	Load regulation $V_{OUT} = 3.3V$, FPWM mode.	14
10	Load regulation $V_{OUT} = 5V$, FPWM mode.	14
11	Load regulation $V_{OUT} = 3.3V$, PFM mode.	15
12	Load regulation $V_{OUT} = 5V$, PFM mode.	15
13	Line regulation $V_{OUT} = 3.3V$, FPWM mode.	16
14	Line regulation $V_{OUT} = 5V$, FPWM mode.	16
15	Line regulation $V_{OUT} = 3.3V$, PFM mode.	17
16	Line regulation $V_{OUT} = 5V$, PFM mode.	17
17	Block diagram.	18
18	Design flow schematic.	19
19	Output voltage selection schematic.	20
20	Transient response $V_{IN} = 48V$, $V_{OUT} = 5V$, $I_{OUT} = 0.03A$ to $0.3A$, $C_{OUT} = 4.7\mu F$, FPWM mode.	21
21	Transient response $V_{IN} = 48V$, $V_{OUT} = 5V$, $I_{OUT} = 0.03A$ to $0.3A$, $C_{OUT} = 4.7\mu F$, PFM mode.	22
22	Output voltage ripple $V_{IN} = 48V$, $V_{OUT} = 5V$, $I_{OUT} = 0.3A$, $C_{OUT} = 4.7\mu F$, FPWM mode.	24
23	Output voltage ripple $V_{IN} = 48V$, $V_{OUT} = 5V$, $I_{OUT} = 0.03A$, $C_{OUT} = 4.7\mu F$, PFM mode.	24
24	Overcurrent protection $V_{IN} = 48V$, $V_{OUT} = 5V$, $I_{OUT} = 0A$ to $0.47A$	25
25	Short circuit protection $V_{IN} = 48V$, $V_{OUT} = 5V$	26
26	Soft-start $V_{IN} = 24V$, $V_{OUT} = 5V$	27
27	Prebiased start-up $V_{PREBIAS} = 2.3V$, $V_{OUT} = 5V$	27
28	Sync to external signal schematic.	29
29	Layout recommendation for fixed frequency operation.	30
30	Design example schematic.	31
31	Solder profile.	32
32	Physical dimensions.	33
33	Example landpattern design.	34
34	Tape.	35
35	Reel.	36

24 LIST OF TABLES

1	Pin description.	4
2	Ordering information.	5
3	Sales information.	5
4	Absolute maximum ratings.	6
5	Operating conditions.	6
6	Thermal specifications.	6
7	Electrical specifications part 1.	7
8	RoHS, REACh.	8
9	Package specifications.	8
10	Output voltage selection.	20
11	Output capacitor selection.	21
12	Switching frequency selection.	22
13	Design example bill of materials.	31
14	Reflow solder profile.	32
15	Tape dimensions.	35
16	Reel dimensions.	36
17	Document history.	37

25 CAUTIONS AND WARNINGS

The following conditions apply to all goods within the product series of MagI³C of Würth Elektronik eiSos GmbH & Co. KG:

General:

- All recommendations according to the general technical specifications of the data-sheet have to be complied with.
- The usage and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.
- The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products
- Residual washing varnish agent that is used during the production to clean the application might change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long term function of the product. Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.
- Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG.
- Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions
- Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications

Product specific:

Follow all instructions mentioned in the datasheet, especially:

- The solder profile has to comply with the technical reflow or wave soldering specification, otherwise this will void the warranty.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will void the warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

Disclaimer:

This electronic component has been designed and developed for usage in general electronic equipment only. This product is not authorized for use in equipment where a higher safety standard and reliability standard is especially required or where a failure of the product is reasonably expected to cause severe personal injury or death, unless the parties have executed an agreement specifically governing such use. Moreover Würth Elektronik eiSos GmbH & Co. KG products are neither designed nor intended for use in areas such as military, aerospace, aviation, nuclear control, submarine, transportation (automotive control, train control, ship control), transportation signal, disaster prevention, medical, public information network etc. Würth Elektronik eiSos GmbH & Co. KG must be informed about the intent of such usage before the design-in stage. In addition, sufficient reliability evaluation checks for safety must be performed on every electronic component which is used in electrical circuits that require high safety and reliability functions or performance. These cautions and warnings comply with the state of the scientific and technical knowledge and are believed to be accurate and reliable. However, no responsibility is assumed for inaccuracies or incompleteness.

26 IMPORTANT NOTES

General Customer Responsibility

Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that the datasheet is current before placing orders.

Customer Responsibility Related to Specific, in Particular Safety-Relevant, Applications

It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

Best Care and Attention

Any product-specific notes, warnings and cautions must be strictly observed. Any disregard will result in the loss of warranty.

Customer Support for Product Specifications

Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

Product R&D

Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard we inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

Product Life Cycle

Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

Property Rights

All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG. Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

General Terms and Conditions

Unless otherwise agreed in individual contracts, all orders are subject to the current version of the "General Terms and Conditions of Würth Elektronik eiSos Group", last version available at www.we-online.com.