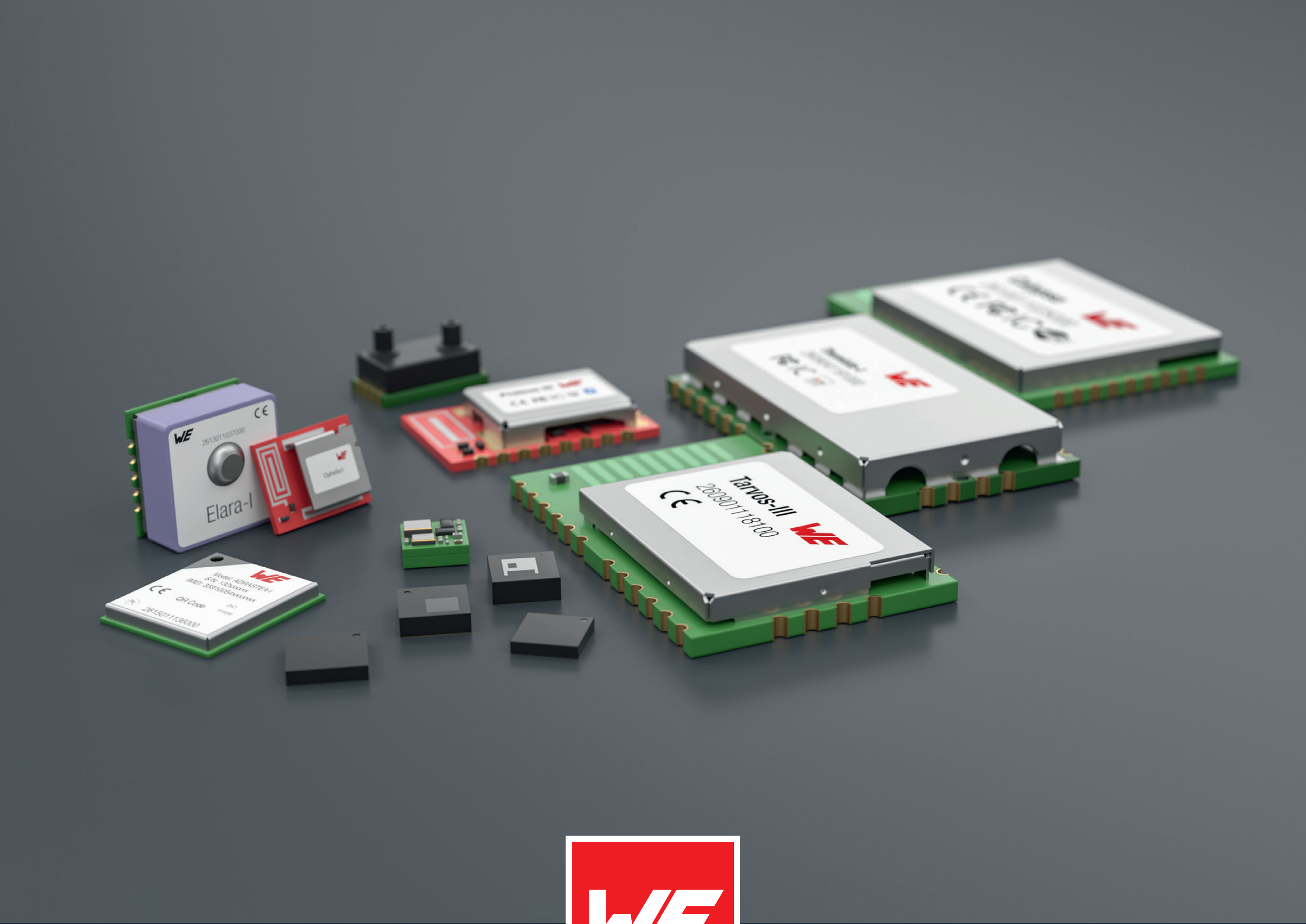


User manual

WSEN-ISDS Inertial Measurement Unit

2536030320001,
2536030320001 1

Version 1.3

July 18, 2024

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

Revision history

Manual version	Product version	Notes	Date
1.0	1.0	• Initial release of the manual	December 2022
1.1	1.0	• Chapter 15.2: Footprint dimension is updated • Chapter 10 : 'Application specific sensor features' is updated	May 2023
1.2	1.0	• Chapter 14.50: Corrected alignment error	January 2024
1.3	1.0	• Chapter 12.2, Chapter 12.3: Corrected the concatenation equation • Chapter 15.1: Corrected the sensor axes	July 2024

Abbreviations

Abbreviation	Description
ASIC	Application specific integrated circuit
BDU	Block update data
BLE	Big/Little Endian
DRDY	Data ready
DC	Direct current
ESD	Electrostatic discharge
FIFO	First-in first-out
HBM	Human body model
I^2C	Inter integrated circuit
IMU	Inertial measurement unit
LSB	Least significant bit
LGA	Land grid array
MEMS	Micro-Electro Mechanical system
MSB	Most significant bit
MSL	Moisture sensitivity level
ODR	Output data rate
PCB	Printed circuit board
SPI	Serial peripheral interface

Contents

Overview of helpful application notes

Application note ANM001 - MEMS Sensor PCB design and soldering guideline

http://www.we-online.com/ANM001
This technical document provides necessary information and general guidelines for soldering and PCB design for the Würth Elektronik eiSos MEMS sensor products with an LGA surface-mount package.

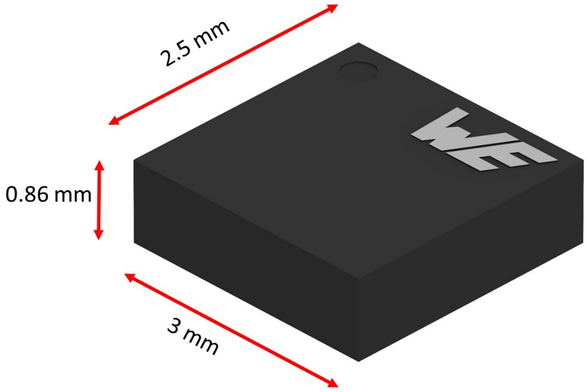
1 Product description

1.1 Introduction

The IMU sensor is a 16-bit digital ultra-low power and high performance sensor with 3-axis linear accelerometer and 3-axis gyroscope with digital I^2C and SPI serial interface. It measures user selectable acceleration range of ±2*g*, ±4*g*, ±8*g*, ±16*g* and an angular rate range of ±125 dps, ±250 dps, ±500 dps, ±1000 dps, ±2000 dps with an output data rate up to 6.66kHz. It consists of an in-built FIFO buffer to store the output data. The dimension of the sensor is 2.5 ×3.0 ×0.86 mm. It is available in land grid array package (LGA).

1.2 Applications

- Localization and navigation
- Industrial tools and factory equipment
- Antenna and platform stabilization
- Industrial IoT and connected devices
- Robotics, drones and automation



1.3 Sensor features

Parameters	Description
Acceleration selectable full scale	±2*g*, ±4*g*, ±8*g*, ±16*g*
Gyroscope selectable full scale	±250 dps, ±500 dps, ±1000 dps, ±2000 dps
Sensitivity accuracy	±3 %
Acceleration offset	±40mg
Gyroscope offset	±2 dps
Output data rate	Up to 6.66 kHz
Bandwidth	up to 1400 Hz for acceleration up to 937 Hz for gyroscope
Operating modes	High performance, normal, low power
Current consumption	0.69 mA @ high performance mode
FIFO	4-kbyte
Communication interface	I^2C & SPI, two independent interrupt pins
Motion detection functionality	Free-fall, wake-up, tap, activity, motion, tilt and 6D orientation

Table 1: Sensor Features

1.4 Block diagram

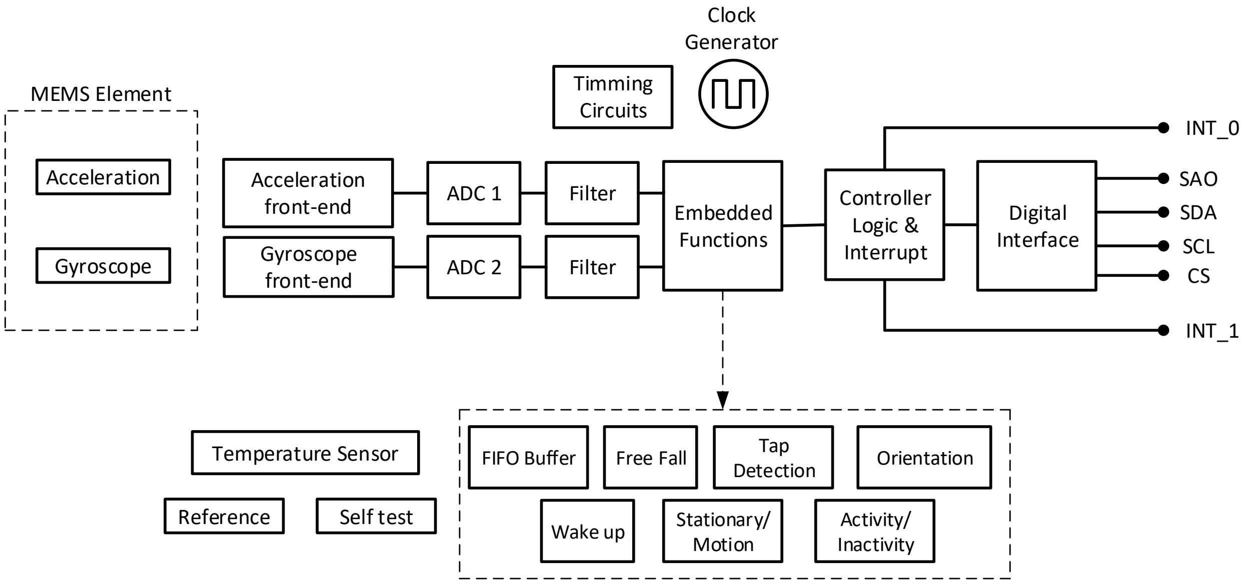


Figure 1: Block diagram

The sensor is a MEMS based capacitive sensor for acceleration and gyroscope measurement with an integrated ASIC. The acceleration MEMS element is capable of measuring both dynamic acceleration due to motion or vibration and also static acceleration due to gravity. The sensor measures the acceleration or vibration through MEMS capacitive sensing principle. The MEMS element consists of a fixed structure and movable structure. The movable structure is free to move in the direction of acceleration applied i.e. X, Y and Z direction. The force induced on the MEMS element produces change in the capacitance value that is proportional to the force exerted on it. Similarly, the gyroscope element is capable of measuring the angular velocity in degree per second (dps). The induced analog signal is converted to digital form using an analog to digital converter followed by filters and controller logic blocks. The sensor is integrated with a temperature sensor and self test functionality for both acceleration and gyroscope. The final sensor data from the output register can be accessed through an I^2C or SPI digital communication interface using a host processor.

1.5 Ordering information

WE order code	Temperature Range	Description
2536030320001	-40 °C to +85 °C	Tape & reel packaging (1000 pcs/reel)
25360303200011	-40 °C to +85 °C	Tape & reel packaging (5000 pcs/reel)

Table 2: Ordering information

2 Sensor and electrical specifications

T = 25 °C, supply voltage VDD = 3.3V, unless otherwise stated. Minimum and maximum values are based on characterization at 3σ, unless otherwise stated.

2.1 Acceleration sensor specifications

Parameters	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Measurement range	a_{RANGE}	User selectable		±2, ±4, ±8, ±16		*g*
Axis		X, Y, Z			3	
Output data rate	ODR	User selectable	1.6		6664	Hz
Resolution	RES_a			16		bits
Sensitivity accuracy [1]	SEN_{a_ACC}	T = 25 °C, a_{RANGE} = ±2g	-3		+3	%
Sensitivity change over temperature	SEN_{a_TC}	delta from T = +25 °	-0.024	±0.01	+0.024	% / °C
Noise density [2]	n_D	T = 25 °C, a_{RANGE} = ±2g, High performance mode		75	170	$\mu g/\sqrt{Hz}$
0g offset [3]	a_{OFF}	T = 25 °C	-85	±40	+85	m*g*
0g Offset change over temperature	a_{TCO}			±0.1		m*g* /°C
Nonlinearity	NL	a_{RANGE} = ±2g; Best-fit straight line		±2		%FS
Resonant frequency	f_{res_X}	X		3		kHz
	f_{res_Y}	Y		3		kHz
	f_{res_Z}	Z		2.2		kHz
Self test output change			90		1700	m*g*

Table 3: Acceleration sensor specifications

g: unit of acceleration, 1g = 9.81 m/s²
[1] *Values are after factory calibration and trimming (parts are not soldered on PCB)*
[2] *The output values are independent of the selected output data rate*

[3] *Not measured during final test after production. These are characterization values with limited number of samples*

2.2 Gyroscope sensor specifications

Parameters	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Measurement range	g_{RANGE}	User selectable		±125, ±250, ±500, ±1000, ±2000		*dps*
Axis		X, Y, Z			3	
Output data rate	ODR	User selectable	12.5		6664	Hz
Resolution	RES_g			16		bits
Sensitivity accuracy [1]	SEN_{g_ACC}	T = 25 °C, g_{RANGE} = ±125 dps	-3		+3	%
Sensitivity change over temperature	SEN_{g_TC}	delta from T = +25°	-0.048	±0.007	+0.048	% / °C
Noise density [2]	n_D	T = 25 °C, High performance mode		3.8	11	mdps /$\sqrt{Hz}$
Zero rate offset [3]	g_{OFF}	T = 25 °C		±2		dps
Zero rate Offset change over temperature	g_{TCO}			±0.015		dps /°C
Nonlinearity	NL	g_{RANGE} = ±2000dps; Best-fit straight line		±0.07		%FS
Resonant frequency	f_{res}	X,Y & Z axis		20		kHz
Self test output change		g_{RANGE} = ±250 dps	20		80	dps
		g_{RANGE} = ±2000 dps	150		700	dps

Table 4: Gyroscope sensor specifications

[1] *Values are after factory calibration and trimming (parts are not soldered on PCB)*
[2] *The output values are independent of the selected output data rate*

[3] *Not measured during final test after production. These are characterization values with limited number of samples*

2.3 Sensitivity parameter

Parameters	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Acceleration sensitivity [1]	SEN_a	a_{RANGE} = ±2g		0.061		mg /digit
		a_{RANGE} = ±4g		0.122		mg /digit
		a_{RANGE} = ±8g		0.244		mg /digit
		a_{RANGE} = ±16g		0.488		mg /digit
Gyroscope sensitivity [1]	SEN_g	g_{RANGE} = ±125dps		4.375		mdps /digit
		g_{RANGE} = ±250dps		8.75		mdps /digit
		g_{RANGE} = ±500dps		17.5		mdps /digit
		g_{RANGE} = ±1000dps		35		mdps /digit
		g_{RANGE} = ±2000dps		70		mdps /digit

Table 5: Acceleration and gyroscope sensitivity parameter

[1] *Values are after factory calibration and trimming (parts are not soldered on PCB)*

2.4 Temperature sensor specifications

Parameters	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Measurement range	T_{RANGE}		-40		+85	℃
Sensitivity	SEN_T			0.00390625		℃/digit
Resolution	RES_T			16		bits
Offset [1]	T_{OFF}		-15		+15	℃
Temperature stabilization time [2]	T_{ST}				500	µs

Table 6: Temperature sensor specification

[1] *Output of temperature sensor is 0 LSB typical at 25 ℃*
[2] *Time from power ON bit to the valid data based on characterization data ℃*

2.5 Electrical specifications

Parameters	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}		1.71	1.8	3.6	V
Operating supply voltage for I/O pins	V_{DD_IO}		1.62		3.6	V
Current consumption in high performance mode	I_{DD_HP}	ODR 6.66 kHz		694		µA
Current consumption in normal mode	I_{DD_NM}	ODR 104 Hz		376		µA
Current consumption in low power mode	I_{DD_LP}	ODR 12.5Hz		280		µA
Current consumption in power down mode	I_{DD_PD}			10		µA
Digital input voltage - high-level	V_{IH}		0.7 * V_{DD_IO}			V
Digital input voltage - low-level	V_{IL}				0.3 * V_{DD_IO}	V
Digital output voltage - high-level	V_{OH}	I_{OH} = 4 mA [1]	V_{DD_IO} - 0.2			V
Digital output voltage - low-level	V_{OL}	I_{OL} = 4 mA [1]			0.2	V

Table 7: Electrical specification

[1] *4 mA is the maximum driving capability i.e. the maximum DC current that can be sourced/-sunk by digital pin in order to guarantee correct digital output voltage levels V_{OH} and V_{OL}.*

2.6 Absolute maximum rating

Parameter	Symbol	Test conditions	Min.	Max.	Unit
Input voltage V_{DD} pin	V_{DD}		-0.3	4.8	V
Input voltage V_{DD_IO} pin	V_{DD_IO}		-0.3	4.8	V
Input voltage control pins [1]	V_{IN}		-0.3	V_{DD_IO} + 0.3	V
Acceleration	a_{MAX}	for 0.2 ms		10000	*g*

Table 8: Absolute maximum rating

[1] *SDA, SCL, CS & SAO are control pins. Input voltage on any pin should never exceed 4.8 V.*

Supply voltage on any pin should never exceed 4.8 V

2.7 General information

Parameters	Values
Operating temperature	-40 °C to +85 °C
Storage temperature	-40 °C; < 90 % RH
Communication interface	I^2C & SPI
Moisture sensitivity level (MSL)	3
Electrostatic discharge protection (HBM)	2 kV

Table 9: General information

The device is susceptible to damage by electrostatic discharge (ESD). Always use proper ESD precautions when handling. Improper handling of the device can cause performance degradation or permanent damage to the part

3 Pinning description

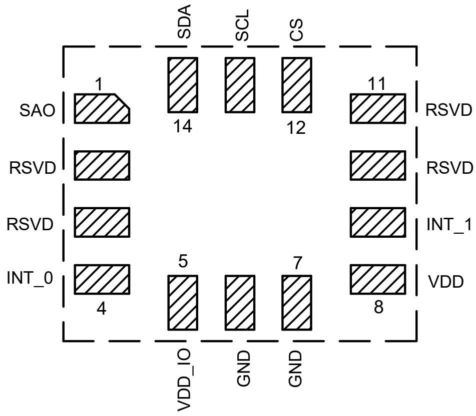


Figure 2: Pinout (top view)

No	Function	Description	Input/Output
1	*SAO*	I^2C device address selection, SPI serial data output (MISO)	Input/Output
2	*RSVD*	Connect to VDD_IO	Input
3	*RSVD*	Connect to VDD_IO	Input
4	*INT_0*	Interrupt pin 0	Output
5	*VDD_IO*	Positive supply voltage for I/O pins	Supply
6	*GND*	Negative supply voltage	Supply
7	*GND*	Negative supply voltage	Supply
8	*VDD*	Positive supply voltage	Supply
9	*INT_1*	Interrupt pin 1	Output
10	*RSVD*	Leave electrically unconnected and solder to the PCB	Input
11	*RSVD*	Connect to VDD_IO or Leave electrically unconnected and solder to the PCB	Input
12	*CS*	I^2C enable/disable, SPI chip select	Input
13	*SCL*	I^2C enable/SPI serial clock	Input
14	*SDA*	I^2C serial data, SPI serial data input (MOSI)	Input/Output

Table 10: Pin description

4 Application circuit

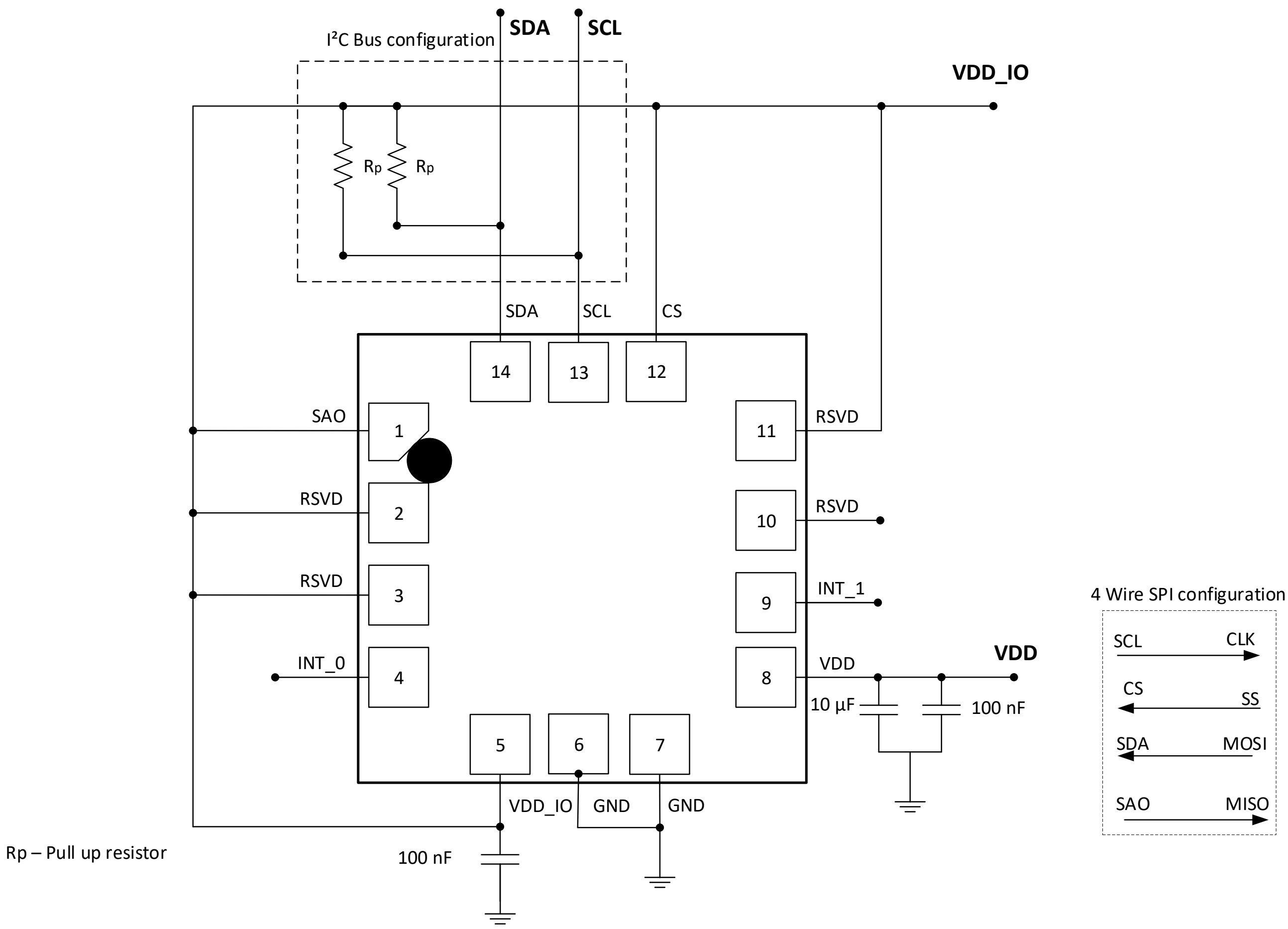


Figure 3: Electrical connection (top view)

A positive supply voltage is applied to the sensor through *VDD* pin and I/O supply voltage for digital interface through *VDD_IO*. The decoupling capacitor of 100 nF and 10µF in parallel is highly recommended and should be placed as close as possible to the *VDD* pin, but also maintain a keep out area of 2mm distance from the sensor. Communication is still possible, even if the supply voltage to the *VDD* pin is removed but maintaining the *VDD_IO*. In this case, measurement chain of the sensor is not active.

The *CS* pin shall be connected to SS (slave select) pin on the controller side to enable SPI communication interface. The *CS* pin shall be connected to *VDD_IO* in order to enable the I^2C communication interface. It is possible to have two I^2C slave addresses of the sensor by connecting *SAO* pin either to *VDD_IO* or to *GND*. In the above connection the *SAO* pin is connected to *VDD_IO*. R_p are the recommended pull up resistors for I^2C communication interface which should be connected parallel between I/O supply voltage *VDD_IO* and *SCL* and *SDA* pins.

5 Inter-Integrated Circuit (I²C)

The acceleration sensor supports standard I²C (Inter-IC) bus protocol. Further information of the I²C interface can be found at *https://www.nxp.com/docs/en/user-guide/UM10204.pdf*. I²C is a serial 8-bit protocol with two-wire interface which supports communication between different ICs. For example, between the microcontroller and other peripheral devices.

5.1 General characteristics

A serial data line (*SDA*) and a serial clock line (*SCL*) are required for the communication between the devices connected via I²C bus. Both *SDA* and *SCL* lines are bidirectional. The output stages of devices connected to the bus must have an open-drain or open-collector. Hence, the *SDA* and *SCL* lines are connected to a positive supply voltage via pull-up resistors. In I²C protocol, the communication is realized through master-slave principle. The master device generates the clock pulse, a start command and a stop command for the data transfer. Each connected device on the bus is addressable via a unique address. Master and slave can act as a transmitter or a receiver depending upon whether the data needs to be transmitted or received.

> The sensor implements the I²C role "slave"

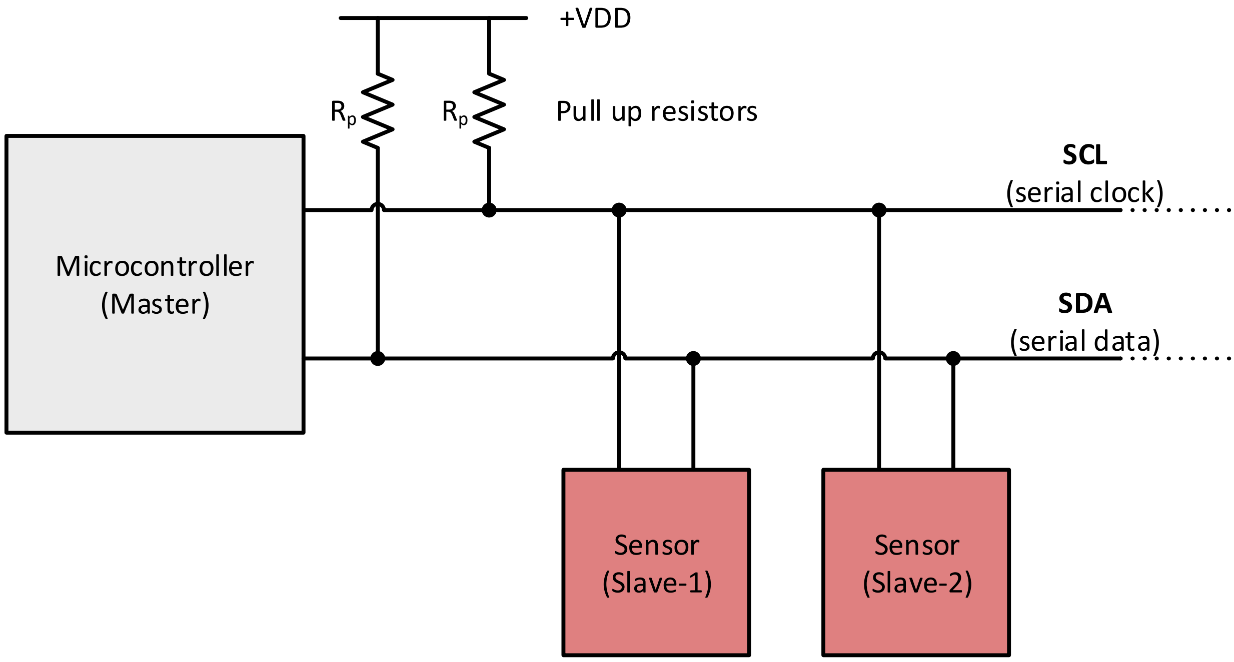


Figure 4: Master-slave concept

5.2 *SDA* and *SCL* logic levels

The positive supply voltage to which *SDA* and *SCL* lines are pulled up (through pull-up resistors), in turn determines the high level input for the slave devices. The sensor has separate supply voltage *VDD_IO* for the *SDA* and *SCL* lines. The logic high '1' and logic low '0' levels for the *SDA* and *SCL* lines then depend on the *VDD_IO*. Input reference levels for the acceleration sensor are set as 0.7 * *VDD_IO* (for logic high) and 0.3 * *VDD_IO* (for logic low). See in figure 5.

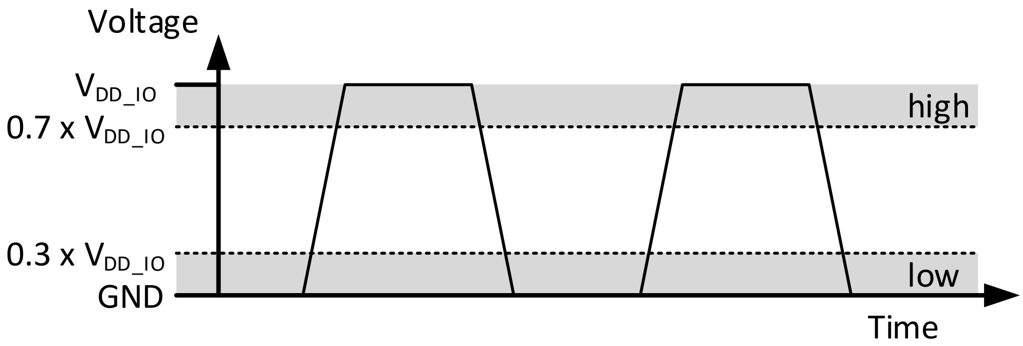


Figure 5: *SDA* and *SCL* logic levels

5.3 Communication phase

5.3.1 Idle state

During the idle state, the bus is free and both *SDA* and *SCL* lines are in logic high '1' state.

5.3.2 START(S) and STOP(P) condition

Data transfer on the bus starts with a START command, which is generated by the master. A start condition is defined as a high-to-low transition on the *SDA* line while the *SCL* line is held high. The bus is considered busy after the start condition.

Data transfer on the bus is terminated with a STOP command, which is also generated by the master. A low-to-high transition on the *SDA* line, while the *SCL* line being high is defined as a STOP condition. After the stop condition, the bus is again considered free and is in idle state. Figure 6 shows the I^2C bus START and STOP conditions.

Master can also send a REPEATED START (SR) command instead of STOP command. REPEATED START condition is same as the START condition.

5.3.3 Data validity

After the start condition, one data bit is transmitted with each clock pulse. The transmitted data is only valid when the *SDA* line data is stable (high or low) during the high period of the clock pulse. High or low state of the data line can only change when the clock pulse is in low state.

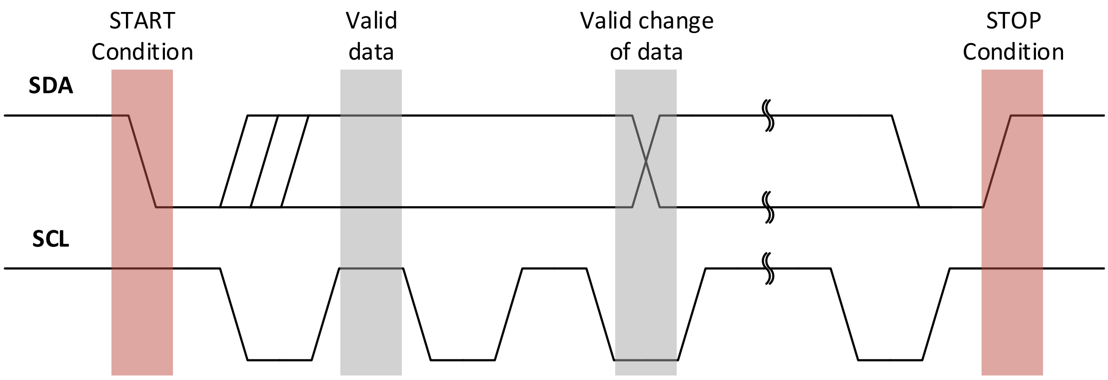


Figure 6: Data validity, START and STOP condition

5.3.4 Byte format

Data transmission on the *SDA* line is always done in bytes, with each byte being 8-bits long. Data is transmitted with the most significant bit (MSB) followed by other bits.

If the slave cannot receive or transmit another complete byte of data, it can force the master into a wait state by holding *SCL* LOW. Data transfer continues when the slave is ready which is indicated by releasing the *SCL* pin.

5.3.5 Acknowledge (ACK) and No-Acknowledge (NACK)

Each byte transmitted on the data line must follow an Acknowledge bit. The receiver (master or slave) generates an Acknowledge signal to indicate that the data byte was received successfully and ready to receive next data byte.

After one byte is transmitted, the master generates an additional Acknowledge clock pulse to continue the data transfer. The transmitter releases the *SDA* line during this clock pulse so that the receiver can pull the *SDA* line to low state in such a way that the *SDA* line remains stable low during the entire high period of the clock pulse. It is considered as an Acknowledge signal.

If the receiver does not want to receive any further byte, it will not pull down the *SDA* line and it remains in stable high state during the entire clock pulse. It is considered as a No-Acknowledge signal and the master can generate either a stop condition to terminate the data transfer or a repeated start condition to initiate a new data transfer.

5.3.6 Slave address of the sensor

The slave address is transmitted after sending the start condition. Each device on the I^2C bus has a unique address. Master selects the slave by sending corresponding slave address after the start condition. A slave address is a 7 bits long followed by a Read/Write bit.

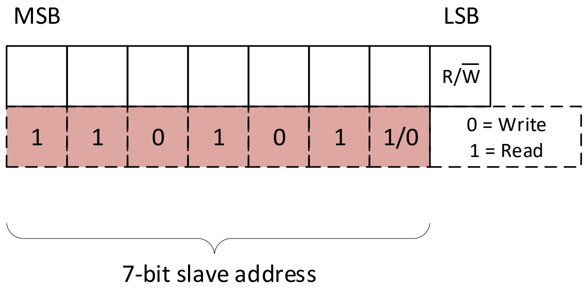


Figure 7: Slave address format

The 7-bit slave address of the acceleration sensor is 110101xb. LSB of the 7-bit slave address can be modified with the *SAO* pin. If *SAO* is connected to positive supply voltage i.e. LSB is '1', making 7-bit slave address 1101011b (0x6B). If *SAO* is connected to ground i.e. LSB is '0', making 7-bit address 1101010b (0x6A).

The R/W bit determines the data direction. A '0' indicates a write operation (transmission from master to slave) and a '1' indicates a read operation (data request from slave).

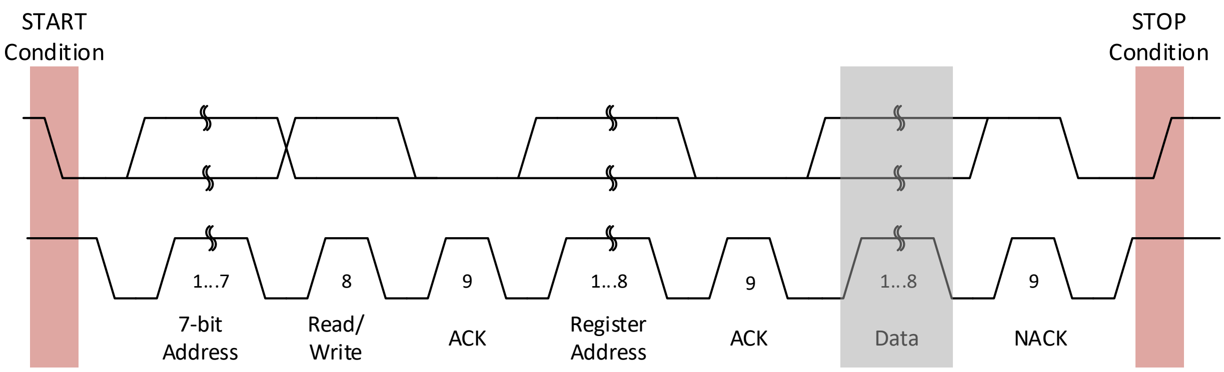


Figure 8: Complete data transfer

7-bit slave address of the IMU sensor is 110101xb. LSB of the 7-bit slave address depends on the *SAO* pin connection

Slave address[6:1]	Slave address[0]	7-bit slave address	R/W	Slave address + R/W
110101	SAO = 0	1101010 (0x6A)	0	11010100 (0xD4)
110101			1	11010101 (0xD5)
110101	SAO = 1	1101011 (0x6B)	0	11010110 (0xD6)
110101			1	11010111 (0xD7)

Table 11: Slave address and Read/Write commands

5.3.7 Read/Write operation

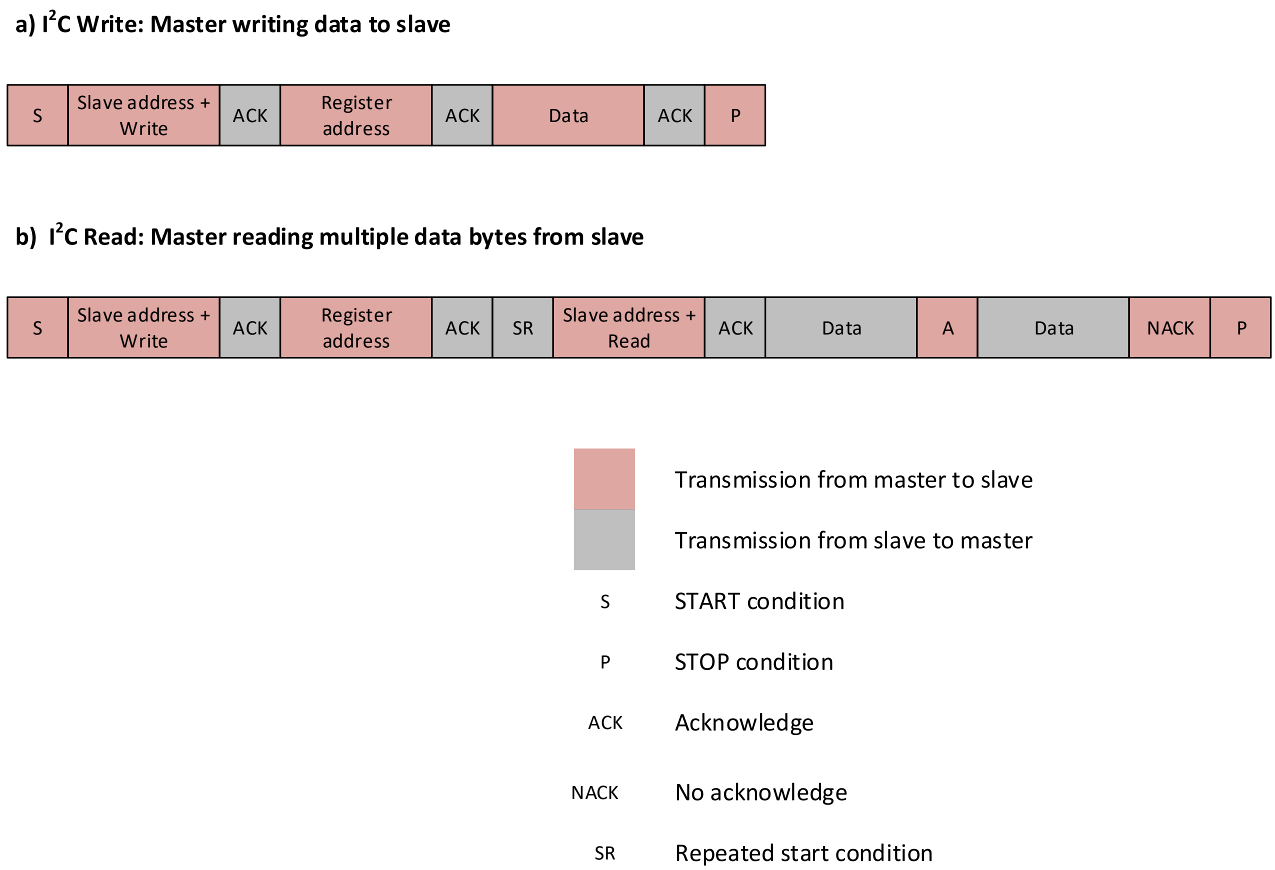


Figure 9: Write and read operations of the sensor

Once the slave-address and data direction bit is transmitted, the slave acknowledges the master. The next byte is transmitted by the master, which must be a register-address of the sensor. It indicates the address of the register where data needs to be written to or read from.

After receiving the register address, the slave sends an Acknowledgment (ACK). If the master is still writing to the slave (R/W bit = 0), it will transmit the data to slave in the same direction. If the master wants to read from the addressed register (R/W bit =1), a repeated start (SR) condition must be transmitted to the slave. Master acknowledges the slave after receiving each data byte. If the master no longer wants to receive further data from the slave, it would send No-Acknowledge (NACK). Afterwards, master can send a STOP condition to terminate the data transfer. Figure 9 shows the writing and reading procedures between the master and the slave device (sensor).

5.4 I^2C timing parameters

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
LOW period for *SCL* clock	t_{LOW_SCL}	4.7		1.3		µs
HIGH period for *SCL* clock	t_{HIGH_SCL}	4.0		0.6		µs
Hold time for START condition	t_{HD_S}	4		0.6		µs
Setup time for (repeated) START condition	f_{SCL}	4.7		0.6	400	µs
SDA setup time	t_{SU_SDA}	250		100		ns
SDA data hold time	t_{HD_SDA}	0	3.45	0	0.9	µs
Setup time for STOP condition	t_{SU_P}	4		0.6		µs
Bus free time between STOP and START condition	t_{BUF}	4.7		1.3		µs

Table 12: I^2C timing parameters

6 Serial Peripheral Interface (SPI)

Serial Peripheral Interface (SPI) is a synchronous serial communication bus system for the communication between host microcontroller and other peripheral ICs such as ADCs, EEP-ROMs, sensors, etc. SPI is a full-duplex master-slave based interface allowing the communication to happen in both directions simultaneously. The data from the master or the slave is synchronized either on the rising or falling edge of clock pulse. SPI can be either 4-wire or 3-wire interface. 4-wire interface consists of two signal lines and two data lines. All of these bus lines are unidirectional.

1. Clock (SCL)
2. Chip select (CS)
3. Master out, slave in (MOSI)
4. Master in, slave out (MISO)

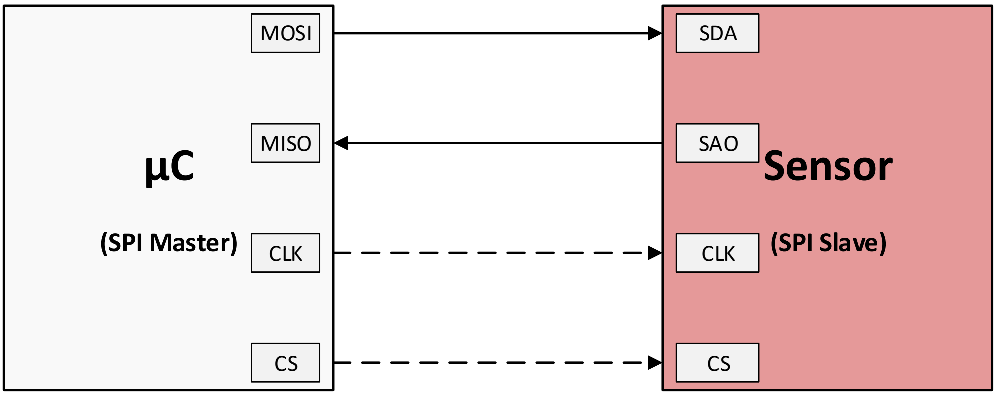


Figure 10: SPI Interface

Master generates the clock signal and is connected to all slave devices. Data transmission between the master and salves is synchronized to the clock signal generated by the master.

One master can be connected to one or more slave devices. Each slave device is addressed and controlled by the master via individual chip select (CS) signals. CS is controlled by the master and is normally an active low signal.

MOSI and MISO are data lines. MOSI transmits data from the master to the slave. MISO transmits data from the slave to the master.

The IMU sensor supports 4-wire SPI communication protocol

6.1 Data transfer

Communication begins when the master selects a slave device by pulling the *CS* line to LOW. The clock and data lines (MOSI/MISO) are available for the selected slave device. Data stored in the specific shift registers are exchanged synchronously between master and the slave through MISO and MOSI lines. The data transmission is over when the chip select line is pulled up to the HIGH state. 4-wire SPI uses both data lines for the synchronous data exchange in both the direction.

6.2 Communication modes

In SPI, the master can select the clock polarity (CPOL) and clock phase (CPHA). The CPOL bit sets the polarity of the clock signal during the idle state. The CPHA bit selects the clock phase. Depending on the CPHA bit, the rising or falling clock edge is used to sample and shift the data. Depending on the CPOL and CPHA bit selection in the SPI control registers, four SPI modes are available as per table 13. In order to ensure proper communication, master and the slave must be set to same communication modes.

CPOL	CPHA	Description
0	0	Clock polarity LOW in idle state; Data sampled on the rising clock edge
0	1	Clock polarity LOW in idle state; Data sampled on the falling clock edge
1	1	Clock polarity HIGH in idle state; Data sampled on the falling clock edge
1	0	Clock polarity HIGH in idle state; Data sampled on the rising clock edge

Table 13: SPI communication modes

6.3 Sensor SPI Communication

4-Wire SPI of this sensor uses following lines: *SDA* (data input, MOSI),*SAO* (data output, MISO), *SCL* (serial clock) and *CS* (chip select). For more information, please refer to pin description in the section 3.

CS is pulled LOW by the master at the start of communication. The *SCL* polarity is HIGH in the idle state (CPOL = 1). The data lines (*SDA* & *SAO*) are sampled at the falling clock edge and latched at the rising clock edge (CPHA = 1). Data is transmitted with MSB first and the LSB last.

SPI read and write operations are completed in 2 or more bytes (multiple of 16 or more clock pulses). Each block consists of a register address byte and a data byte. The first byte is the register address. In the SPI communication, the register address is specified in the 7-bits and the MSB of the register address is used as an SPI read/write bit (Figure 11). When R/W is '0', the data is written on to the sensor. When '1', the data is read from the sensor.

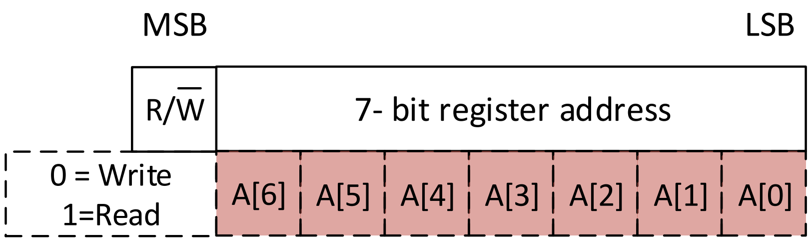


Figure 11: SPI register address

The next bytes of data, depending on the R/W bit, is either written to or read from the indexed register. Figure 12 shows the complete SPI data transfer protocol.

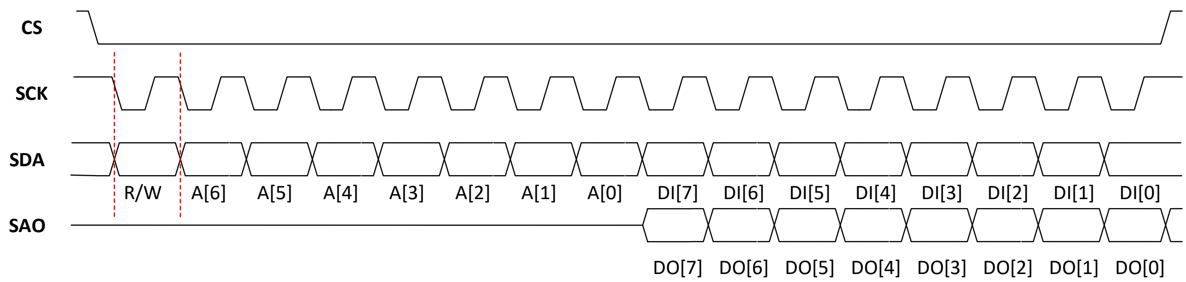


Figure 12: 4-wire SPI data transfer (CPOL = 1, CPHA = 1)

6.3.1 SPI write operation

The write operation starts with the *CS* = LOW and sending the 7-bit register address with R/W bit = '0' (write command). Next byte is the data byte that is the data to be written to the indexed register. Several write command pairs can be sent without raising the *CS* back to HIGH. The operation is ended with *CS* = HIGH. The SPI write protocol is shown in the figure 13.

Start	R/$\overline{W}$	Register address							Data to be written								Stop
CS = LOW	**0**	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	DI [7]	DI [6]	DI [5]	DI [4]	DI [3]	DI [2]	DI [1]	DI [0]	CS = HIGH

Figure 13: SPI write protocol

6.3.2 SPI read operation

The read operation starts with the *CS* = LOW and sending the 7-bit register address with R/W bit = '1' (read command). Data is sent out from the sensor through the *SAO* line. The SPI read protocol is shown in the figure 14.

Start	R/$\overline{W}$	Register address							Data from indexed register								Stop
CS = LOW	**1**	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	DI [7]	DI [6]	DI [5]	DI [4]	DI [3]	DI [2]	DI [1]	DI [0]	CS = HIGH

Figure 14: SPI read protocol

During multiple read/write operation, the register address is automatically incremented after each block. This feature is enabled by default with the bit IF_ADD_INC set to '1' in the *CTRL_2* register.

6.3.3 SPI timing parameters

Table 14 shows general SPI timing parameters. They are subject to VDD and the operating temperature.

Parameter	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}		10 [1]	MHz
SPI clock cycle	t_{SCL}	100		ns
CS setup time	t_{SU_CS}	6		ns
CS hold time	t_{h_CS}	6		ns
SDA input setup time	t_{SU_SDA}	5		ns
SDA input hold time	t_{h_SDA}	15		ns
SAO valid output time	t_{v_SAO}		50	ns
SAO output hold time	t_{h_SAO}	9		ns
SAO output disable time	t_{dis_SAO}		50	ns

Table 14: SPI timing parameters

1. *Recommended maximum SPI clock frequency for ODR $\leq$ 50 Hz is 8 MHz*

7 Sensor specific parameters

7.1 Acceleration Sensitivity

Sensitivity is defined as the ratio of change in input to the change in the output signal. The unit of sensitivity is typically expressed in m*g*/digit for acceleration sensor. Acceleration sensitivity can be measured by pointing the sensor horizontally downwards, an acceleration of 1*g* is measured due to earth's gravity (9.807 m/s^2). Similarly by pointing sensor horizontally upwards (rotation of 180 degree), again an acceleration of 1*g* is measured due to earth's gravity (9.807 m/s^2). By subtracting the larger measured output value from the smaller measured output value and dividing by two gives the actual sensitivity of the acceleration sensor.

$$\text{Sensitivity} = \frac{\text{larger value - smaller value}}{2} \tag{1}$$

7.2 Gyroscope Sensitivity

An angular rate gyroscope produces a positive digital output for counterclockwise rotation around the axis and negative digital output for clockwise rotation around the axis considered. The unit of sensitivity is typically expressed in mdps/digit (milli degree per second/digit) for gyroscope sensor. The sensitivity of the gyroscope sensor is defined by the gain of the sensor which can be determined by applying a known angular velocity.

> **!** The sensitivity value will drift over time and temperature

7.3 0 *g* Level offset

0 *g* level is the output level when there is no acceleration or motion acting on the sensor i.e. zero input. A sensor placed on a perfect horizontal plane will give 0 *g* output on X-axis and Y-axis but 1 *g* on Z-axis. The deviation of an actual output value from the ideal value gives the 0 *g* level offset. 0 *g* offset value is influenced by external parameters like temperature and stress. External stress on the sensor will affect the sensor performance significantly. The 0 *g* level offset will also drift over temperature.

> **!** External stress: Vias under the sensor on a PCB, PCB warpage, external mechanical stress to the sensor

7.4 Zero rate Level offset

Zero rate level is the actual output signal when there is no angular rate acting on the sensor. i.e. zero input. Similarly as acceleration sensor, the gyroscope sensor zero rate output is influenced by external parameter like temperature and also stress after mounting onto a printed circuit board.

7.5 Noise density

Noise density of the sensor is expressed as $\mu g/\sqrt{Hz}$ for acceleration sensor and $mdps/\sqrt{Hz}$ for gyroscope sensor. Noise density of the sensor is dependent on the output data rate. The values are expressed in the chapter 9. The noise of the sensor is determined by the equivalent noise bandwidth of the output filter and coefficient of the filter order. In general, the noise density of the sensor is determined by the following equation:

$$\text{Noise density\_Acc} = \frac{\text{rms noise of acceleration sensor}}{\sqrt{\text{Bandwidth * filter coefficient}}} \qquad [\mu g/\sqrt{\text{Hz}}] \tag{2}$$

$$\text{Noise density\_Gyr} = \frac{\text{rms noise of gyroscope sensor}}{\sqrt{\text{Bandwidth * filter coefficient}}} \qquad [mdps/\sqrt{\text{Hz}}] \tag{3}$$

8 Quick start guide

This chapter describes the start up sequence of the acceleration sensor.

8.1 Power supply

The sensor has two individual supply voltage pins.

- *VDD* is main supply voltage
- *VDD_IO* is the I/O pin supply voltage for the digital I^2C or SPI communication interface

It should be noted that *VDD* level should never be lower than *VDD_IO* i.e. proper power up should be *VDD* > *VDD_IO*. It is possible to remove *VDD* by keeping *VDD_IO* pin without communication interruption but the measurement chain of the sensor is turned off i.e. *VDD* = 0 with *VDD_IO* "high" is allowed. In this case, the measurement chain is turned off but the communication to the sensor is possible without interruption.

Power up sequence should be *VDD* > *VDD_IO*

8.2 Boot status

By proper powering up of the sensor with correct voltage level to the respective pins, the sensor enters into a 20 ms boot sequence to load the trimming parameters. After completion of the boot up sequence the sensor automatically enters to power down mode.

It is also possible to initiate the boot sequence manually by the user. It is performed by setting the BOOT bit of the *CTRL3_C* register to '1', then the boot sequence is initiated and trimming parameters are reloaded. In this case, the device operation mode does not change after boot procedure. No toggle of the power is required and the content of the device control registers is not modified.

The registers are not accessible during the 20 ms boot sequence

The boot status signal is identified by setting the INT0_BOOT bit of the *INT0_CTRL* register to '1'. When the sensor is in boot sequence, INT_0 interrupt pin is driven high. Similarly when the boot sequence is completed, INT_0 interrupt pin is driven low.

8.2.1 Soft reset

If required, the soft reset of the sensor is possible. It resets the default value of the control registers. The soft reset procedure will take 5 µs.

The below steps should be considered for setting the BOOT bit manually:
1. Write SOFT_RESET bit to '1'
2. Wait for 5 µs
3. Write BOOT bit to '1'
4. Wait for 20 ms

Parameter	Time
Boot sequence	20 ms
Soft reset duration	5 µs

Table 15: Time consumption

8.3 Flow chart

8.3.1 Communication check

After proper powering of the sensor, the first step is to check the communication of the sensor with an I²C or SPI communication interface. It can be verified by reading the value of *Device_ID* register(0x0F). If the value from the *Device_ID* register(0x0F) is 0x6A, then the communication to the sensor is successful.

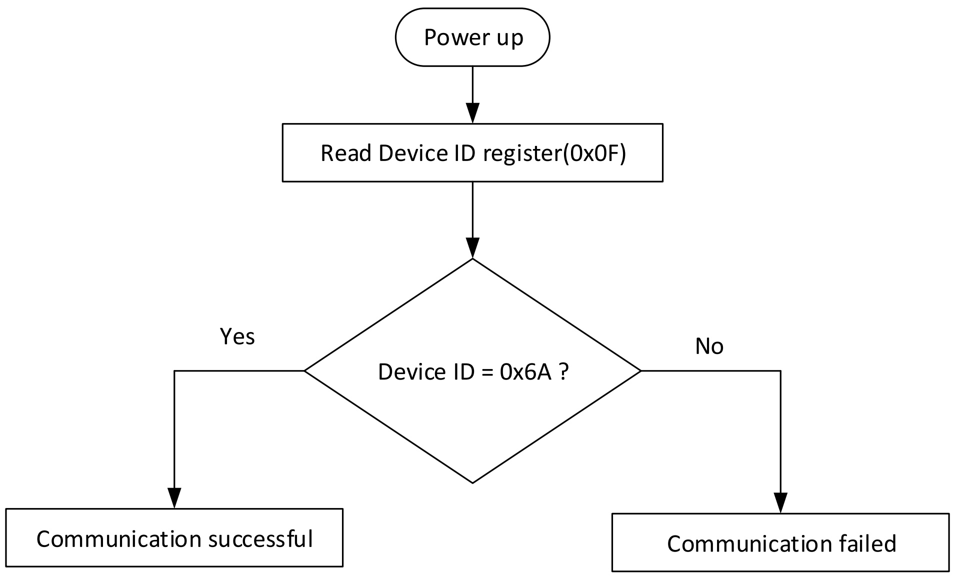


Figure 15: Communication check

8.3.2 Sensor in operation with high performance mode

The following flow chart is an initialization example to operate the sensor in high performance mode with output data rate of 208 Hz.

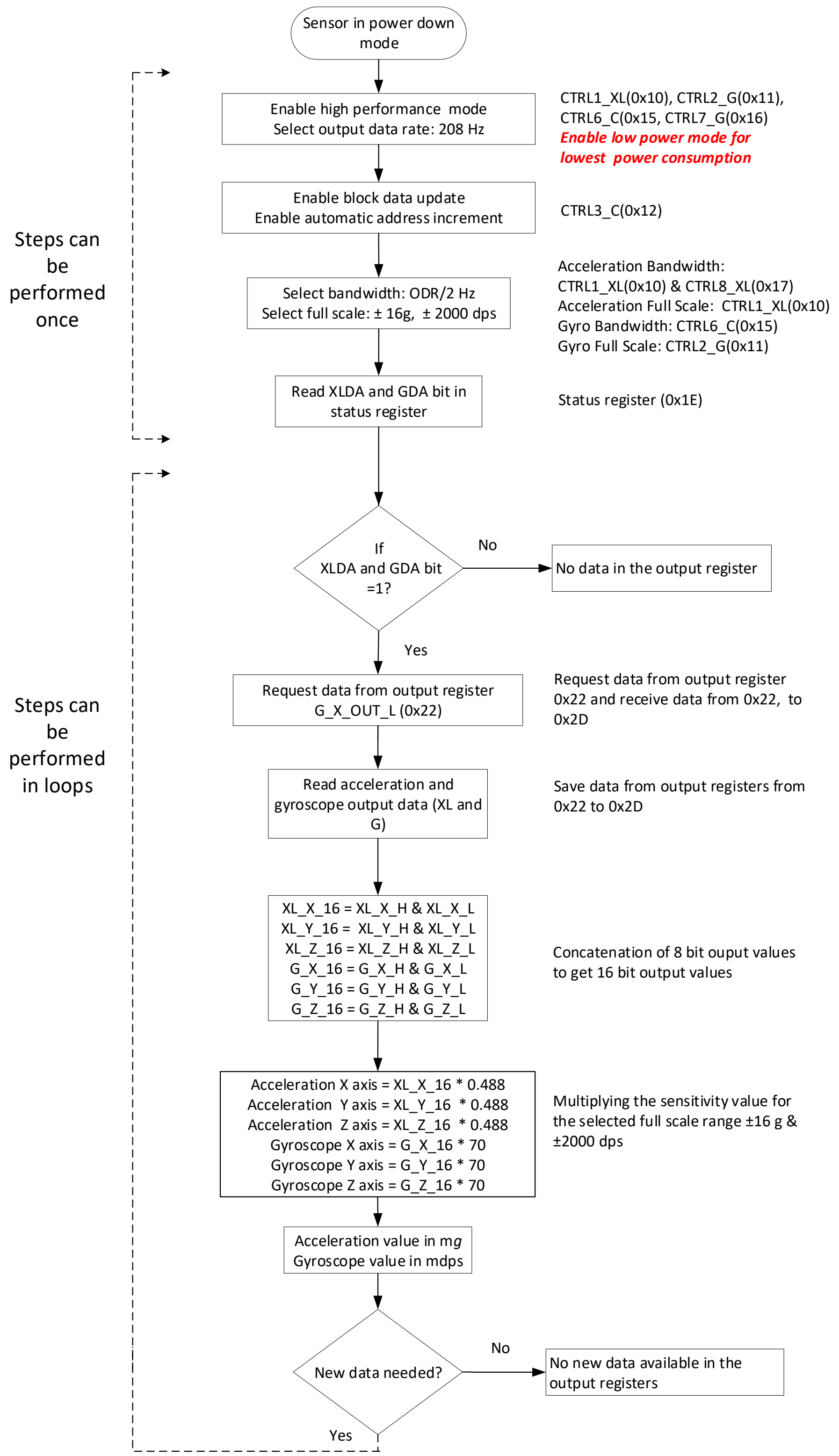


Figure 16: Sensor in operation with high performance mode

In order to set the sensor in one of the operation modes, the sensor needs to be initialized. The initialization of the sensor can be performed by defining output data rate, full scale setting and filtering path. After initializing the sensor, it is recommended to check if the data samples are available in the output registers. It can be verified by reading GDA and XLDA bit in *STATUS_REG* register(0x1E). If the GDA and XLDA bit is enabled, the output data from acceleration and gyroscope sensor of three axes from 0x22 to 0x2D registers are available. The acceleration and angular velocity values of the sensors are obtained by multiplying output data with respective sensitivity parameter value based on the selected full scale range. Sensitivity parameter values for different full scale ranges are mentioned in the table 5.

9 Operating modes

The sensor can be operated in three different operation modes which provides different combination of noise and current consumption values. These operating modes are selected by using the ODR_XL[3:0] bits in the *CTRL1_XL* register(0x10) and ODR_G[3:0] bits in the *CTRL2_G* register(0x11).

- High performance mode
- Normal mode
- Low power mode

The acceleration and the gyroscope sensor can be turned on/off independently of each other and are capable to operate with different ODRs and power modes. The three operating modes are available

- Acceleration sensor active and gyroscope power down
- Gyroscope sensor active and acceleration power down
- Both acceleration and gyroscope sensor active with independent ODRs

9.1 Gyroscope power modes

By default after power up, the sensor is in power down mode. The gyroscope sensor can be configured in four different operating modes:

- Power down
- Low power
- Normal mode
- High performance mode

The operating modes can be selected using the G_HM_MODE bit in *CTRL7_G* (0x16). If G_HM_MODE is set to ’0’, high performance mode is valid for all ODRs (from 12.5 Hz up to 6.66 kHz). To enable the low power and normal mode, the G_HM_MODE bit has to be set to ’1’. Low power mode is available for lower ODRs (12.5, 26, 52 Hz) while normal mode is available for ODRs equal to 104 and 208 Hz.

9.2 Acceleration power modes

By default after power up, the sensor is in power down mode. The acceleration sensor can be configured in four different operating modes:

- Power down
- Low power
- Normal mode
- High performance mode

The operating mode can be selected using the XL_HM_MODE bit in *CTRL6_C* (0x15). If XL_HM_MODE is set to '0', high performance mode is valid for all ODRs (from 12.5 Hz up to 6.66 kHz).To enable the low power and normal mode, the XL_HM_MODE bit has to be set to '1'. Low power mode is available for lower ODRs (1.6, 12.5, 26, 52 Hz) while normal mode is available for ODRs equal to 104 and 208 Hz.

10 Application specific sensor features

10.1 Single tap/Double tap

The single tap event interrupt is generated when the applied tap acceleration to any axis is greater than defined threshold and returns below within specific interval time. Similarly in double tap event an interrupt is generated, if two consecutive tap acceleration applied to any axis is greater than the threshold with duration time after first tap acceleration.

10.2 Activity/Inactivity

The activity/inactivity function monitors the sensor, which defines whether the sensor is active or not. This function allows developing application with low power consumption. If the sensor is not active, the output data rate automatically goes to output data rate of 12.5 Hz with low power operating mode. As soon as the sensor detects an activity, the output data rate is switched back to the selected output data rate.

10.3 Stationary/Motion

Stationary/motion function is similar to the activity/inactivity function but the output data rate and operating mode will not change after the motion is detected.

10.4 6D Orientation

Six dimension (6D) orientation of the sensor is detected when one axis exceeds a selected threshold and the acceleration values from other two axes are lower than the defined threshold value.

10.5 Wake-Up

If a number of data samples exceed the defined threshold on both positive and negative acceleration a wake-up interrupt signal is generated. It can either be achieved by setting high-pass filter or user defined offset function.

10.6 Free-Fall

Free fall detection interrupt is generated when the device is in free-fall i.e. the acceleration measured in all axes goes to zero. In a real case, a free-fall zone is defined around the zero-g level where all the acceleration values from the three axes are small enough to generate the interrupt.

10.7 Tilt detection

The tilt detection function helps to identify the change in the activity/angle of the sensor. This feature is implemented in the hardware only using the acceleration sensor. The tilt detection is based on the trigger of an event each time when the sensor is tilted. It can be easily configured using the programmable average window and average threshold parameters.

10.8 FIFO

The integrated FIFO buffer allows consistent power saving operation for the system since the host processor does not need continuously data logging from the sensor. But it can wake up only when needed and burst the significant data out from the FIFO. The sensor embeds 4 kbytes data FIFO to store the following data:

- Gyroscope sensor output data
- Acceleration sensor output data
- Temperature output data

11 Self test

The sensor includes a self test feature which tests the both acceleration and gyroscope sensor functionality without any external force. When the self test feature is enabled, an actuation force is applied to the sensor which causes the non-stationary part to move. This change in the movement provides the change in the DC level of the sensor.

The self test function is enabled by writing '01' to ST_G[1:0] and ST_XL[1:0] in *CTRL5_C* (0x14) register which causes movement in positive direction of the axis for both acceleration and gyroscope sensor. Similarly by writing '10' to ST_G[1:0] and ST_XL[1:0] in *CTRL5_C* (0x14) register causes the movement in negative direction of the axis for both acceleration and gyroscope sensor. When the sensor self test functionality is enabled, the output level is given by the algebraic sum of the data produced by the electrostatic test force and gravity.

> **!** The device should be fixed without any movement during self test procedure

The following procedure is recommended for the self test verification. Refer to the block diagram in the figure 17 for acceleration sensor self test procedure and figure 18 for gyroscope sensor self test procedure.

- Average five data samples before enabling the self test without moving the sensor
- Average five data samples after enabling the self test without moving the sensor
- The difference in the absolute value of each axis provides the self test induced DC acceleration value.
- Verify the value, whether it is in the range of 70 m*g* to 1500 m*g* for acceleration and 150 dps to 700 dps for gyroscope sensor

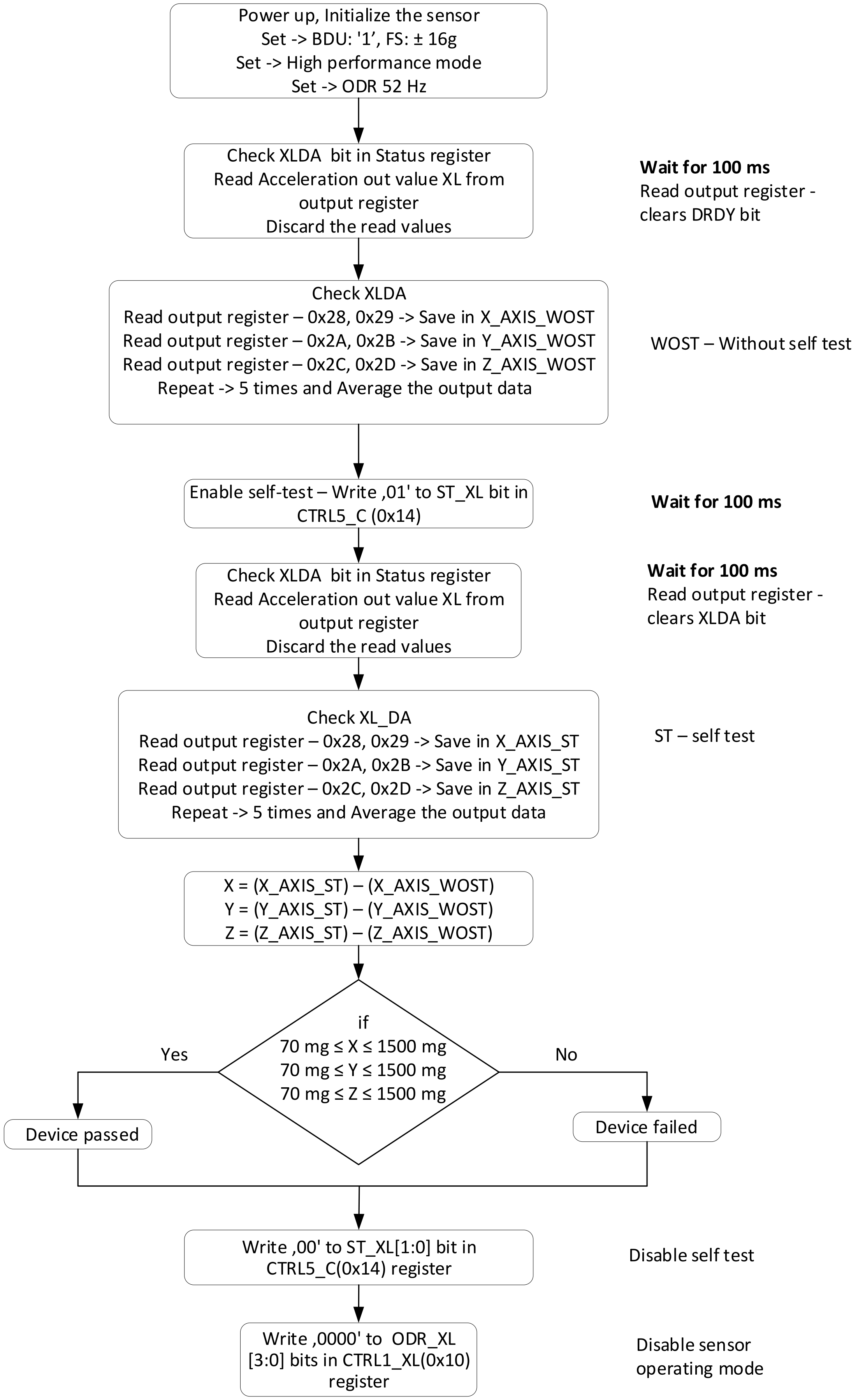


Figure 17: Self test procedure for acceleration sensor

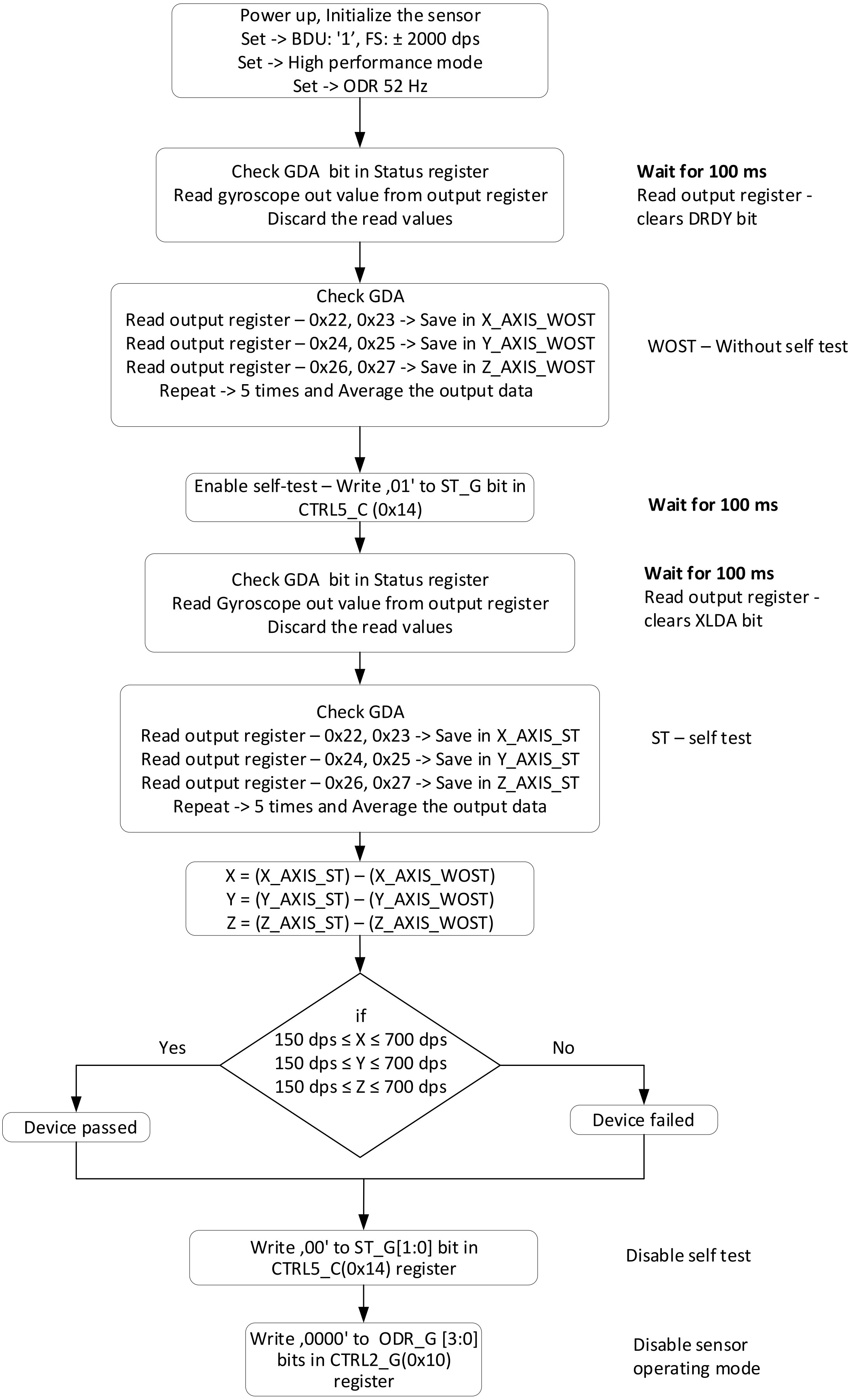


Figure 18: Self test procedure for gyroscope sensor

12 Sensor output data

12.1 Output values from the register

The acceleration output data is obtained by reading output registers from (0x28) to (0x2D) and similarly for gyroscope output data from the registers (0x22) to (0x27). The 8-bit output data from the registers of least significant bit and most significant bit are concatenated to get 16-bit data for each axis i.e. X, Y and Z axis. The values from the output register are represented as 16-bit values, left aligned and provided in two's complement. The value is multiplied with respective sensitivity parameter to convert the data related to the value in mg for acceleration and mdps (milli degree per second) for gyroscope .

12.2 Acceleration sensor

Below is an example of how to convert the output data into acceleration value in mg. With an assumption of sensor operating in high performance mode with full scale selection of ±16g.

Step 1:

Read the output registers.

1. XL_X_OUT_L (0x28)
2. XL_X_OUT_H (0x29)
3. XL_Y_OUT_L (0x2A)
4. XL_Y_OUT_H (0x2B)
5. XL_Z_OUT_L (0x2C)
6. XL_Z_OUT_H (0x2D)

Step 2:

Concatenation of two 8-bit output values from the registers to get a signed 16-bit output value for each axis.

1. X_16 $=$ (XL_X_OUT_H $\ll 8)$ | XL_X_OUT_L
2. Y_16 $=$ (XL_Y_OUT_H $\ll 8)$ | XL_Y_OUT_L
3. Z_16 $=$ (XL_Z_OUT_H $\ll 8)$ | XL_Z_OUT_L

Step 3:

Multiply with respective sensitivity will provide the acceleration value in mg.
(Sensitivity = 0.488 m*g* /digit for FS: ±16*g*, please refer to table 5)

1. X axis = X_16 * (0.488) = value in m*g*
2. Y axis = Y_16 * (0.488) = value in m*g*
3. Z axis = Z_16 * (0.488) = value in m*g*

12.3 Gyroscope sensor

Below is an example of how to convert the output data into gyroscope value in mdps (milli degree per second). With an assumption of sensor operating in high performance mode with full scale selection of ±2000 dps.

Step 1:

Read the output registers.

1. G_X_OUT_L (0x22)
2. G_X_OUT_H (0x23)
3. G_Y_OUT_L (0x24)
4. G_Y_OUT_H (0x25)
5. G_Z_OUT_L (0x26)
6. G_Z_OUT_H (0x27)

Step 2:

Concatenation of two 8-bit output values from the registers to get a signed 16-bit output value for each axis.

1. P_16 $=$ (XL_X_OUT_H $\ll 8$) | XL_X_OUT_L
2. R_16 $=$ (XL_Y_OUT_H $\ll 8$) | XL_Y_OUT_L
3. Y_16 $=$ (XL_Z_OUT_H $\ll 8$) | XL_Z_OUT_L

Step 3:

Multiply with respective sensitivity will provide the gyroscope value in mdps.
(Sensitivity = 70 mdps /digit for FS: ±2000 dps, please refer to table 5)

1. Pitch = P_16 * 70 = value in mdps
2. Roll = R_16 * 70 = value in mdps
3. Yaw = Y_16 * 70 = value in mdps

12.4 Temperature sensor

The IMU sensor includes embedded temperature sensor for ambient temperature measurement. The temperature data is represented as a 16 bit in two's complement form and left aligned in the output registers *T_OUT_L* (0x20) and *T_OUT_H* (0x21) with a sensitivity of 256 LSB/℃. The output zero level corresponds to 25 ℃.
If both the acceleration and the gyroscope sensors are in power down mode, the temperature sensor is off. The maximum output data rate of the temperature sensor is 52 Hz and its value depends on how the acceleration and gyroscope sensors are configured. If the gyroscope is in power down mode:

- The temperature data rate is equal to 12.5 Hz if the acceleration sensor ODR is equal to 12.5 Hz low power mode
- The temperature data rate is equal to 26 Hz if the acceleration sensor configuration is 26 Hz low power mode
- The temperature data rate is equal to 52 Hz for all other acceleration sensor configurations.

If both the acceleration and the gyroscope sensors are in power down mode, the temperature sensor is off

If the gyroscope is not in power down mode, the temperature data rate is equal to 52 Hz, regardless of the acceleration and gyroscope sensor configuration. table 16 and table 17 provides a few basic examples of the data that is read from the temperature data registers at different ambient temperature values. The values listed in this table are given under the hypothesis of perfect device calibration (i.e. no offset, no gain error).

Temperature values (if BLE (big/little endian) bit = 0)	T_OUT_H (0x21)	T_OUT_L (0x20)
0 ℃	0xE7	0x00
25 ℃	0x00	0x00
50 ℃	0x19	0x00

Table 16: Temperature output data BLE bit = 0

Temperature values (if BLE (big/little endian) bit = 1)	T_OUT_H (0x21)	T_OUT_L (0x20)
0 ℃	0x00	0xE7
25 ℃	0x00	0x00
50 ℃	0x00	0x19

Table 17: Temperature output data BLE = 1

We recommend our WSEN-TIDS temperature sensor part no: 2521020222501 for high accurate and precise temperature measurement applications

13 Register mapping

Register Addr (Hex)	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Comments
0x00-05	Reserved[1]	-								-	Reserved
0x06	*FIFO_CTRL1*	FTH_[7:0]								R/W	FIFO configuration register
0x07	*FIFO_CTRL2*	FIFO_TIMER_EN	0[2]			FIFO_TEMP_EN	FTH_[10:8]			R/W	
0x08	*FIFO_CTRL3*	0[2]		DEC_FIFO_GYRO[2:0]			DEC_FIFO_XL[2:0]			R/W	
0x09	*FIFO_CTRL4*	ON_FTH	HIGH_DATA	DEC_DS4_FIFO[2:0]			DEC_DS3_FIFO[2:0]			R/W	
0x0A	*FIFO_CTRL5*	0[2]	ODR_FIFO_[3:0]				FIFO_MODE_0[2:0]			R/W	
0x0B	*DRDY_PULSE_CFG*	DRDY_PULSED	0[2]							R/W	
0x0C	Reserved[1]	-								-	Reserved
0x0D	INT0_CTRL	0[2]		INT0_FIFO_FLAG	INT0_FIFO_OVR	INT0_FTH	INT0_BOOT	INT0_DRDY_G	INT0_DRDY_XL	R/W	INT0 pin control
0x0E	INT1_CTRL	0[2]		INT1_FIFO_FLAG	INT1_FIFO_OVR	INT1_FTH	INT0_DRDY_TEMP	INT1_DRDY_G	INT1_DRDY_XL	R/W	INT1 pin control
0x0F	*DEVICE_ID*	0	1	1	0	1	0	1	0	R	Device address
0x10	*CTRL1_XL*	ODR_XL[3:0]				FS_XL[1:0]		LPF1_BW_SEL	BW0_XL	R/W	Acceleration and gyroscope register
0x11	*CTRL2_G*	ODR_G[3:0]				FS_G[1:0]		FS_125	0[2]	R/W	
0x12	*CTRL3_C*	BOOT	BDU	H_LACTIVE	PP_OD	SIM	IF_INC	BLE	SW_RESET	R/W	
0x13	*CTRL4_C*	DEN_XL_EN	SLEEP	INT1_ON_INT0	DEN_DRDY_INT0	DRDY_MASK	I2C_DISABLE	LPF1_SEL_G	0[2]	R/W	
0x14	*CTRL5_C*	ROUNDING[2:0]			DEN_LH	ST_G[1:0]		ST_XL[1:0]		R/W	
0x15	*CTRL6_C*	TRIG_EN	LVL1_EN	LVL2_EN	XL_HM_MODE	USR_OFF_W	0[2]	FTYPE[1:0]		R/W	
0x16	*CTRL7_G*	G_HM_MODE	HP_EN_G	HPM_G[1:0]		0[2]	ROUNDING_STATUS	0[2]	0[2]	R/W	
0x17	*CTRL8_XL*	LPF2_XL_EN	HPCF_XL_1[1:0]		HP_REF_MODE	IN_COM	HP_SL_XL_EN	0[2]	LOW_PASS_ON_6D	R/W	
0x18	*CTRL9_XL*	DEN_X	DEN_Y	DEN_Z	DEN_XL_G	0[2]	0	0[2]	0[2]	R/W	
0x19	*CTRL10_C*	0[2]	0[2]	0	0[2]	TILT_EN	FUNC_EN	0[2]	0[2]	R/W	
0x1A	*MASTER_CONFIG*	DRDY_ON_INT1	DATA_VALID_SEL_FIFO	0[2]	START_CONFIG	PULL_UP_EN	PASS_THROUGH_MODE	0	MASTER_ON	R/W	I^{2}C master configuration register
0x1B	*WAKE_UP_SRC*	0	0	FF_IA	SLEEP_STATE_IA	WW_IA	X_WU	Y_WU	Z_WU	R	Interrupt register
0x1C	*TAP_SRC*	0	TAP_IA	SINGLE_TAP	DOUBLE_TAP	TAP_SIGN	X_TAP	Y_TAP	Z_TAP	R	
0x1D	*D6D_SRC*	DEN_DRDY	D6D_IA	ZH	ZL	YH	YL	ZH	ZL	R	
0x1E	*STATUS_REG*	0	0	0	0	0	TDA	GDA	XLDA	R	Status data register for GP and OIS data
0x1F	Reserved[1]	-								-	Reserved
0x20	*T_OUT_L*	TEMP[7:0]								R	Temperature data registers
0x21	*T_OUT_H*	TEMP[15:8]								R	
0x22	*G_X_OUT_L*	G_X[7:0]								R	Gyroscope data registers
0x23	*G_X_OUT_H*	G_X[15:8]								R	
0x24	*G_Y_OUT_L*	G_Y[7:0]								R	
0x25	*G_Y_OUT_H*	G_Y[15:8]								R	
0x26	*G_Z_OUT_L*	G_Z[7:0]								R	
0x27	*G_Z_OUT_H*	G_Z[15:8]								R	
0x28	*XL_X_OUT_L*	XL_X[7:0]								R	Acceleration data registers
0x29	*XL_X_OUT_H*	XL_X[15:8]								R	
0x2A	*XL_Y_OUT_L*	XL_Y[7:0]								R	
0x2B	*XL_Y_OUT_H*	XL_Y[15:8]								R	
0x2C	*XL_Z_OUT_L*	XL_Z[7:0]								R	
0x2D	*XL_Z_OUT_H*	XL_Z[15:8]								R	

Register Addr (Hex)	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Comments
0x2E-39	Reserved[1]	-								-	Reserved
0x3A	*FIFO_STATUS1*	DIFF_FIFO[7:0]								R	FIFO status registers
0x3B	*FIFO_STATUS2*	WATERM	OVER_RUN	FIFO_FULL_SMART	FIFO_EMPTY	0	DIFF_FIFO[10:8]			R	
0x3C	*FIFO_STATUS3*	FIFO_PATTERN[7:0]								R	
0x3D	*FIFO_STATUS4*	0						FIFO_PATTERN[9:8]		R	
0x3E	*FIFO_DATA_OUT_L*	DATA_OUT_FIFO_L[7:0]								R	FIFO data registers
0x3F	*FIFO_DATA_OUT_H*	DATA_OUT_FIFO_H[7:0]								R	
0x40-52	Reserved[1]	-								-	Reserved
0x53	*FUNC_SRC1*	0	0	TILT_IA	0	0	0	0	0	R	Interrupt registers
0x54-57	Reserved[1]	-								-	Reserved
0x58	*TAP_CFG*	INTERUPPTS_ENABLE	INACT_EN[1:0]		SLOPE_FDS	TAP_X_EN	TAP_Y_EN	TAP_Z_EN	LIR	R/W	Interrupt registers
0x59	*TAP_THS_6D*	D4D_EN	SIXD_THS[1:0]		TAP_THS[4:0]					R/W	
0x5A	*INT_DUR2*	DUR[3:0]				QUITE[1:0]		SHOCK[1:0]		R/W	
0x5B	*WAKE_UP_THS*	SINGLE_DOUBLE_TAP	0	WK_THS[5:0]						R/W	
0x5C	*WAKE_UP_DUR*	FF_DUR5	WAKE_DUR[1:0]		0	SLEEP_DUR[3:0]				R/W	
0x5D	*FREE_FALL*	FF_DUR[4:0]					FF_THS[2:0]			R/W	
0x5E	*MD1_CFG*	INT0_INACT_STATE	INT0_SINGLE_TAP	INT0_WU	INT0_FF	INT0_DOUBLE_TAP	INT0_6D	INT0_TILT	0	R/W	
0x5F	*MD2_CFG*	INT1_INACT_STATE	INT1_SINGLE_TAP	INT1_WU	INT1_FF	INT1_DOUBLE_TAP	INT1_6D	INT1_TILT	0	R/W	
0x60-72	Reserved[1]	-								-	Reserved
0x73	*X_OFS_USR*	X_OFS_USR[7:0]								R/W	Acceleration user offset correction
0x74	*Y_OFS_USR*	Y_OFS_USR[7:0]								R/W	
0x75	*Z_OFS_USR*	Z_OFS_USR[7:0]								R/W	
0x76-7F	Reserved[1]	-								-	Reserved

[1] *The registers contents that are loaded at boot procedure should not be changed. They contain the factory calibration values and their content is automatically restored when the device is powered up.*

[2] *This bit must be set to '0' for the correct operation of the device.*

Writing to Reserved registers is not allowed, it will cause permanent damage to the sensor

14 Register description

14.1 FIFO_CTRL1 (0x06)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
FTH[7:0]								R/W

Table 18: *FIFO_CTRL1* register

bits	Description
FTH[7:0]	FIFO threshold level setting. Default value: 0000 0000[1] Watermark flag rises when the number of bytes written to FIFO after the next write is greater than or equal to the threshold level. Minimum resolution for the FIFO is 1 LSB = 2 bytes (1 word) in FIFO

Table 19: *FIFO_CTRL1* register description

1. Consider FTH_[10:8] in *FIFO_CTRL2* (0x07) for a complete watermark threshold configuration.

14.2 FIFO_CTRL2 (0x07)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
FIFO_TIMER_EN	0	0	0	FIFO_TEMP_EN	FTH[10:8]			R/W

Table 20: *FIFO_CTRL2* register

bits	Description
FIFO_TIMER_EN	Enables timestamp data to be stored as the 4th FIFO data set. (0: timestamp not included in FIFO; 1: timestamp included in FIFO)
FIFO_TEMP_EN	Enables the temperature data storage in FIFO. Default: 0 (0: temperature not included in FIFO; 1: temperature included in FIFO)
FTH[10:8]	FIFO threshold level setting. Default value: 0000[1] Watermark flag rises when the number of bytes written to FIFO after the next write is greater than or equal to the threshold level. Minimum resolution for the FIFO is 1LSB = 2 bytes (1 word) in FIFO

Table 21: *FIFO_CTRL2* register description

1. Consider FTH_[7:0] in *FIFO_CTRL1* (06h) for a complete watermark threshold configuration.

14.3 FIFO_CTRL3 (0x08)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
0	0	DEC_FIFO_GYRO [2:0]			DEC_FIFO_XL [2:0]			R/W

Table 22: *FIFO_CTRL3* register

bits	Description
DEC_FIFO_GYRO [2:0]	Gyro FIFO (first data set) decimation setting. Default: 000 For the configuration setting, refer to Table 24.
DEC_FIFO_XL [2:0]	Acceleration sensor FIFO (second data set) decimation setting. Default: 000 For the configuration setting, refer to Table 25.

Table 23: *FIFO_CTRL3* register description

DEC_FIFO_GYRO [2:0]	Configuration
000	Gyroscope sensor not in FIFO
001	No decimation
010	Decimation with factor 2
011	Decimation with factor 3
100	Decimation with factor 4
101	Decimation with factor 8
110	Decimation with factor 16
111	Decimation with factor 32

Table 24: Gyro FIFO decimation setting

DEC_FIFO_XL [2:0]	Configuration
000	Acceleration sensor not in FIFO
001	No decimation
010	Decimation with factor 2
011	Decimation with factor 3
100	Decimation with factor 4
101	Decimation with factor 8
110	Decimation with factor 16
111	Decimation with factor 32

Table 25: Acceleration FIFO decimation setting

14.4 FIFO_CTRL4 (0x09)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
ON_FTH	HIGH_DATA	DEC_DS4_FIFO[2:0]			DEC_DS3_FIFO[2:0]			R/W

Table 26: *FIFO_CTRL4* register

bits	Description
ON_FTH	Enable FIFO threshold level use. Default value: 0 (0: FIFO depth is not limited; 1: FIFO depth is limited to threshold level).
HIGH_DATA	8-bit data storage in FIFO. Default: 0 (0: disable MSByte only memorization in FIFO for XL and Gyro; 1: enable MSByte only memorization in FIFO for XL and Gyro in FIFO)
DEC_DS4_FIFO[2:0]	Fourth FIFO data set decimation setting. Default: 000. For the configuration setting, refer to Table 28.
DEC_DS3_FIFO[2:0]	Third FIFO data set decimation setting. Default: 000. For the configuration setting, refer to Table 29.

Table 27: *FIFO_CTRL4* register description

DEC_DS4_FIFO[2:0]	Configuration
000	Fourth FIFO data set not in FIFO
001	No decimation
010	Decimation with factor 2
011	Decimation with factor 3
100	Decimation with factor 4
101	Decimation with factor 8
110	Decimation with factor 16
111	Decimation with factor 32

Table 28: Fourth FIFO data set decimation setting

DEC_DS3_FIFO[2:0]	Configuration
000	Third FIFO data set not in FIFO
001	No decimation
010	Decimation with factor 2
011	Decimation with factor 3
100	Decimation with factor 4
101	Decimation with factor 8
110	Decimation with factor 16
111	Decimation with factor 32

Table 29: Third FIFO data set not in FIFO

14.5 FIFO_CTRL5 (0x0A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
0	ODR_FIFO[3:0]				FIFO_MODE[2:0]			R/W

Table 30: *FIFO_CTRL5* register

bits	Description
ODR_FIFO[3:0]	FIFO ODR selection, setting FIFO_MODE also. Default: 0000 For the configuration setting, refer to Table 32.
FIFO_MODE_[2:0]	FIFO mode selection bits, setting ODR_FIFO also. Default value: 000 For the configuration setting, refer to Table 33.

Table 31: *FIFO_CTRL5* register description

ODR_FIFO[3:0]	Configuration
0000	FIFO disabled
0001	FIFO ODR is set to 12.5 Hz
0010	FIFO ODR is set to 26 Hz
0011	FIFO ODR is set to 52 Hz
0100	FIFO ODR is set to 104 Hz
0101	FIFO ODR is set to 208 Hz
0110	FIFO ODR is set to 416 Hz
0111	FIFO ODR is set to 833 Hz
1000	FIFO ODR is set to 1.66 kHz
1001	FIFO ODR is set to 3.33 kHz
1010	FIFO ODR is set to 6.66 kHz

Table 32: FIFO ODR selection

If the device is working at an ODR slower than the one selected, FIFO ODR is limited to that ODR value. Moreover, these bits are effective if the DATA_VALID_SEL FIFO bit of *MASTER_CONFIG* (0x1A) is set to 0.

FIFO_MODE_[2:0]	Configuration
000	Bypass mode. FIFO disabled.
001	FIFO mode. Stops collecting data when FIFO is full.
010	Reserved
011	Continuous mode until trigger is deasserted, then FIFO mode.
100	Bypass mode until trigger is deasserted, then Continuous mode.
101	Reserved
110	Continuous mode. If the FIFO is full, the new sample overwrites the older one.
111	Reserved

Table 33: FIFO mode selection

14.6 DRDY_PULSE_CFG (0x0B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
DRDY_PULSED	0	0	0	0	0	0	0	R/W

Table 34: *DRDY_PULSE_CFG*

bits	Description
DRDY_PULSED	Enable pulsed data-ready mode. Default value: 0 (0: data-ready latched mode. Returns to 0 only after output data has been read; 1: data-ready pulsed mode. The data-ready pulses are 75 µs long.)

Table 35: *DRDY_PULSE_CFG* register description

14.7 INT0_CTRL (0x0D)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3
0	0	INT0_FULL_FLAG	INT0_FIFO_OVR	INT0_FTH

Table 36: *INT0_CTRL* register

Bit 2	Bit 1	Bit 0	Type
INT0_BOOT	INT0_DRDY_G	INT0_DRDY_XL	R/W

Table 37: *INT0_CTRL* register

bits	Description
INT0_FULL_FLAG	FIFO full flag interrupt enable on INT0 pad. Default value: 0 (0: disabled; 1: enabled)
INT0_FIFO_OVR	FIFO overrun interrupt on INT0 pad. Default value: 0 (0: disabled; 1: enabled)
INT0_FTH	FIFO threshold interrupt on INT0 pad. Default value: 0 (0: disabled; 1: enabled)
INT0_BOOT	Boot status available on INT0 pad. Default value: 0 (0: disabled; 1: enabled)
INT0_DRDY_G	Gyroscope data-ready on INT0 pad. Default value: 0 (0: disabled; 1: enabled)
INT0_DRDY_XL	Acceleration sensor data-ready on INT0 pad. Default value: 0 (0: disabled; 1: enabled)

Table 38: *INT0_CTRL* register description

14.8 INT1_CTRL (0x0E)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3
0	0	INT2_FULL_FLAG	INT1_FIFO_OVR	INT1_FTH

Table 39: *INT1_CTRL* register

Bit 2	Bit 1	Bit 0	Type
INT1_DRDY_TEMP	INT1_DRDY_G	INT1_DRDY_XL	R/W

Table 40: *INT1_CTRL* register

bits	Description
INT1_FULL_FLAG	FIFO full flag interrupt enable on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_FIFO_OVR	FIFO overrun interrupt on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_FTH	FIFO threshold interrupt on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_DRDY_TEMP	Temperature data-ready on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_DRDY_G	Gyroscope data-ready on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_DRDY_XL	Acceleration sensor data-ready on INT1 pad. Default value: 0 (0: disabled; 1: enabled)

Table 41: *INT1_CTRL* register description

14.9 Device_ID (0x0F)

The value of this register gives the device ID, a value which is fixed: 0x6A(b01101010).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
0	1	1	0	1	0	1	0	R

Table 42: *Device_ID* register

14.10 CTRL1_XL (0x10)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
ODR_XL[3:0]				FS_XL[1:0]		LPF1_BW_SEL	BW0_XL	R/W

Table 43: *CTRL1_XL* register

bits	Description
ODR_XL[3:0]	Output data rate and power mode selection. Default value: 0000
FS_XL[1:0]	Acceleration full-scale selection. Default value: 00 (00: ±2 g; 01: ±16 g; 10: ±4 g; 11: ±8 g)
LPF1_BW_SEL	Acceleration digital LPF (LPF1) bandwidth selection. For bandwidth selection refer to *CTRL8_XL* (0x17).
BW0_XL	Acceleration analog chain bandwidth selection (only for acceleration $ODR \geq 1.67kHz$). (0: BW @ 1.5 kHz; 1: BW @ 400 Hz)

Table 44: *CTRL1_XL* register description

ODR_XL[3:0]	ODR selection @ XL_HM_MODE = 1	ODR selection @ XL_HM_MODE = 0
0000	Power down	Power down
1011	1.6 Hz (low power only)	12.5 Hz (high performance)
0001	12.5 Hz (low power)	12.5 Hz (high performance)
0010	26 Hz (low power)	26 Hz (high performance)
0011	52 Hz (low power)	52 Hz (high performance)
0100	104 Hz (normal mode)	104 Hz (high performance)
0101	208 Hz (normal mode)	208 Hz (high performance)
0110	416 Hz (high performance)	416 Hz (high performance)
0111	833 Hz (high performance)	833 Hz (high performance)
1000	1.66 kHz (high performance)	1.66 kHz (high performance)
1001	3.33 kHz (high performance)	3.33 kHz (high performance)
1010	6.66 kHz (high performance)	6.66 kHz (high performance)

Table 45: Acceleration sensor output data rate configuration

14.11 CTRL2_G (0x11)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
ODR_G[3:0]				FS_G[1:0]		FS_125	0	R/W

Table 46: *CTRL2_G* register

bits	Description
ODR_G[3:0]	Output data rate and power mode selection. Default value: 0000
FS_G[1:0]	Gyroscope full-scale selection. Default value: 00 (00: ±250 dps; 01: ±500 dps; 10: ±1000 dps; 11: ±2000 dps)
FS_125	Gyroscope full-scale at ±125 dps. Default 0 (0: disabled; 1: enabled)

Table 47: *CTRL2_G* register description

ODR_G[3:0]	ODR selection @ G_HM_MODE = 1	ODR selection @ G_HM_MODE = 0
0000	Power down	Power down
0001	12.5 Hz (low power)	12.5 Hz (high performance)
0010	26 Hz (low power)	26 Hz (high performance)
0011	52 Hz (low power)	52 Hz (high performance)
0100	104 Hz (normal mode)	104 Hz (high performance)
0101	208 Hz (normal mode)	208 Hz (high performance)
0110	416 Hz (high performance)	416 Hz (high performance)
0111	833 Hz (high performance)	833 Hz (high performance)
1000	1.66 kHz (high performance)	1.66 kHz (high performance)
1001	3.33 kHz (high performance)	3.33 kHz (high performance)
1010	6.66 kHz (high performance)	6.66 kHz (high performance)

Table 48: Gyroscope sensor output data rate configuration

14.12 CTRL3_C (0x12)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
BOOT	BDU	H_LACTIVE	PP_OD	SIM	IF_INC	BLE	SW_RESET	R/W

Table 49: *CTRL3_C* register

bits	Description
BOOT	Reboots memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
BDU	Block Data Update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
H_LACTIVE	Interrupt activation level. Default value: 0 (0: interrupt output pads active high; 1: interrupt output pads active low)
PP_OD	Push-pull/open-drain selection on INT0 and INT1 pads. Default value: 0 (0: push-pull mode; 1: open-drain mode)
SIM	SPI Serial Interface Mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
IF_INC	Register address automatically incremented during a multiple byte access with a serial interface (I^2C or SPI). Default value: 1 (0: disabled; 1: enabled)
BLE	Big/Little Endian Data selection. Default value 0 (0: data LSB @ lower address; 1: data MSB @ lower address)
SW_RESET	Software reset. Default value: 0 (0: normal mode; 1: reset device) This bit is automatically cleared.

Table 50: *CTRL3_C* register description

14.13 CTRL4_C (0x13)

Bit 7	Bit 6	Bit 5	Bit 4
DEN_XL_EN	SLEEP	INT1_on_INT0	DEN_DRDY_INT0

Table 51: *CTRL4_C* register

Bit 3	Bit 2	Bit 1	Bit 0	Type
DRDY_MASK	I^2C_disable	LPF1_SEL_G	0	R/W

Table 52: *CTRL4_C* register

bits	Description
DEN_XL_EN	Extend DEN functionality to acceleration sensor. Default value: 0 (0: disabled; 1: enabled)
SLEEP	Gyroscope sleep mode enable. Default value: 0 (0: disabled; 1: enabled)
INT1_on_INT0	All interrupt signals available on INT0 pad enable. Default value: 0 (0: interrupt signals divided between INT0 and INT1 pads; 1: all interrupt signals in logic or on INT0 pad)
DEN_DRDY_INT0	DEN DRDY signal on INT0 pad. Default value: 0 (0: disabled; 1: enabled)
DRDY_MASK	Configuration 1 data available enable bit. Default value: 0 (0: DA timer disabled; 1: DA timer enabled)
I^2C_disable	Disable I^2C interface. Default value: 0 (0: both I^2C and SPI enabled; 1: I^2C disabled, SPI only)
LPF1_SEL_G	Enable gyroscope digital LPF1. the bandwidth can be selected through FTYPE [1:0] in *CTRL6_C* (0x15) (0: disabled; 1: enabled)

Table 53: *CTRL4_C* register description

14.14 CTRL5_C (0x14)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
ROUNDING[2:0]			DEN_LH	ST_G[1:0]		ST_XL[1:0]		R/W

Table 54: *CTRL5_C* register

bits	Description
ROUNDING[2:0]	Circular burst-mode (rounding) read from output registers through the primary interface. Default value: 000 (000: no rounding; others: refer to Table 56)
DEN_LH	DEN active level configuration. Default value: 0 (0: active low; 1: active high)
ST_G [1:0]	Angular rate sensor self-test enable. Default value: 00 (00: self-test disabled; others: refer to Table 57)
ST_XL [1:0]	Linear acceleration sensor self-test enable. Default value: 00 (00: self-test disabled; others: refer to Table 58)

Table 55: *CTRL5_C* register description

ROUNDING[2:0]	Rounding pattern
000	No rounding
001	Acceleration only
010	Gyroscope only
011	Gyroscope + acceleration

Table 56: Output registers rounding pattern

ST1_G	ST0_G	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Not allowed
1	1	Negative sign self-test

Table 57: Angular rate sensor self-test mode selection

ST1_XL	ST0_XL	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

Table 58: Linear acceleration sensor self-test mode selection

14.15 CTRL6_C (0x15)

Bit 7	Bit 6	Bit 5
TRIG_EN	LVL1_EN	LVL2_EN

Table 59: *CTRL6_C* register

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
XL_HM_MODE	USR_OFF_W	0	FTYPE[1:0]		R/W

Table 60: *CTRL6_C* register

bits	Description
TRIG_EN	DEN data edge-sensitive trigger enable. Refer to Table 62.
LVL1_EN	DEN data level-sensitive trigger enable. Refer to Table 62.
LVL2_EN	DEN level-sensitive latched enable. Refer to Table 62.
XL_HM_MODE	High performance operating mode disable for acceleration. Default value: 0 (0: high performance operating mode enabled; 1: high performance operating mode disabled)
USR_OFF_W	Weight of XL user offset bits of registers *X_OFS_USR* (0x73), *Y_OFS_USR* (0x74), *Z_OFS_USR* (0x75) (0: 2^{-10} g/LSB; 1: 2^{-6} g/LSB)
FTYPE[1:0]	Gyroscope low pass filter (LPF1) bandwidth selection.Table 63 and Table 64 show the selectable bandwidth values.

Table 61: *CTRL6_C* register description

TRIG_EN, LVL1_EN, LVL2_EN	Trigger mode
100	Edge-sensitive trigger mode is selected
010	Level-sensitive trigger mode is selected
011	Level-sensitive latched mode is selected
110	Level-sensitive FIFO enable mode is selected

Table 62: Trigger mode selection

FTYPE[1:0]	Phase delay[1] (ODR=800 Hz)	Phase delay[1] (ODR=1.6 kHz)
00	14° (BW = 245 Hz)	10° (BW = 315 Hz)
01	17° (BW = 195 Hz)	12° (BW = 224 Hz)
10	19° (BW = 155 Hz)	15° (BW = 168 Hz)
11	13° (BW = 293 Hz)	8° (BW = 505 Hz)

Table 63: Gyroscope LPF1 bandwidth selection for ODR=800 Hz and ODR=1.6 kHz

FTYPE[1:0]	Phase delay[1] (ODR=3.3 kHz)	Phase delay[1] (ODR=6.6 kHz)
00	8° (BW = 343 Hz)	7° (BW = 351 Hz)
01	10° (BW = 234 Hz)	9° (BW = 237 Hz)
10	12° (BW = 172 Hz)	11° (BW = 173 Hz)
11	6° (BW = 925 Hz)	5° (BW = 937 Hz)

Table 64: Gyroscope LPF1 bandwidth selection for ODR=3.3 kHz and ODR=6.6 kHz

1. Phase delay @ 20 Hz

14.16 CTRL7_G (0x16)

Bit 7	Bit 6	Bit 5	Bit 4
G_HM_MODE	HP_EN_G	HPM_G[1:0]	

Table 65: *CTRL7_G* register

Bit 3	Bit 2	Bit 1	Bit 0	Type
0	ROUNDING_STATUS	0	0	R/W

Table 66: *CTRL7_G* register

bits	Description
G_HM_MODE	High performance operating mode disable for gyroscope. Default: 0 (0: high performance operating mode enabled; 1: high performance operating mode disabled)
HP_EN_G	Gyroscope digital high-pass filter enable. The filter is enabled only if the gyro is in HP mode. Default value: 0 (0: HPF disabled; 1: HPF enabled)
HPM_G[1:0]	Gyroscope digital HP filter cutoff selection. Default: 00 (00: 16 mHz; 01: 65 mHz; 10: 260 mHz; 11; 1.04 Hz)
ROUNDING_STATUS	Source register rounding function on *WAKE_UP_SRC* (0x1B), *TAP_SRC* (0x1C), *D6D_SRC* (0x1D), *STATUS_REG* (0x1E), and *FUNC_SRC1* (0x53) registers in the primary interface. Default value: 0 (0: rounding disabled; 1: rounding enabled)

Table 67: *CTRL7_G* register description

14.17 CTRL8_XL (0x17)

Bit 7	Bit 6	Bit 5	Bit 4
LPF2_XL_EN	HPCF_XL[1:0]		HP_REF_MODE

Table 68: *CTRL8_XL* register

Bit 3	Bit 2	Bit 1	Bit 0	Type
IN_COM	HP_SLOPE_XL_EN	0	LOW_PASS_ON_6D	R/W

Table 69: *CTRL8_XL* register

bits	Description
LPF2_XL_EN	Acceleration low-pass filter LPF2 selection.
HPCF_XL[1:0]	Acceleration LPF2 and high-pass filter configuration and cutoff setting. Refer to Table 71.
HP_REF_MODE	Enable HP filter reference mode. Default value: 0[1] (0: disabled; 1: enabled))
IN_COM	Composite filter input selection. Default: 0 (0: ODR/2 low pass filtered sent to composite filter (default) 1: ODR/4 low pass filtered sent to composite filter)
HP_SL_XL_EN	Acceleration slope filter / high-pass filter selection.
LOW_PASS_ON_6D	LPF2 on 6D function selection.

Table 70: *CTRL8_XL* register description

1. When enabled, the first output data has to be discarded.

HP_SL_XL_EN	LPF2_XL_EN	LPF1_BW_SEL	IN_COM	HPCF_XL[1:0]	Bandwidth
0[1](low-pass path)	0	0	-	-	ODR/2
		1	-	-	ODR/4
	1	-	1 (low noise) 0 (low latency)	00	ODR/50
				01	ODR/100
				10	ODR/9
				11	ODR/400
1[2](high-pass path)	-	-	0	00	ODR/4
				01	ODR/100
				10	ODR/9
				11	ODR/400

Table 71: Acceleration bandwidth selection

1. The bandwidth column is related to LPF1 if LPF2_XL_EN = 0 or LPF2 if LPF2_XL_EN = 1.
2. The bandwidth column is related to the slope filter if HPCF_XL[1:0] = 00 or to the HP filter if HPCF_XL[1:0] = 01/10/11.

14.18 CTRL9_XL (0x18)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
DEN_X	DEN_Y	DEN_Z	DEN_XL_G	0	0	0	0	R/W

Table 72: *CTRL9_XL* register

bits	Description
DEN_X	DEN value stored in LSB of X-axis. Default value: 1 (0: DEN not stored in X-axis LSB; 1: DEN stored in X-axis LSB)
DEN_Y	DEN value stored in LSB of Y-axis. Default value: 1 (0: DEN not stored in Y-axis LSB; 1: DEN stored in Y-axis LSB)
DEN_Z	DEN value stored in LSB of Z-axis. Default value: 1 (0: DEN not stored in Z-axis LSB; 1: DEN stored in Z-axis LSB)
DEN_XL_G	DEN stamping sensor selection. Default value: 0 (0: DEN pin info stamped in the gyroscope axis selected by bits [7:5]; 1: DEN pin info stamped in the acceleration axis selected by bits [7:5])

Table 73: *CTRL9_XL* register description

14.19 CTRL10_C (0x19)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
0	0	0	0	TILT_EN	FUNC_EN	0	0	R/W

Table 74: *CTRL10_C* register

bits	Description
TILT_EN	Enable tilt calculation.[1]
FUNC_EN	Enable embedded functionalities (tilt). Default value: 0 (0: disable functionalities of embedded functions and acceleration filters; 1: enable functionalities of embedded functions and acceleration filters)

Table 75: *CTRL10_C* register description

1. This is effective if the FUNC_EN bit is set to '1'.

14.20 MASTER_CONFIG (0x1A)

Bit 7	Bit 6	Bit 5	Bit 4
DRDY_ON_INT1	DATA_VALID_SEL_FIFO	0	START_CONFIG

Table 76: *MASTER_CONFIG* register

Bit 3	Bit 2	Bit 1	Bit 0	Type
0	0	0	0	R/W

Table 77: *MASTER_CONFIG* register

bits	Description
DRDY_ON_INT1	Manage the master DRDY signal on INT0 pad. Default: 0 (0: disable master DRDY on INT0; 1: enable master DRDY on INT0)
DATA_VALID_SEL_FIFO	Selection of FIFO data-valid signal. Default value: 0 (0: data-valid signal used to write data in FIFO is the XL/Gyro data-ready; 1: data-valid signal used to write data in FIFO is the sensor hub data-ready)

Table 78: *MASTER_CONFIG* register description

14.21 WAKE_UP_SRC (0x1B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
0	0	FF_IA	SLEEP_STATE_IA	WU_IA	X_WU	Y_WU	Z_WU	R

Table 79: *WAKE_UP_SRC* register

bits	Description
FF_IA	Free-fall event detection status. Default: 0 (0: free-fall event not detected; 1: free-fall event detected)
SLEEP_STATE_IA	Sleep event status. Default value: 0 (0: sleep event not detected; 1: sleep event detected)
WU_IA	Wakeup event detection status. Default value: 0 (0: wakeup event not detected; 1: wakeup event detected.)
X_WU	Wakeup event detection status on X-axis. Default value: 0 (0: wakeup event on X-axis not detected; 1: wakeup event on X-axis detected)
Y_WU	Wakeup event detection status on Y-axis. Default value: 0 (0: wakeup event on Y-axis not detected; 1: wakeup event on Y-axis detected)
Z_WU	Wakeup event detection status on Z-axis. Default value: 0 (0: wakeup event on Z-axis not detected; 1: wakeup event on Z-axis detected)

Table 80: *WAKE_UP_SRC* register description

14.22 TAP_SRC (0x1C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
0	TAP_IA	SINGLE_TAP	DOUBLE_TAP	TAP_SIGN	X_TAP	Y_TAP	Z_TAP	R

Table 81: *TAP_SRC* register

bits	Description
TAP_IA	Tap event detection status. Default: 0 (0: tap event not detected; 1: tap event detected)
SINGLE_TAP	Single-tap event status. Default value: 0 (0: single tap event not detected; 1: single tap event detected)
DOUBLE_TAP	Double-tap event detection status. Default value: 0 (0: double-tap event not detected; 1: double-tap event detected.)
TAP_SIGN	Sign of acceleration detected by tap event. Default: 0 (0: positive sign of acceleration detected by tap event; 1: negative sign of acceleration detected by tap event)
X_TAP	Tap event detection status on X-axis. Default value: 0 (0: tap event on X-axis not detected; 1: tap event on X-axis detected)
Y_TAP	Tap event detection status on Y-axis. Default value: 0 (0: tap event on Y-axis not detected; 1: tap event on Y-axis detected)
Z_TAP	Tap event detection status on Z-axis. Default value: 0 (0: tap event on Z-axis not detected; 1: tap event on Z-axis detected)

Table 82: *TAP_SRC* register description

14.23 D6D_SRC (0x1D)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
DEN_DRDY	D6D_IA	ZH	ZL	YH	YL	XH	XL	R

Table 83: *D6D_SRC* register

bits	Description
DEN_DRDY	DEN data-ready signal. It is set high when data output is related to the data coming from a DEN active condition.[1]
D6D_IA	Interrupt active for change position portrait, landscape, face-up, face-down. Default value: 0 (0: change position not detected; 1: change position detected)
ZH	Z-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
ZL	Z-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
YH	Y-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over-threshold) detected)
YL	Y-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
XH	X-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
XL	X-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)

Table 84: *D6D_SRC* register description

1. The DEN data-ready signal can be latched or pulsed depending on the value of the dataready_pulsed bit of the *DRDY_PULSE_CFG* (0x0B) register.

14.24 STATUS_REG (0x1E)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
0	0	0	0	0	TDA	GDA	XLDA	R

Table 85: *STATUS_REG* register

bits	Description
TDA	Temperature new data available. Default: 0 (0: no set of data is available at temperature sensor output; 1: a new set of data is available at temperature sensor output)
GDA	Gyroscope new data available. Default value: 0 (0: no set of data available at gyroscope output; 1: a new set of data is available at gyroscope output)
XLDA	Acceleration new data available. Default value: 0 (0: no set of data available at acceleration output; 1: a new set of data is available at acceleration output)

Table 86: *STATUS_REG* register description

14.25 T_OUT_L (0x20)

Temperature data output register. L and H registers together express a 16-bit word in two's complement.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
Temp[7:0]								R

Table 87: *T_OUT_L* register

14.26 T_OUT_H (0x21)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
Temp[15:8]								R

Table 88: *T_OUT_H* register

bits	Description
Temp[15:0]	Temperature sensor output data. The value is expressed as two's complement sign extended on the MSB.

Table 89: *T_OUT_H* register description

14.27 G_X_OUT_L (0x22)

Angular rate sensor pitch axis (X) angular rate output register. The value is expressed as a 16-bit word in two's complement. If this register is read by the primary interface, data are according to the full scale and ODR settings (*CTRL2_G* (0x11))

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
G_X[7:0]								R

Table 90: *G_X_OUT_L* register

bits	Description
G_X[7:0]	Pitch axis (X) angular rate value (LSbyte) G_X[15:0] expressed in two's complement and its value depends on the interface used: SPI/I²C: Gyro GP chain pitch axis output

Table 91: *G_X_OUT_L* register description

14.28 G_X_OUT_H (0x23)

Angular rate sensor pitch axis (X) angular rate output register. The value is expressed as a 16-bit word in two's complement. If this register is read by the primary interface, data are according to the full scale and ODR settings (*CTRL2_G*(0x11))

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
G_X[15:8]								R

Table 92: *G_X_OUT_H* register

bits	Description
G_X[15:8]	Pitch axis (X) angular rate value (MSbyte) G_X[15:0] expressed in two's complement and its value depends on the interface used: SPI/I²C: Gyro GP chain pitch axis output

Table 93: *G_X_OUT_H* register description

14.29 G_Y_OUT_L (0x24)

Angular rate sensor roll axis (Y) angular rate output register. The value is expressed as a 16-bit word in two's complement. If this register is read by the primary interface, data are according to the full scale and ODR settings (*CTRL2_G* (0x11))

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
G_Y[7:0]								R

Table 94: *G_Y_OUT_L* register

bits	Description
G_Y[7:0]	Roll axis (Y) angular rate value (LSbyte) G_Y[15:0] expressed in two's complement and its value depends on the interface used: SPI/I²C: Gyro GP chain roll axis output

Table 95: *G_Y_OUT_L* register description

14.30 G_Y_OUT_H (0x25)

Angular rate sensor roll axis (Y) angular rate output register. The value is expressed as a 16-bit word in two's complement. If this register is read by the primary interface, data are according to the full scale and ODR settings (*CTRL2_G* (0x11))

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
G_Y[15:8]								R

Table 96: *G_Y_OUT_H* register

bits	Description
G_Y[15:8]	Roll axis (Y) angular rate value (MSbyte) G_Y[15:0] expressed in two's complement and its value depends on the interface used: SPI/I^{2}C: Gyro GP chain roll axis output

Table 97: *G_Y_OUT_H* register description

14.31 G_Z_OUT_L (0x26)

Angular rate sensor yaw axis (Z) angular rate output register. The value is expressed as a 16-bit word in two's complement. If this register is read by the primary interface, data are according to the full scale and ODR settings (*CTRL2_G* (0x11))

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
G_Z[7:0]								R

Table 98: *G_Z_OUT_L* register

bits	Description
G_Z[7:0]	Yaw axis (Z) angular rate value (LSbyte) G_Z[15:0] expressed in two's complement and its value depends on the interface used: SPI/I^{2}C: Gyro GP chain yaw axis output.

Table 99: *G_Z_OUT_L* register description

14.32 G_Z_OUT_H (0x27)

Angular rate sensor yaw axis (Z) angular rate output register. The value is expressed as a 16-bit word in two's complement. If this register is read by the primary interface, data are according to the full scale and ODR settings (*CTRL2_G* (0x11))

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
G_Z[15:8]								R

Table 100: *G_Z_OUT_H* register

bits	Description
G_Z[15:8]	Yaw axis (Z) angular rate value (MSbyte) G_Z[15:0] expressed in two's complement and its value depends on the interface used: SPI/I^{2}C: Gyro GP chain yaw axis output.

Table 101: *G_Z_OUT_H* register description

14.33 XL_X_OUT_L (0x28)

Linear acceleration sensor X-axis output register. The value is expressed as a 16-bit word in two's complement.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
XL_X[7:0]								R

Table 102: *XL_X_OUT_L* register

bits	Description
XL_X[7:0]	X-axis linear acceleration value (LSbyte).

Table 103: *XL_X_OUT_L* register description

14.34 XL_X_OUT_H (0x29)

Linear acceleration sensor X-axis output register. The value is expressed as a 16-bit word in two's complement.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
XL_X[15:8]								R

Table 104: *XL_X_OUT_H* register

bits	Description
XL_X[15:8]	X-axis linear acceleration value (MSbyte).

Table 105: *XL_X_OUT_H* register description

14.35 XL_Y_OUT_L (0x2A)

Linear acceleration sensor Y-axis output register. The value is expressed as a 16-bit word in two's complement.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
XL_Y[7:0]								R

Table 106: *XL_Y_OUT_L* register

bits	Description
XL_Y[7:0]	Y-axis linear acceleration value (LSbyte).

Table 107: *XL_Y_OUT_L* register description

14.36 XL_Y_OUT_H (0x2B)

Linear acceleration sensor Y-axis output register. The value is expressed as a 16-bit word in two's complement.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
XL_Y[15:8]								R

Table 108: *XL_Y_OUT_H* register

bits	Description
XL_Y[15:8]	Y-axis linear acceleration value (MSbyte).

Table 109: *XL_Y_OUT_H* register description

14.37 XL_Z_OUT_L (0x2C)

Linear acceleration sensor Z-axis output register. The value is expressed as a 16-bit word in two's complement.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
XL_Z[7:0]								R

Table 110: *XL_Z_OUT_L* register

bits	Description
XL_Z[7:0]	Z-axis linear acceleration value (LSbyte).

Table 111: *XL_Z_OUT_L* register description

14.38 XL_Z_OUT_H (0x2D)

Linear acceleration sensor Z-axis output register. The value is expressed as a 16-bit word in two's complement.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
XL_Z[15:8]								R

Table 112: *XL_Z_OUT_H* register

bits	Description
XL_Z[15:8]	Z-axis linear acceleration value (MSbyte).

Table 113: *XL_Z_OUT_H* register description

14.39 FIFO_STATUS1 (0x3A)

FIFO status control register. For a proper read of the register, it is recommended to set the BDU bit in *CTRL3_C* (0x12) to 1.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
DIFF_FIFO[7:0]								R

Table 114: *FIFO_STATUS1* register

bits	Description
DIFF_FIFO[7:0]	Number of unread words (16-bit axes) stored in FIFO.

Table 115: *FIFO_STATUS1* register description

14.40 FIFO_STATUS2 (0x3B)

FIFO status control register. For a proper read of the register, it is recommended to set the BDU bit in *CTRL3_C* (0x12) to 1.

Bit 7	Bit 6	Bit 5
WaterM	OVER_RUN	FIFO_FULL_SMART

Table 116: *FIFO_STATUS2* register

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
FIFO_EMPTY	0	DIFF_FIFO[10:8]			R

Table 117: *FIFO_STATUS2* register

bits	Description
WaterM	FIFO watermark status. The watermark is set through bits FTH_[7:0] in *FIFO_CTRL1* (0x06). Default value: 0 (0: FIFO filling is lower than watermark level[1]; 1: FIFO filling is equal to or higher than the watermark level).
OVER_RUN	FIFO overrun status. Default value: 0 (0: FIFO is not completely filled; 1: FIFO is completely filled)
FIFO_FULL_SMART	Smart FIFO full status. Default value: 0 (0: FIFO is not full; 1: FIFO will be full at the next ODR)
FIFO_EMPTY	FIFO empty bit. Default value: 0 (0: FIFO contains data; 1: FIFO is empty)
DIFF_FIFO_[10:8]	Number of unread words (16-bit axes) stored in FIFO.[2]

Table 118: *FIFO_STATUS2* register description

1. FIFO watermark level is set in FTH_[10:0] in *FIFO_CTRL1* (0x06) and *FIFO_CTRL2* (0x07)
2. For a complete number of unread samples, consider DIFF_FIFO [7:0] in *FIFO_STATUS1* (0x3A)

14.41 FIFO_STATUS3 (0x3C)

FIFO status control register. For a proper read of the register, it is recommended to set the BDU bit in *CTRL3_C* (0x12) to 1.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
FIFO_PATTERN[7:0]								R

Table 119: *FIFO_STATUS3* register

bits	Description
FIFO_PATTERN[7:0]	Word of recursive pattern read at the next read.

Table 120: *FIFO_STATUS3* register description

14.42 FIFO_STATUS4 (0x3D)

FIFO status control register. For a proper read of the register, it is recommended to set the BDU bit in *CTRL3_C* (0x12) to 1.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
0	0	0	0	0	0	FIFO_PATTERN[9:8]		R

Table 121: *FIFO_STATUS4* register

bits	Description
FIFO_PATTERN[9:8]	Word of recursive pattern read at the next read.

Table 122: *FIFO_STATUS4* register description

14.43 FIFO_DATA_OUT_L (0x3E)

FIFO data output register. For a proper read of the register, it is recommended to set the BDU bit in *CTRL3_C* (0x12) to 1.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
DATA_OUT_FIFO_L_[7:0]								R

Table 123: *FIFO_DATA_OUT_L* register

bits	Description
DATA_OUT_FIFO_L_[7:0]	FIFO data output (first byte)

Table 124: *FIFO_DATA_OUT_L* register description

14.44 FIFO_DATA_OUT_H (0x3F)

FIFO data output register. For a proper read of the register, it is recommended to set the BDU bit in *CTRL3_C* (0x12) to 1.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
DATA_OUT_FIFO_H_[7:0]								R

Table 125: *FIFO_DATA_OUT_H* register

bits	Description
DATA_OUT_FIFO_H_[7:0]	FIFO data output (second byte)

Table 126: *FIFO_DATA_OUT_H* register description

14.45 FUNC_SRC1 (0x53)

Tilt interrupt source register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
0	0	TILT_IA	0	0	0	0	0	R

Table 127: *FUNC_SRC1* register

bits	Description
TILT_IA	Tilt event detection status. Default value: 0 (0: tilt event not detected; 1: tilt event detected)

Table 128: *FUNC_SRC1* register description

14.46 TAP_CFG (0x58)

Enables interrupt and inactivity functions, configuration of filtering, and tap recognition functions (r/w).

Bit 7	Bit 6	Bit 5	Bit 4
INTERRUPTS_ENABLE	INACT_EN[1:0]		SLOPE_FDS

Table 129: *TAP_CFG* register

Bit 3	Bit 2	Bit 1	Bit 0	Type
TAP_X_EN	TAP_Y_EN	TAP_Z_EN	LIR	R/W

Table 130: *TAP_CFG* register

bits	Description
INTERRUPTS_ENABLE	Enable basic interrupts (6D/4D, free-fall, wake-up, tap, inactivity). Default value: 0 (0: interrupt disabled; 1: interrupt enabled)
INACT_EN[1:0]	Enable inactivity function. Default value: 00 (00: disabled 01: sets acceleration ODR to 12.5 Hz (low power mode), gyro does not change; 10: sets acceleration ODR to 12.5 Hz (low power mode), gyro to sleep mode; 11: sets acceleration ODR to 12.5 Hz (low power mode), gyro to power down mode)
SLOPE_FDS	HPF or SLOPE filter selection on wake-up and activity/inactivity functions. Default value: 0 0: SLOPE filter applied; 1: HPF applied)
TAP_X_EN	Enable X direction in tap recognition. Default value: 0 (0: X direction disabled; 1: X direction enabled)
TAP_Y_EN	Enable Y direction in tap recognition. Default value: 0 (0: Y direction disabled; 1: Y direction enabled)
TAP_Z_EN	Enable Z direction in tap recognition. Default value: 0 (0: Z direction disabled; 1: Z direction enabled)
LIR	Latched Interrupt. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)

Table 131: *TAP_CFG* register description

14.47 TAP_THS_6D (0x59)

Portrait/landscape position and tap function threshold register (r/w).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
D4D_EN	SIXD_THS[1:0]		TAP_THS[4:0]					R/W

Table 132: *TAP_THS_6D* register

bits	Description
D4D_EN	4D orientation detection enable. Z-axis position detection is disabled. Default value: 0 (0: enabled; 1: disabled)
SIXD_THS[1:0]	Threshold for 4D/6D function. Default value: 00. Threshold for D4D/D6D function.
TAP_THS[4:0]	Threshold for tap recognition. Default value: 00000 1 LSb corresponds to FS_XL/2^5

Table 133: *TAP_THS_6D* register description

SIXD_THS[1:0]	Threshold value
00	80 degrees
01	70 degrees
10	60 degrees
11	50 degrees

Table 134: *Threshold for D4D/D6D function*

14.48 INT_DUR2 (0x5A)

Tap recognition function setting register (r/w).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
DUR[3:0]				QUIET[1:0]		SHOCK[1:0]		R/W

Table 135: *INT_DUR2* register

bits	Description
DUR[3:0]	Duration of maximum time gap for double tap recognition. Default: 0000 When double tap recognition is enabled, this register expresses the maximum time between two consecutive detected taps to determine a double tap event. The default value of these bits is 0000b which corresponds to 16*ODR_XL time. If the DUR[3:0] bits are set to a different value, 1LSB corresponds to 32*ODR_XL time.
QUIET[1:0]	Expected quiet time after a tap detection. Default value: 00 Quiet time is the time after the first detected tap in which there must not be any over threshold event. The default value of these bits is 00b which corresponds to 2*ODR_XL time. If the QUIET[1:0] bits are set to a different value, 1LSB corresponds to 4*ODR_XL time.
SHOCK[1:0]	Maximum duration of over threshold event. Default value: 00 Maximum duration is the maximum time of an over threshold signal detection to be recognized as a tap event. The default value of these bits is 00b which corresponds to 4*ODR_XL time. If the SHOCK[1:0] bits are set to a different value, 1LSB corresponds to 8*ODR_XL time.

Table 136: *INT_DUR2* register description

14.49 WAKE_UP_THS (0x5B)

Single and double-tap function threshold register (r/w).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
SINGLE_DOUBLE_TAP	0	WK_THS[5:0]						R/W

Table 137: *WAKE_UP_THS* register

bits	Description
SINGLE_DOUBLE_TAP	Single/double-tap event enable. Default: 0 (0: only single-tap event enabled; 1: both single and double-tap events enabled)
WK_THS[5:0]	Threshold for wakeup. Default value: 000000 1 LSb corresponds to $FS\_XL/2^6$

Table 138: *WAKE_UP_THS* register description

14.50 WAKE_UP_DUR (0x5C)

Free-fall, wakeup, timestamp and sleep mode functions duration setting register (r/w).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
FF_DUR5	WAKE_DUR[1:0]		0	SLEEP_DUR[3:0]				R/W

Table 139: *WAKE_UP_DUR* register

bits	Description
FF_DUR5	Free fall duration event. Default: 0 For the complete configuration of the free-fall duration, refer to FF_DUR[4:0] in *FREE_FALL* (0x5D) configuration. 1 LSB = 1 ODR_time
WAKE_DUR[1:0]	Wake up duration event. Default: 00 1LSB = 1 ODR_time
SLEEP_DUR[3:0]	Duration to go in sleep mode. Default value: 0000 (this corresponds to 16 ODR) 1 LSB = 512 ODR

Table 140: *WAKE_UP_DUR* register description

14.51 FREE_FALL (0x5D)

Free-fall function duration setting register (r/w).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
FF_DUR[4:0]					FF_THS[2:0]			R/W

Table 141: *FREE_FALL* register

bits	Description
FF_DUR[4:0]	Free fall duration event. Default: 0 For the complete configuration of the free-fall duration, refer to FF_DUR5 in *WAKE_UP_DUR* (0x5C) configuration.
FF_THS[2:0]	Free fall threshold setting. Default: 000 For details refer to Table 143

Table 142: *FREE_FALL* register description

FF_THS[2:0]	Threshold value
000	156 mg
001	219 mg
010	250 mg
011	312 mg
100	344 mg
101	406 mg
110	469 mg
111	500 mg

Table 143: *Threshold for free-fall function*

14.52 MD1_CFG (0x5E)

Functions routing on INT0 register (r/w).

Bit 7	Bit 6	Bit 5	Bit 4
INT0_INACT_STATE	INT0_SINGLE_TAP	INT0_WU	INT0_FF

Table 144: *MD1_CFG* register

Bit 3	Bit 2	Bit 1	Bit 0	Type
INT0_DOUBLE_TAP	INT0_6D	INT0_TILT	0	R/W

Table 145: *MD1_CFG* register

bits	Description
INT0_INACT_STATE	Routing on INT0 of inactivity mode. Default: 0 (0: routing on INT0 of inactivity disabled; 1: routing on INT0 of inactivity enabled)
INT0_SINGLE_TAP	Single-tap recognition routing on INT0. Default: 0 (0: routing of single-tap event on INT0 disabled; 1: routing of single-tap event on INT0 enabled)
INT0_WU	Routing of wakeup event on INT0. Default value: 0 (0: routing of wakeup event on INT0 disabled; 1: routing of wakeup event on INT0 enabled)
INT0_FF	Routing of free-fall event on INT0. Default value: 0 (0: routing of free-fall event on INT0 disabled; 1: routing of free-fall event on INT0 enabled)
INT0_DOUBLE_TAP	Routing of tap event on INT0. Default value: 0 (0: routing of double-tap event on INT0 disabled; 1: routing of double-tap event on INT0 enabled)
INT0_6D	Routing of 6D event on INT0. Default value: 0 (0: routing of 6D event on INT0 disabled; 1: routing of 6D event on INT0 enabled)
INT0_TILT	Routing of tilt event on INT0. Default value: 0 (0: routing of tilt event on INT0 disabled; 1: routing of tilt event on INT0 enabled)

Table 146: *MD1_CFG* register description

14.53 MD2_CFG (0x5F)

Functions routing on INT1 register (r/w).

Bit 7	Bit 6	Bit 5	Bit 4
INT1_INACT_STATE	INT1_SINGLE_TAP	INT1_WU	INT1_FF

Table 147: *MD2_CFG* register

Bit 3	Bit 2	Bit 1	Bit 0	Type
INT1_DOUBLE_TAP	INT1_6D	INT1_TILT	0	R/W

Table 148: *MD2_CFG* register

bits	Description
INT1_INACT_STATE	Routing on INT1 of inactivity mode. Default: 0 (0: routing on INT1 of inactivity disabled; 1: routing on INT1 of inactivity enabled)
INT1_SINGLE_TAP	Single-tap recognition routing on INT1. Default: 0 (0: routing of single-tap event on INT1 disabled; 1: routing of single-tap event on INT1 enabled)
INT1_WU	Routing of wakeup event on INT1. Default value: 0 (0: routing of wakeup event on INT1 disabled; 1: routing of wakeup event on INT1 enabled)
INT1_FF	Routing of free-fall event on INT1. Default value: 0 (0: routing of free-fall event on INT1 disabled; 1: routing of free-fall event on INT1 enabled)
INT1_DOUBLE_TAP	Routing of tap event on INT1. Default value: 0 (0: routing of double-tap event on INT1 disabled; 1: routing of double-tap event on INT1 enabled)
INT1_6D	Routing of 6D event on INT1. Default value: 0 (0: routing of 6D event on INT1 disabled; 1: routing of 6D event on INT1 enabled)
INT1_TILT	Routing of tilt event on INT1. Default value: 0 (0: routing of tilt event on INT1 disabled; 1: routing of tilt event on INT1 enabled)

Table 149: *MD2_CFG* register description

14.54 X_OFS_USR (0x73)

Acceleration X-axis user offset correction (r/w). The offset value set in the *X_OFS_USR* offset register is internally added to the acceleration value measured on the X-axis.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
X_OFS_USR[7:0]								R/W

Table 150: *X_OFS_USR* register

bits	Description
X_OFS_USR[7:0]	Acceleration X-axis user offset correction expressed in two's complement, weight depends on the *CTRL6_C*(4) bit. The value must be in the range [-127 127].

Table 151: *X_OFS_USR* register description

14.55 Y_OFS_USR (0x74)

Acceleration Y-axis user offset correction (r/w). The offset value set in the *Y_OFS_USR* offset register is internally added to the acceleration value measured on the Y-axis.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
Y_OFS_USR[7:0]								R/W

Table 152: *Y_OFS_USR* register

bits	Description
Y_OFS_USR[7:0]	Acceleration Y-axis user offset correction expressed in two's complement, weight depends on the *CTRL6_C*(4) bit. The value must be in the range [-127 127].

Table 153: *Y_OFS_USR* register description

14.56 Z_OFS_USR (0x75)

Acceleration Z-axis user offset correction (r/w). The offset value set in the *Z_OFS_USR* offset register is internally added to the acceleration value measured on the Z-axis.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type
Z_OFS_USR[7:0]								R/W

Table 154: *Z_OFS_USR* register

bits	Description
Z_OFS_USR[7:0]	Acceleration Z-axis user offset correction expressed in two's complement, weight depends on the *CTRL6_C*(4) bit. The value must be in the range [-127 127].

Table 155: *Z_OFS_USR* register description

15 Physical specifications

15.1 Module drawing

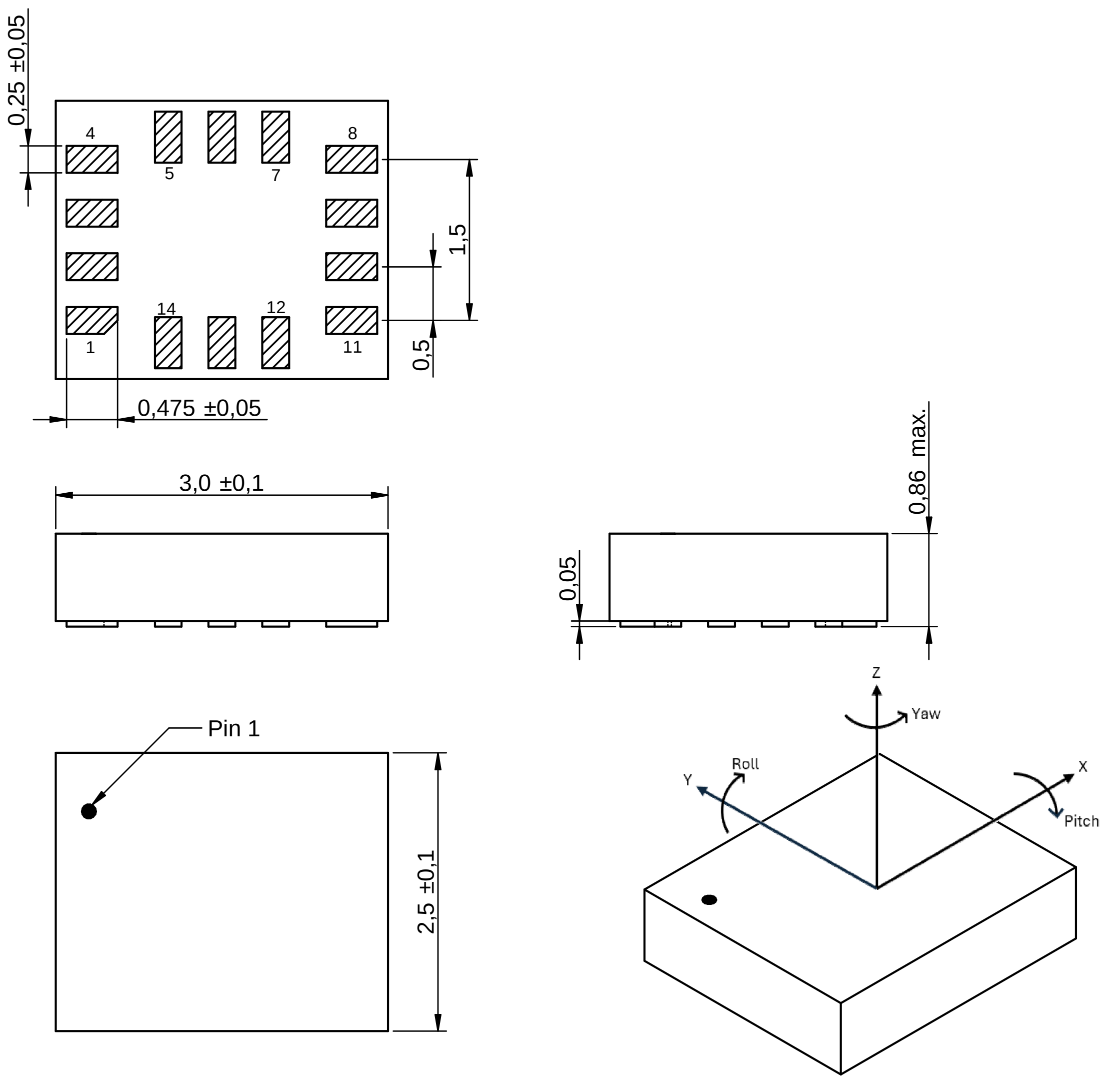


Figure 19: Sensor dimensions [mm]

15.2 Footprint

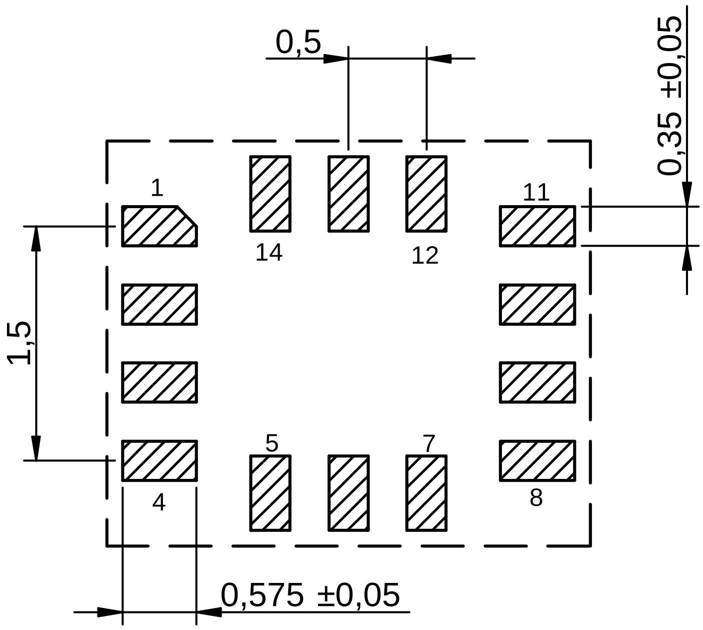


Figure 20: Recommended land pattern [mm] (top view)

16 Manufacturing information

16.1 Moisture sensitivity level

The sensor product is categorized as JEDEC Moisture Sensitivity Level 3 (MSL3), which requires special handling.

More information regarding the MSL requirements can be found in the IPC/JEDEC J-STD-020 standard on *www.jedec.org*. More information about the handling, picking, shipping and the usage of moisture/re-flow and/or process sensitive products can be found in the IPC/JEDEC J-STD-033 standard on *www.jedec.org*.

16.2 Soldering

16.2.1 Reflow soldering

Attention must be paid on the thickness of the solder resist between the host PCB top side and the modules bottom side. Only lead-free assembly is recommended according to JEDEC J-STD020.

Profile feature		Value
Preheat temperature Min	$T_{S\ Min}$	150 °C
Preheat temperature Max	$T_{S\ Max}$	200 °C
Preheat time from $T_{S\ Min}$ to $T_{S\ Max}$	t_S	60 - 120 seconds
Ramp-up rate (T_L to T_P)		3 °C / second max.
Liquidous temperature	T_L	217 °C
Time t_L maintained above T_L	t_L	60 - 150 seconds
Peak package body temperature	T_P	see table below
Time within 5 °C of actual peak temperature	t_P	20 - 30 seconds
Ramp-down Rate (T_P to T_L)		6 °C / second max.
Time 20 °C to T_P		8 minutes max.

Table 156: Classification reflow soldering profile, Note: refer to IPC/JEDEC J-STD-020E

*** In order to reduce residual stress on the sensor component, the recommended ramp-down temperature slope should be lower than 3 °C /s.**

Package thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ >2000
< 1.6 mm	260 ℃	260 ℃	260 ℃
1.6 mm - 2.5 mm	260 ℃	250 ℃	245 ℃
> 2.5 mm	250 ℃	245 ℃	245 ℃

Table 157: Package classification reflow temperature, PB-free assembly, Note: refer to IPC/-JEDEC J-STD-020E

It is recommended to solder the sensor on the last re-flow cycle of the PCB. For solder paste use a LFM-48W or Indium based SAC 305 alloy (Sn 96.5 / Ag 3.0 / Cu 0.5 / Indium 8.9HF / Type 3 / 89%) type 3 or higher.

The reflow profile must be adjusted based on the thermal mass of the entire populated PCB, heat transfer efficiency of the reflow oven and the specific type of solder paste used. Based on the specific process and PCB layout the optimal soldering profile must be adjusted and verified. Other soldering methods (e.g. vapor phase) have not been verified and have to be validated by the customer at their own risk. Rework is not recommended.

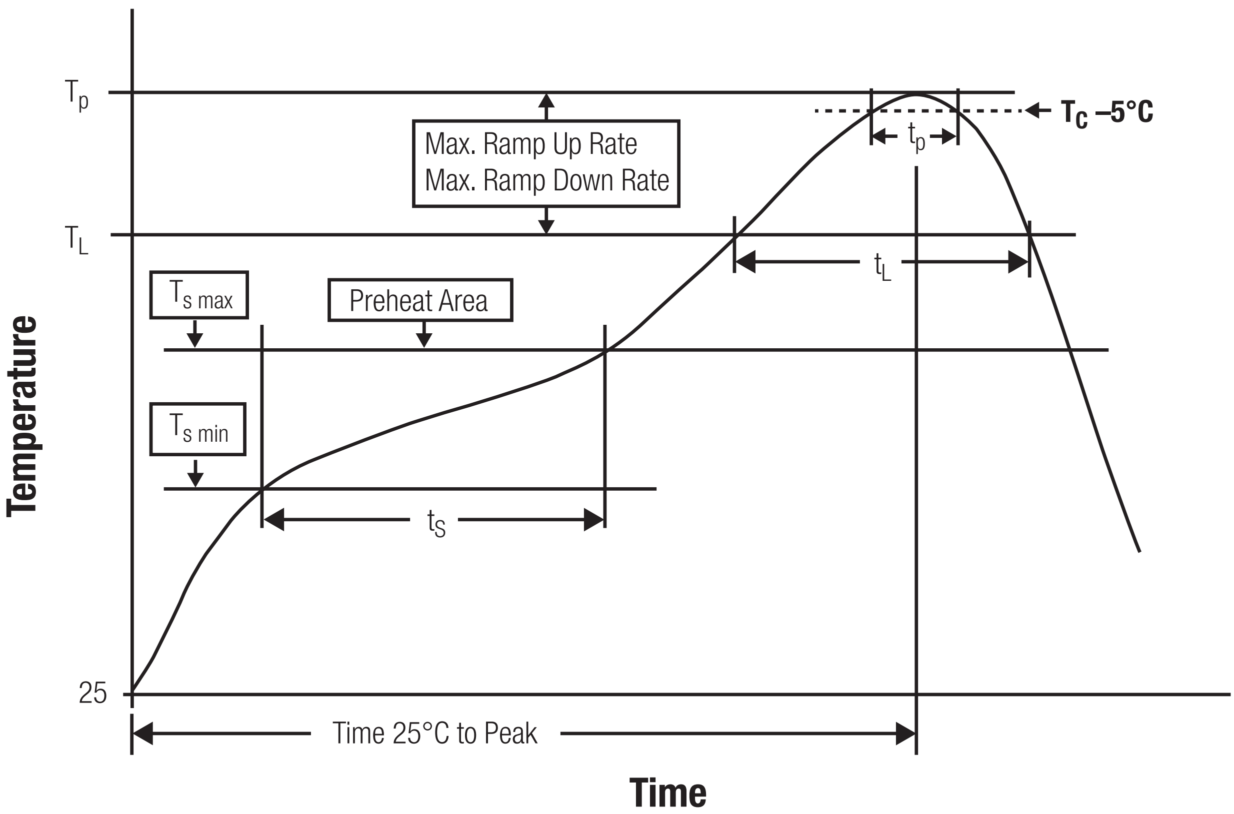


Figure 21: Reflow soldering profile

After reflow soldering, visually inspect the board to confirm proper alignment

16.2.2 Cleaning and washing

Do not clean the product. Any residue cannot be easily removed by washing. Use a "no clean" soldering paste and do not clean the board after soldering.

- Washing agents used during the production to clean the customer application might damage or change the characteristics of the component. Washing agents may have a negative effect on the long-term functionality of the product.
- Using a brush during the cleaning process may damage the component. Therefore, we do not recommend using a brush during the PCB cleaning process

16.2.3 Potting and coating

- Potting material might shrink or expand during and after hardening. This might apply mechanical stress on the components, which can influence the characteristics of the transfer function. In addition, potting material can close existing openings in the housing. This can lead to a malfunction of the component. Thus, potting is not recommended.
- Conformal coating may affect the product performance. We do not recommend coating the components.

16.2.4 Storage conditions

- A storage of Würth Elektronik eiSos products for longer than 12 months is not recommended. Within other effects, the terminals may suffer degradation, resulting in bad solderability. Therefore, all products shall be used within the period of 12 months based on the day of shipment.
- Do not expose the components to direct sunlight.
- The storage conditions in the original packaging are defined according to DIN EN 61760 - 2.
- For a moisture sensitive component, the storage condition in the original packaging is defined according to IPC/JEDEC-J-STD-033. It is also recommended to return the component to the original moisture proof bag and reseal the moisture proof bag again.

16.2.5 Handling

- Violation of the technical product specifications such as exceeding the nominal rated supply voltage, will void the warranty.
- Violation of the technical product specifications such as but not limited to exceeding the absolute maximum ratings will void the conformance to regulatory requirements.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

- The edge castellation is designed and made for prototyping, i.e. hand soldering purposes only.
- The applicable country regulations and specific environmental regulations must be observed.
- Do not disassemble the product. Evidence of tampering will void the warranty.

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