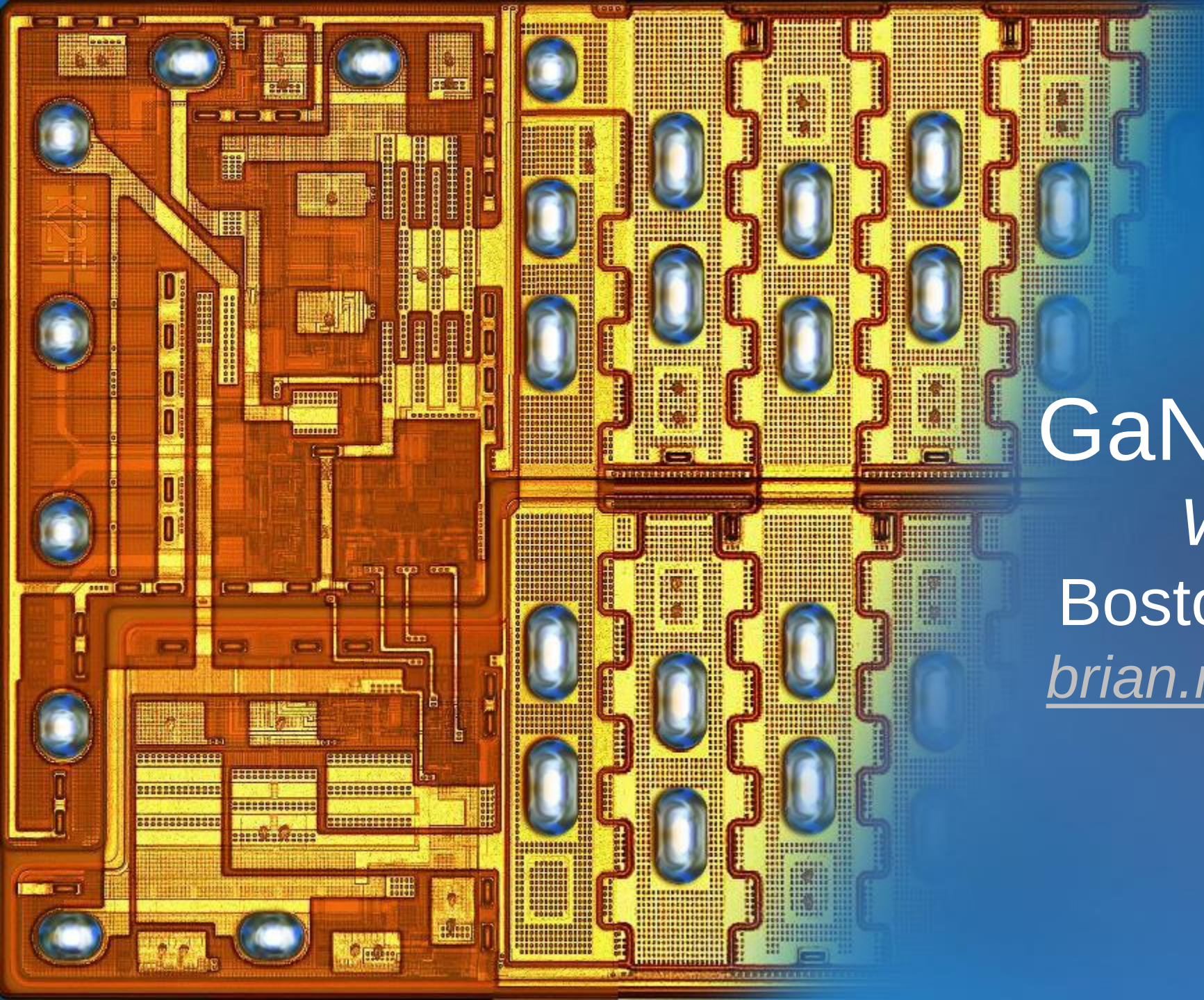


GaN FET Layout

Wurth Power Day

Boston, Oct. 22, 2024

brian.miller@epc-co.com

EFFICIENT POWER CONVERSION

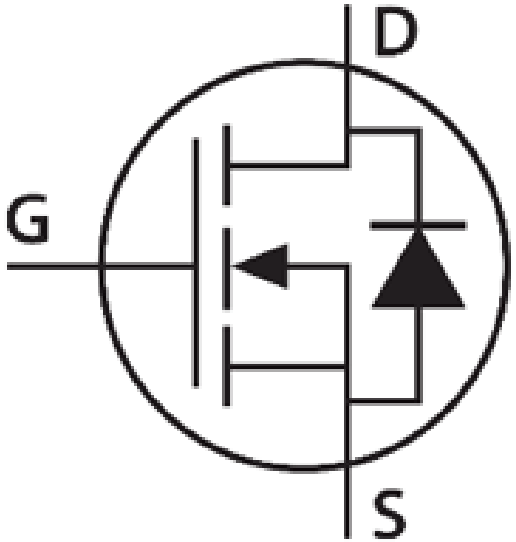
Agenda

- Why use GaN FETs?
- Layout Optimization Benefits
- Layout
  - Shortcuts to get a good layout
- Examples
- Resources

GaN FET Overview

GaN FETs: like MOSFETs but…

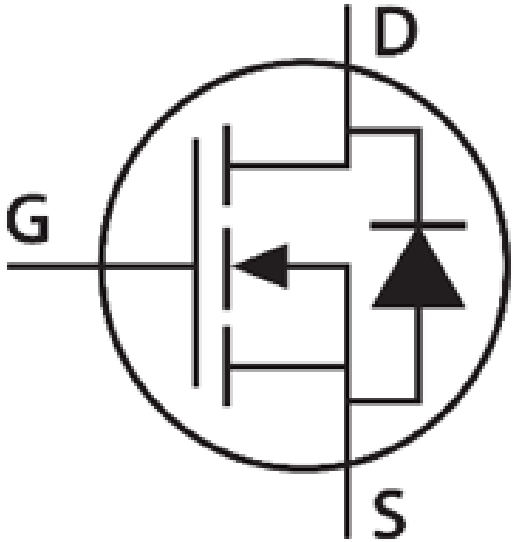
- Smaller
- Switch faster
- Reverse voltage conduction
  - Main channel, not a parasitic element
- Zero reverse recovery (Q_{RR})
- Miller ratio < 1 (Q_{GD}/Q_{GS_Th})
  (dv/dt immunity)
- Exceptional reliability



GaN FET Overview

Benefits:

- Smaller, due to:
  - Smaller devices
  - Higher frequency
  - Smaller heat sinks
- More efficient
- Exceptional reliability



EPC 200 V vs. Si Devices

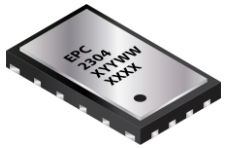
Si MOSFET Benchmark

9.9 x 11.7 mm

eGaN FET

4.6 x 1.6 mm

eGaN FET



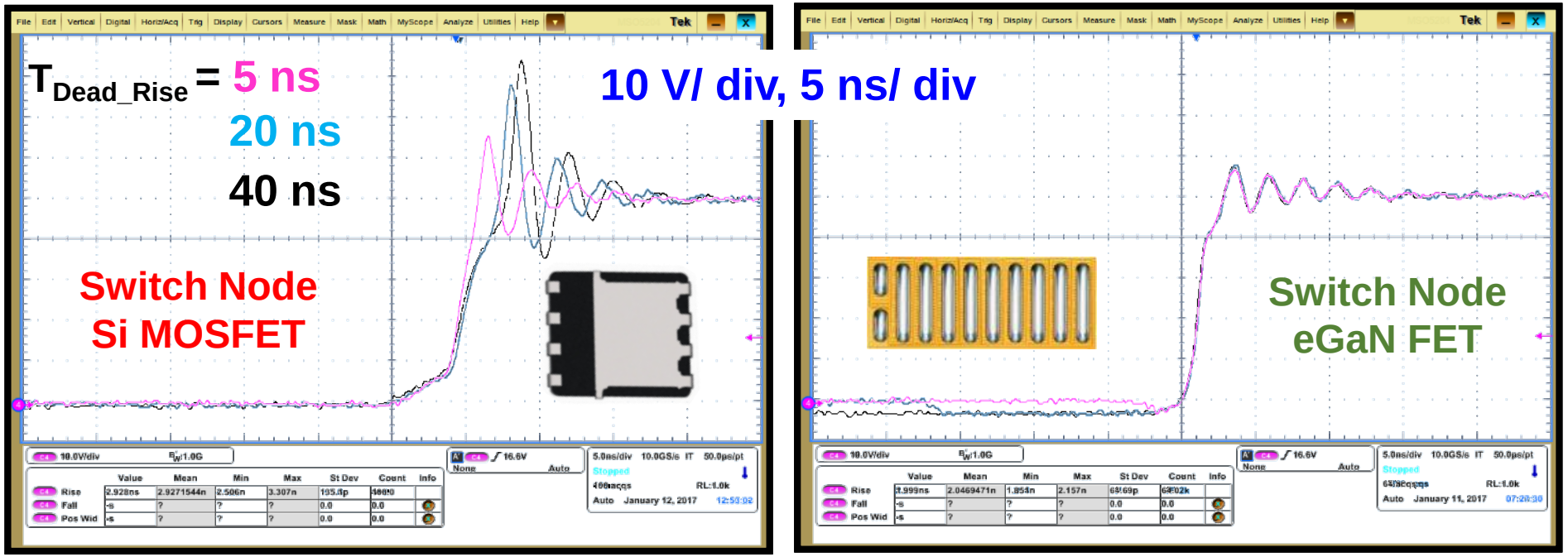
3 x 5 mm

Parameter	IPT111N20NFD (@ 10 V_{GS})	EPC2215 (@ 5 V_{GS})	EPC2304 (@ 5 V_{GS})
$R_{DS(on)}$ typ	9 mΩ	6 mΩ	3.4 mΩ
$R_{DS(on)}$ max	11.1 mΩ	8 mΩ	5 mΩ
Q_G typ	65 nC	10 nC	20 nC
Q_{GD} typ	8 nC	1.6 nC	3.2 nC
Q_{OSS} typ	162 nC	68 nC	68 nC
Q_{RR} typ	309 nC	0 nC	0 nC
Device Size	115.83 mm^2	7.36 mm^2	15 mm^2

15x smaller, less losses, no reverse recovery, higher f_{SW}

GaN FETs: Zero Reverse Recovery

- Higher hard-switching frequencies without penalty
- Lower switching distortion

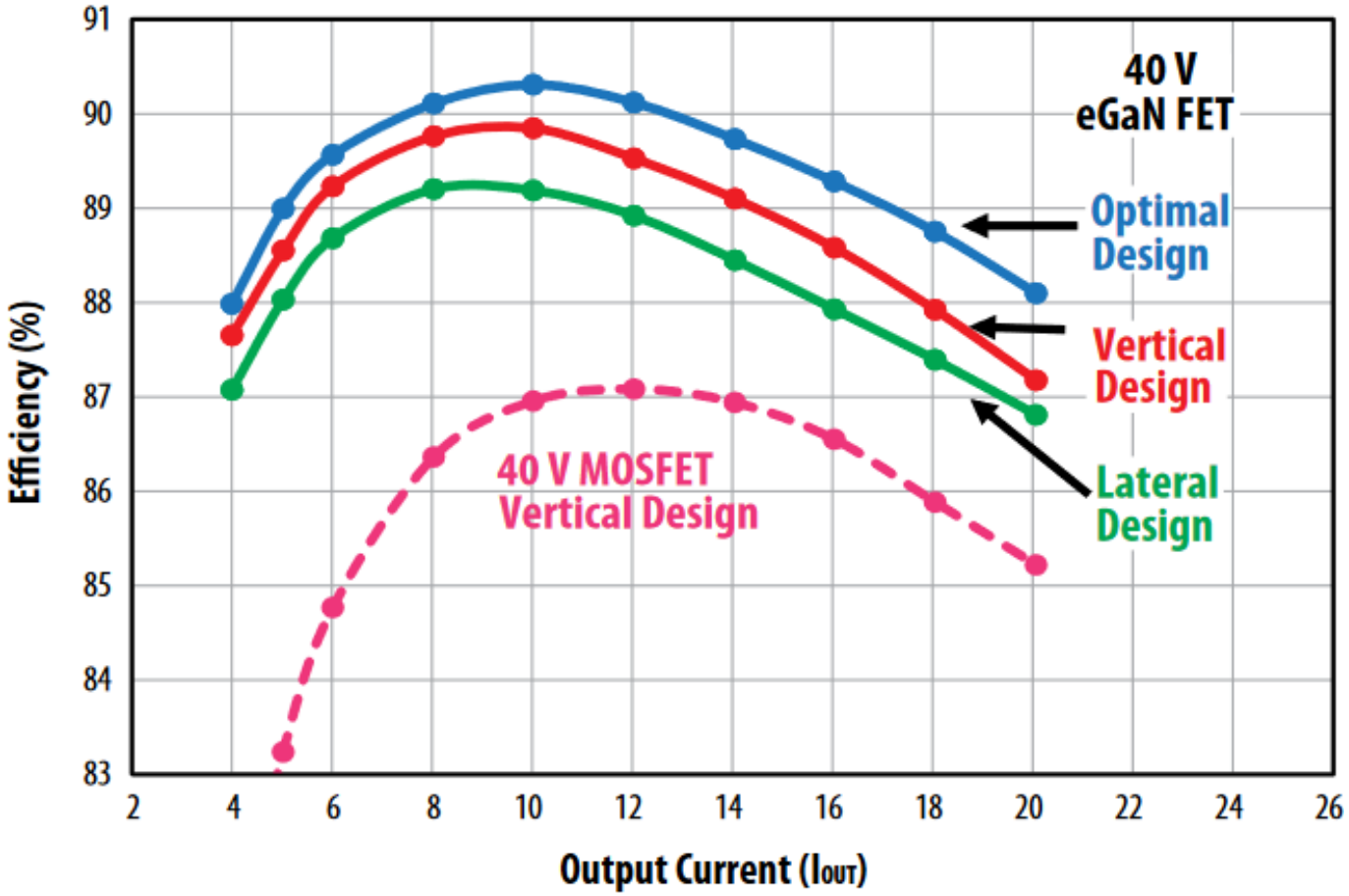


V_{IN} = 48 V, V_{OUT} =12 V, I_{OUT} = 20 A, f_{sw} = 500 kHz, L_{Buck}= 4.7µH

Layout

Layout - Efficiency

- Starting with results:
  - Solid lines: same EPC GaN FET
- Free efficiency improvement
  - Due to layout
  - Same schematic, same FETs



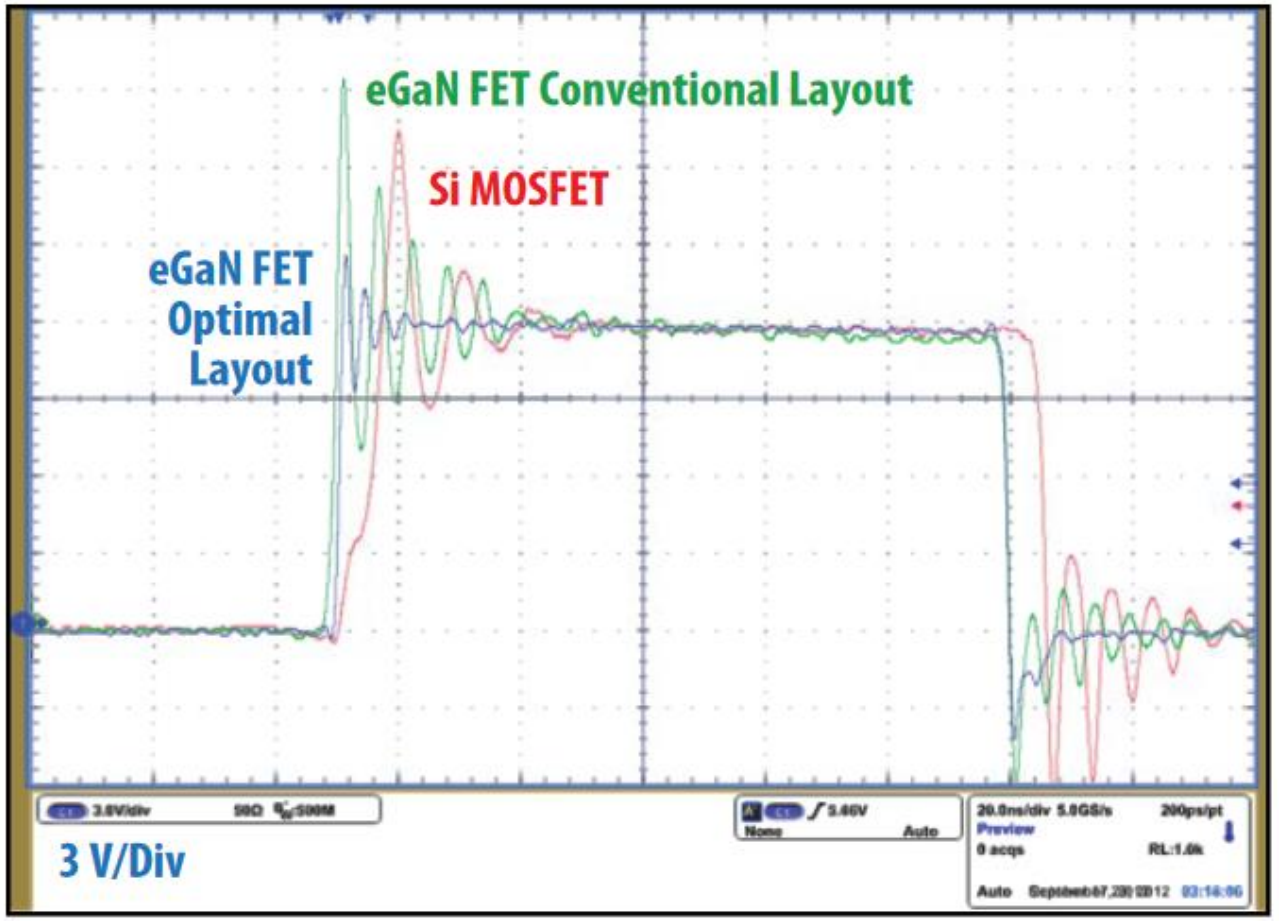
Buck converter, 1 MHz, 12 V to 1.2 V

App note link

Layout - Noise

- Starting with results:
  - Blue line and Green Line: same FETs, same schematic
  - EPC GaN FETs

- Free ringing improvement
  - Due to layout
  - MOSFETs don’t benefit as much…

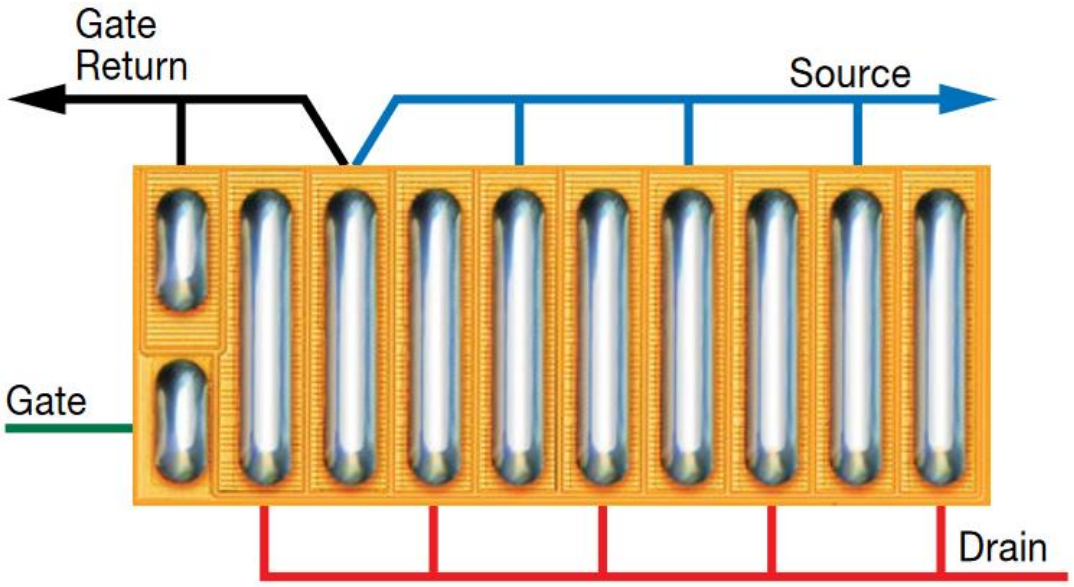


Buck converter, 1 MHz, 12 V to 1.2 V

App note link

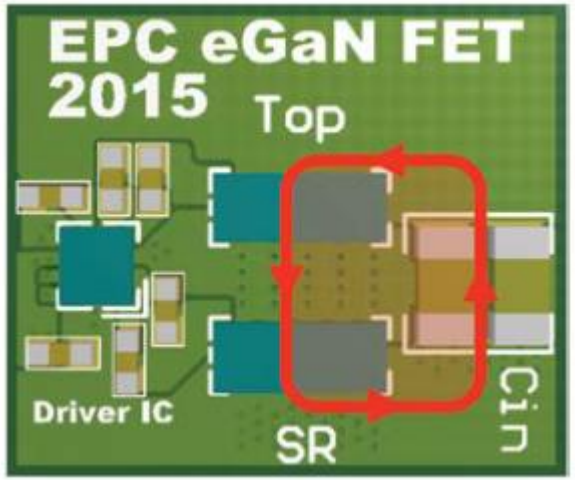
Layout – How?

- “Secret”: minimizing the loop inductances
  - power loop, gate loop
- Easier said than done?
- Not too difficult, because GaN FETs are:
  - Small: less board area
  - Lateral devices: active area near PCB, and no bond wires
  - Pins on GaN FETs help

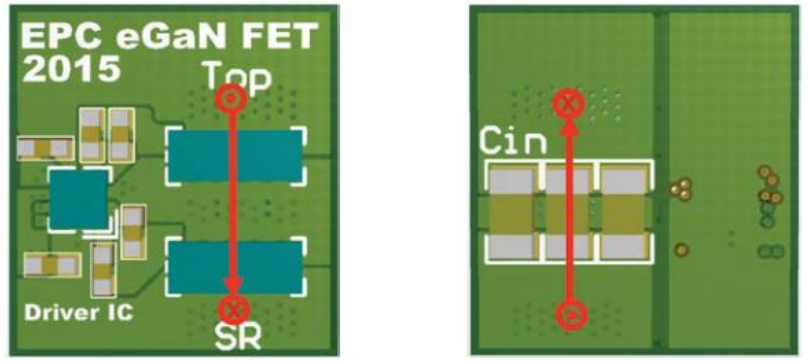


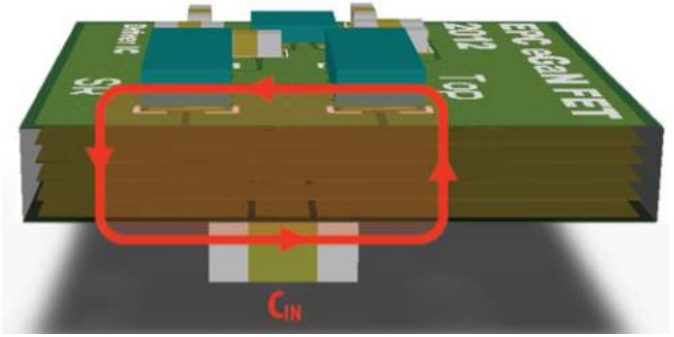
Layout – How?

- Layout options:
  - Conventional Lateral Loop



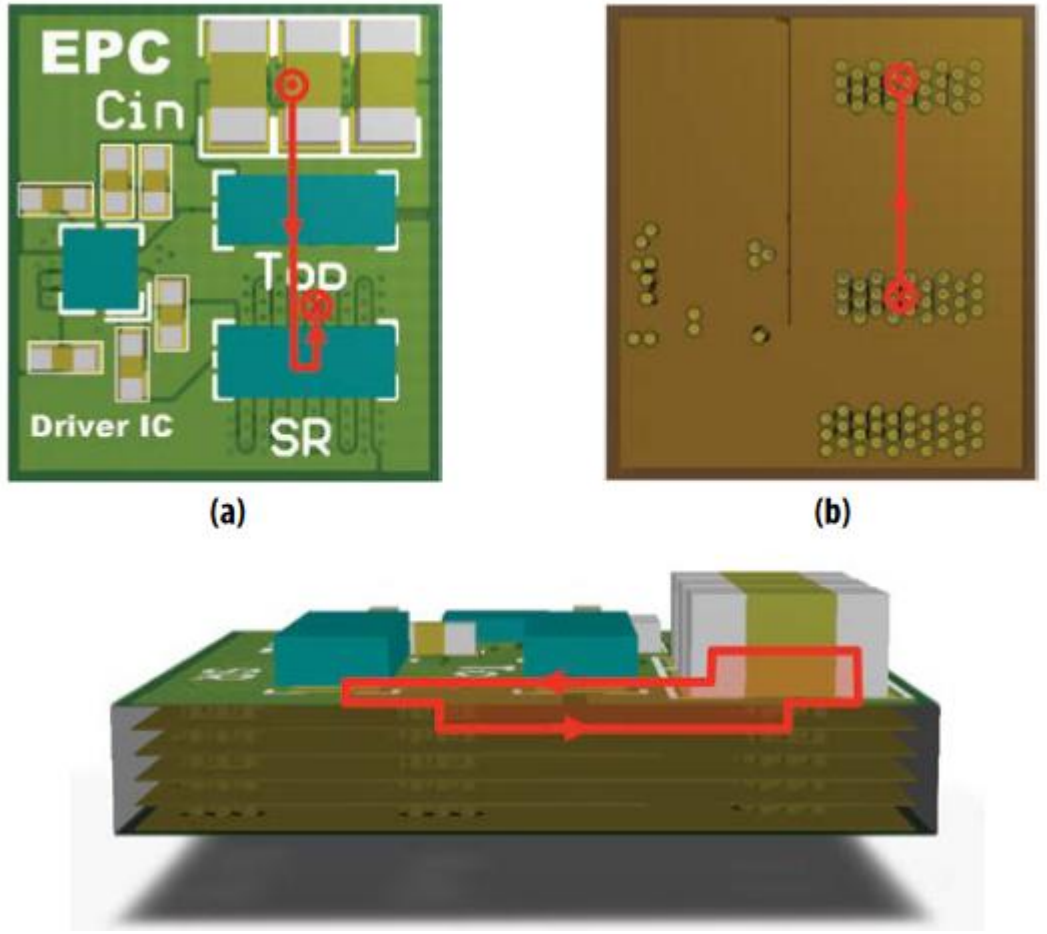
  - Conventional Vertical Loop





Layout – How?

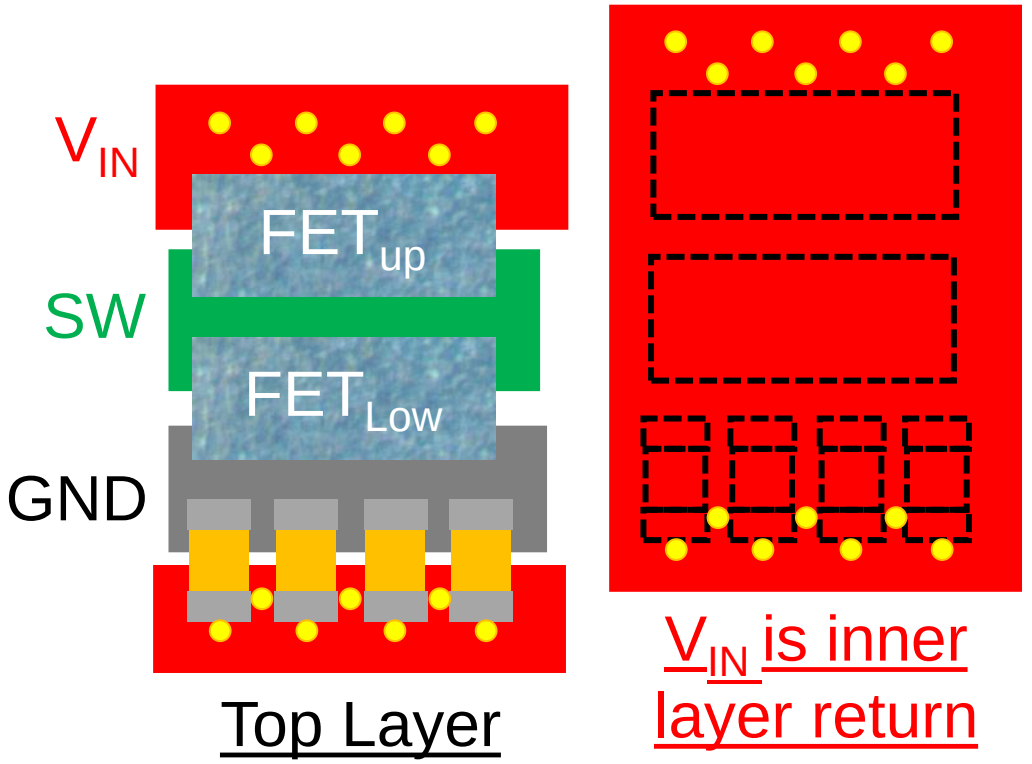
- Layout options:
  - Optimal Power Loop
  - Top View, (a):
    - Current path is a straight line
    - But, what about return current?
  - First inner layer
    - Ground return
  - Side View:
    - Minimal loop lateral *and* vertical



app note link

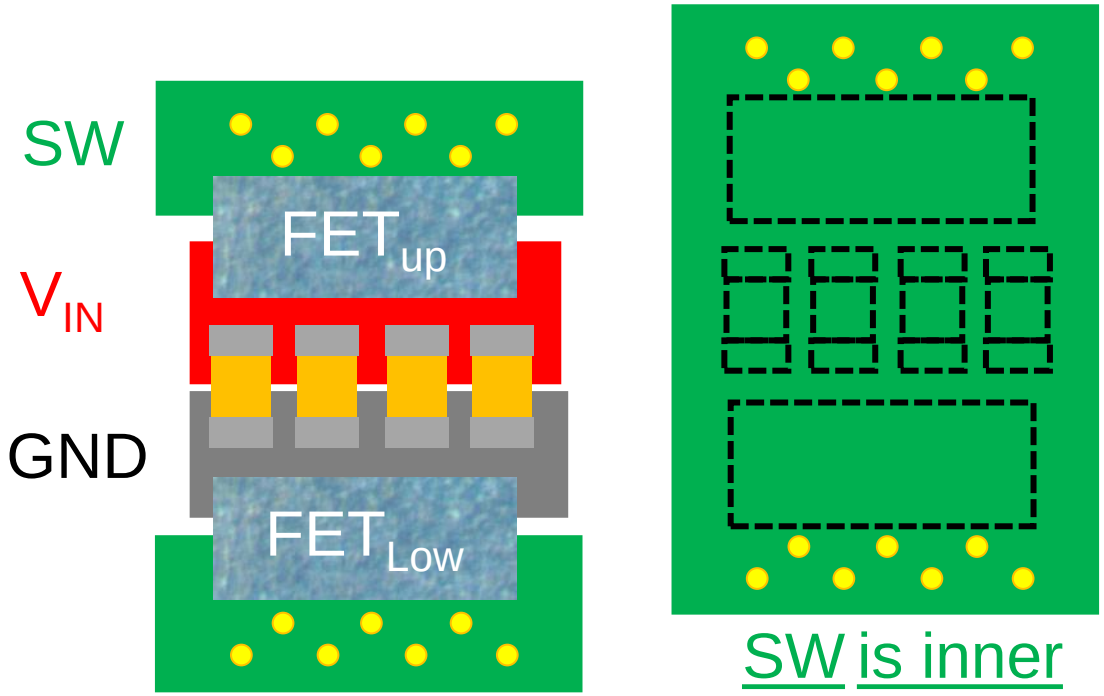
Layout – Variations

- Variations on the Optimal Layout
- Half bridge is a current loop circle of 3 components:
  - Top FET
  - Bottom FET
  - Capacitor(s)
  - So: 3 variations (so far…)
- “Rotate” the loop:
  - Vin buried (first inner layer)
    - Good for top FET cooling



Layout – Variations

- Variations on the Optimal Layout
- “Rotate” the loop, 3rd option:
  - Switch node buried (first inner layer)
    - Reduces E-field EMI
    - Capacitors in the middle



Top Layer

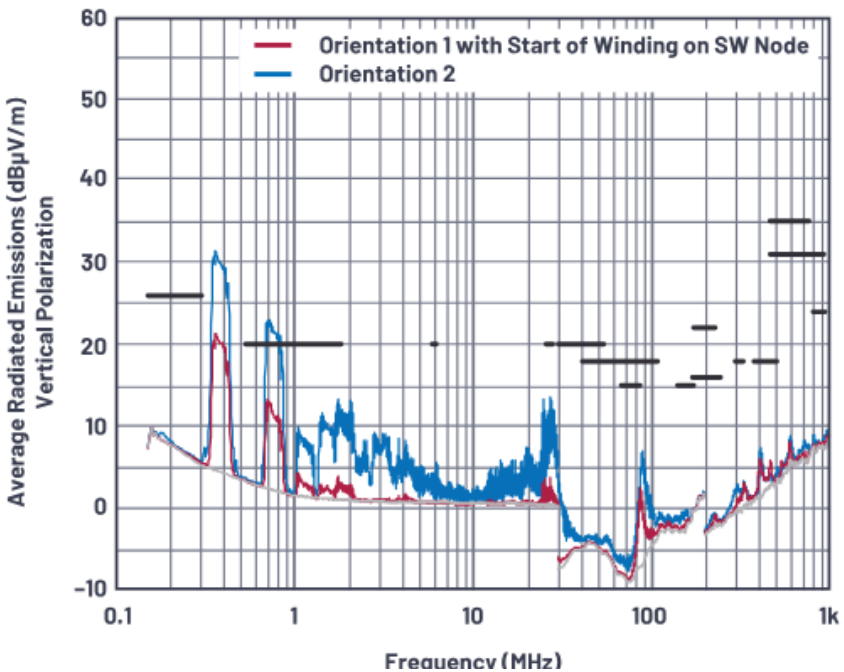
SW is inner layer return

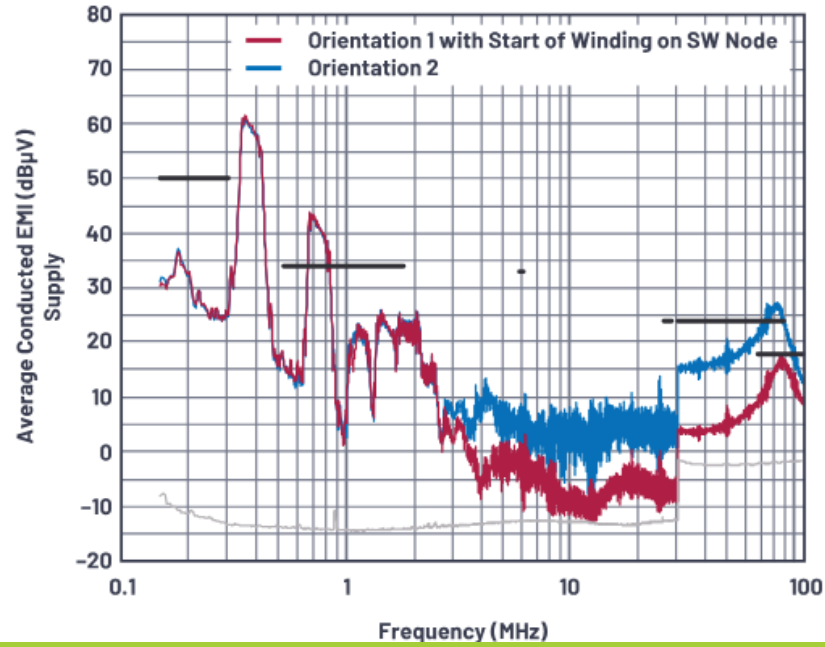
Bus capacitors between the FETs

Layout – System

- How about the Inductor?
  - dv/dt
  - Wurth: polarized inductor
    - Input = switch node → close to PCB / ground
    - Output = DC level → “up in the air”
    - Flatter inductors help

Figure 6: WE-XHMI and WE-PD2 with the 'dot' identifying the location of the start of the winding.





Source: Analog Devices, test of Wurth 74439346150 high performance inductor; Link

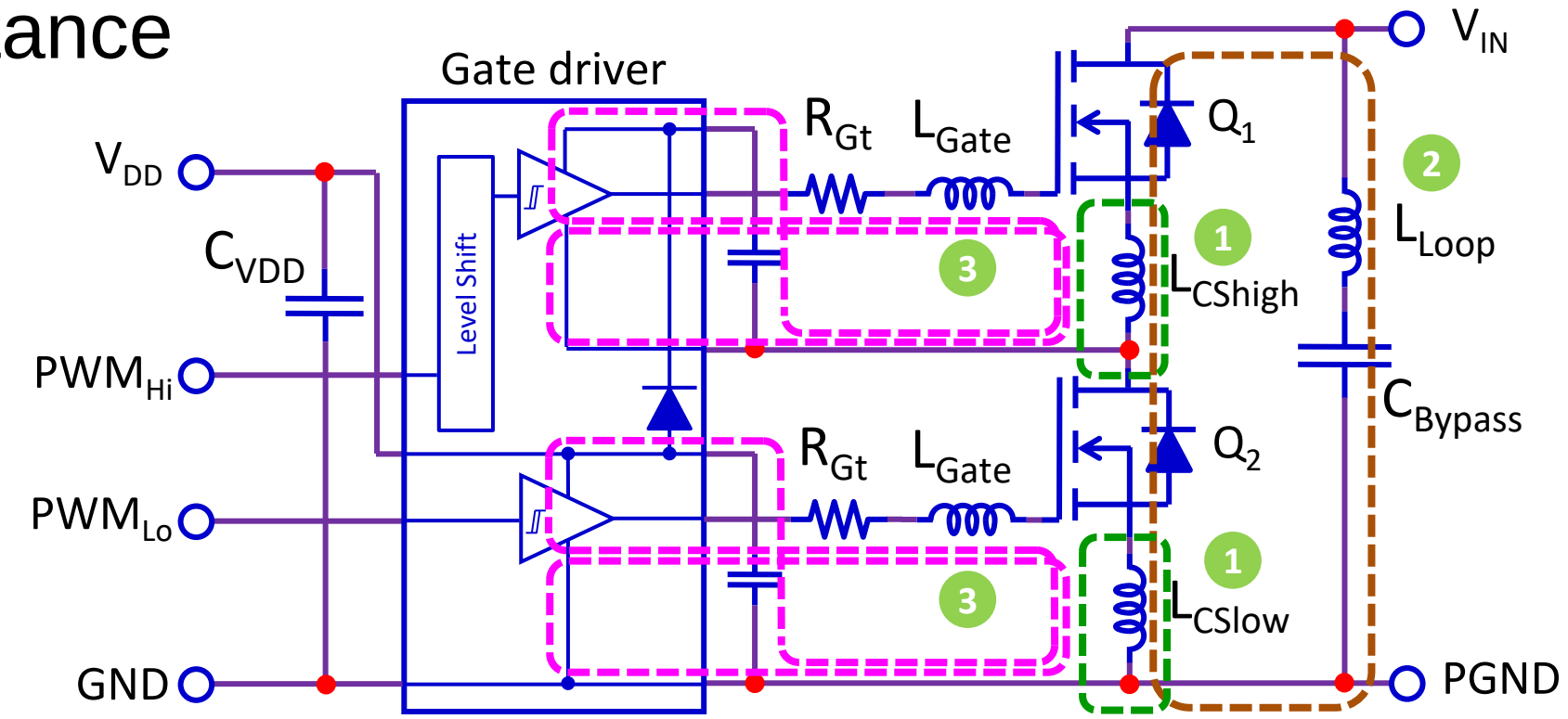
Parasitic inductances

1. Common source inductance
2. Power loop inductance
3. Gate loop inductance
   - Turn-on
   - Turn-off

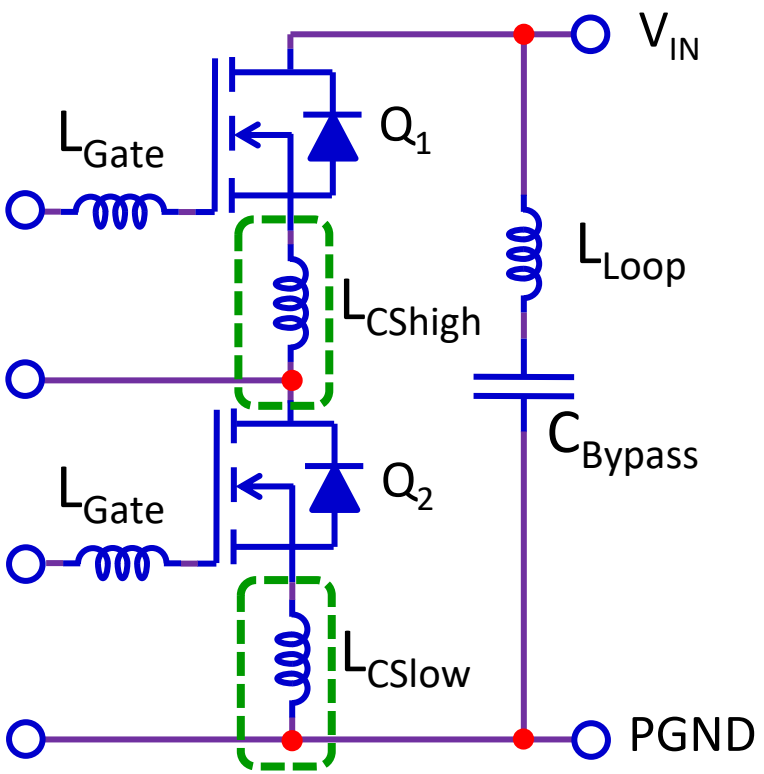
[WP010: Optimizing PCB Layout](#)

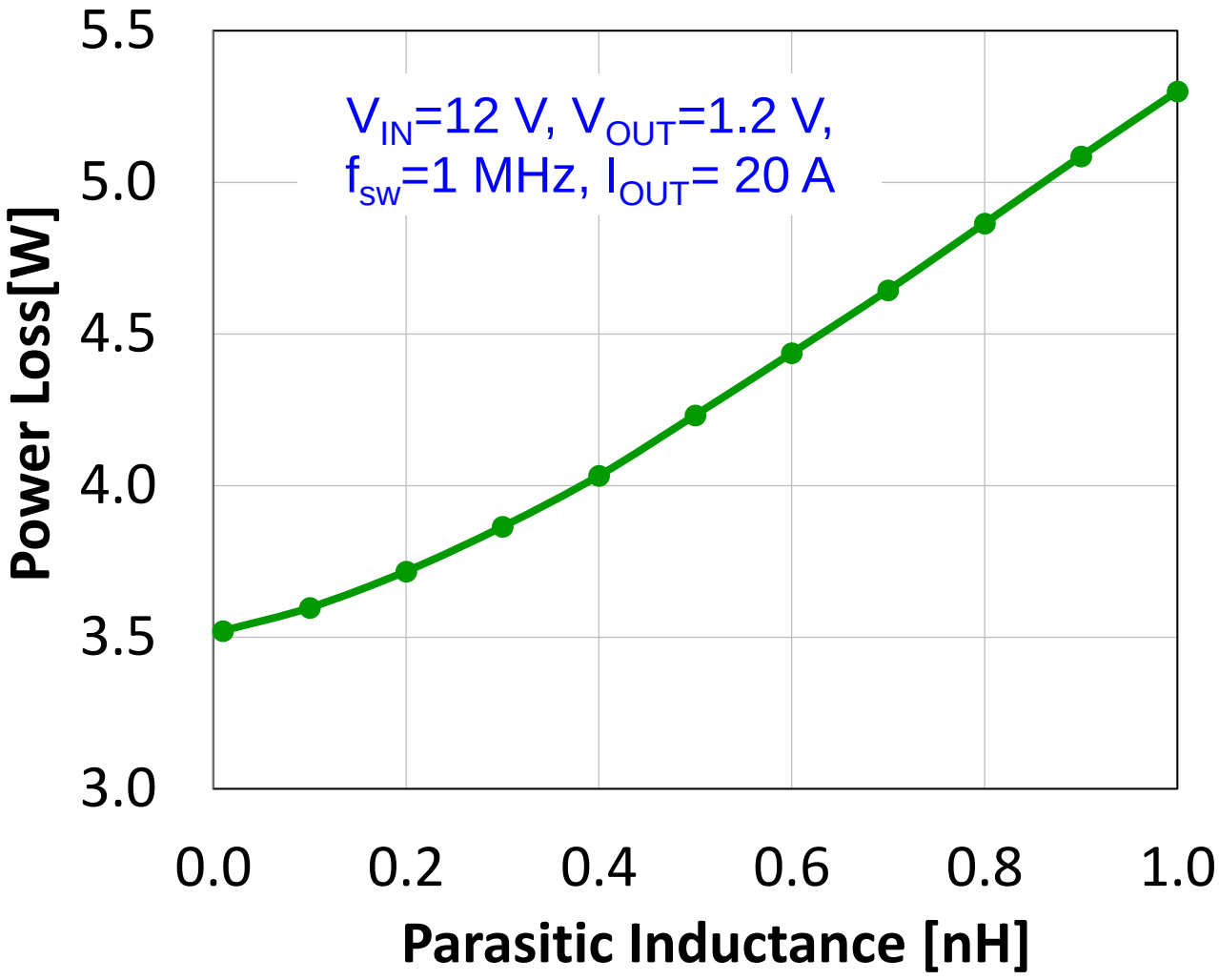
[How to GaN 05](#)

[How to GaN 05a](#)

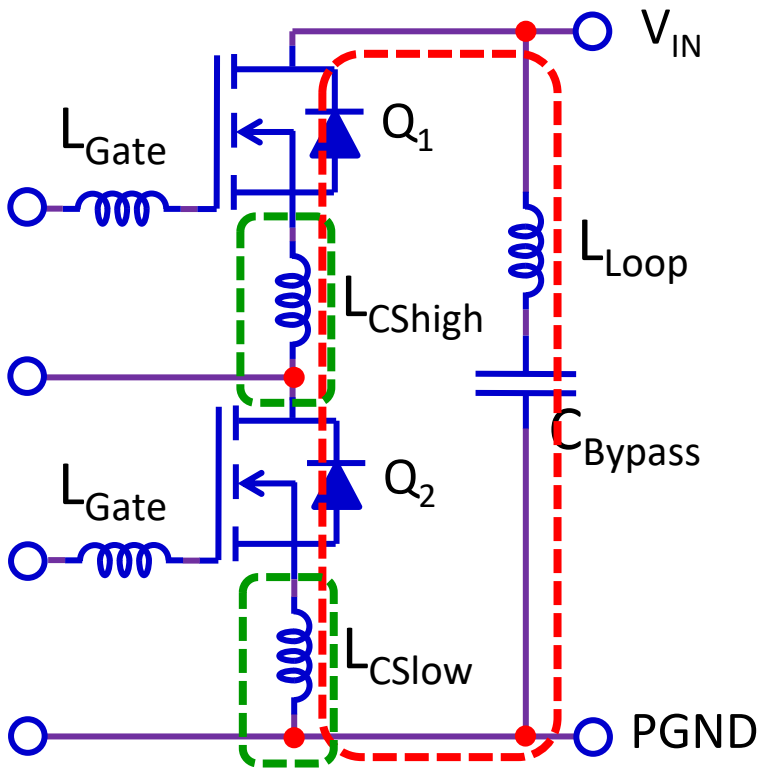


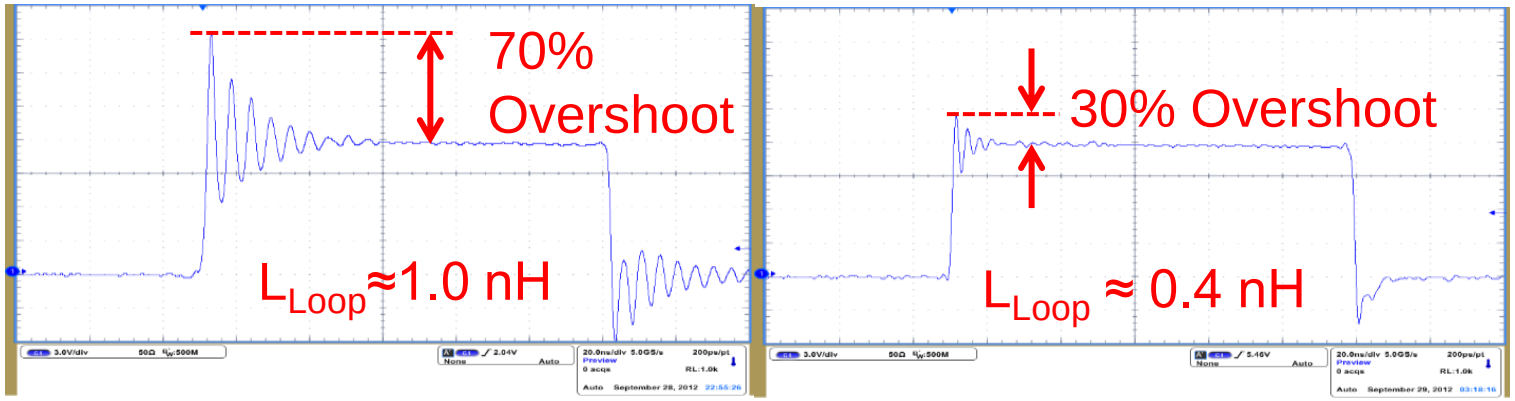
Impact of Common Source Inductance

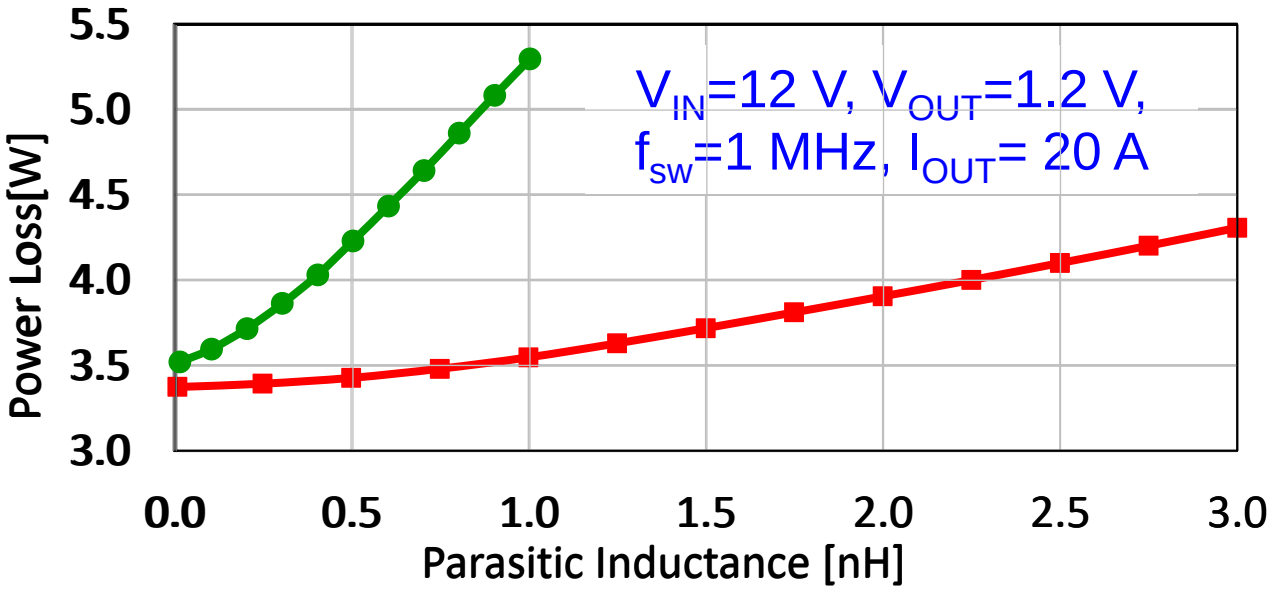




Impact of Power Loop Inductance

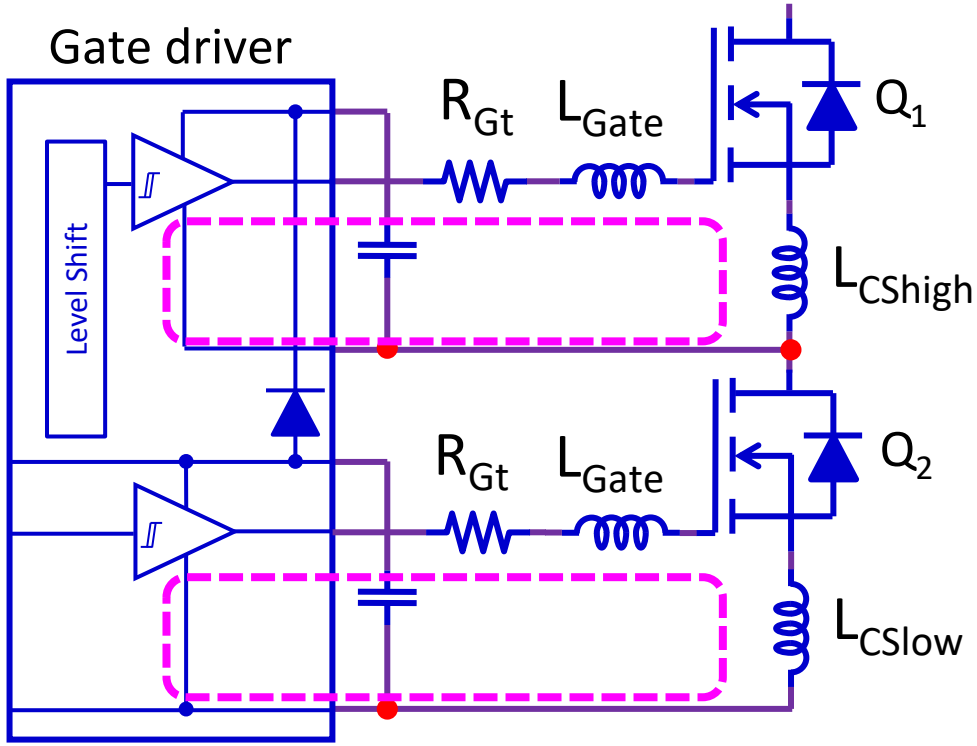




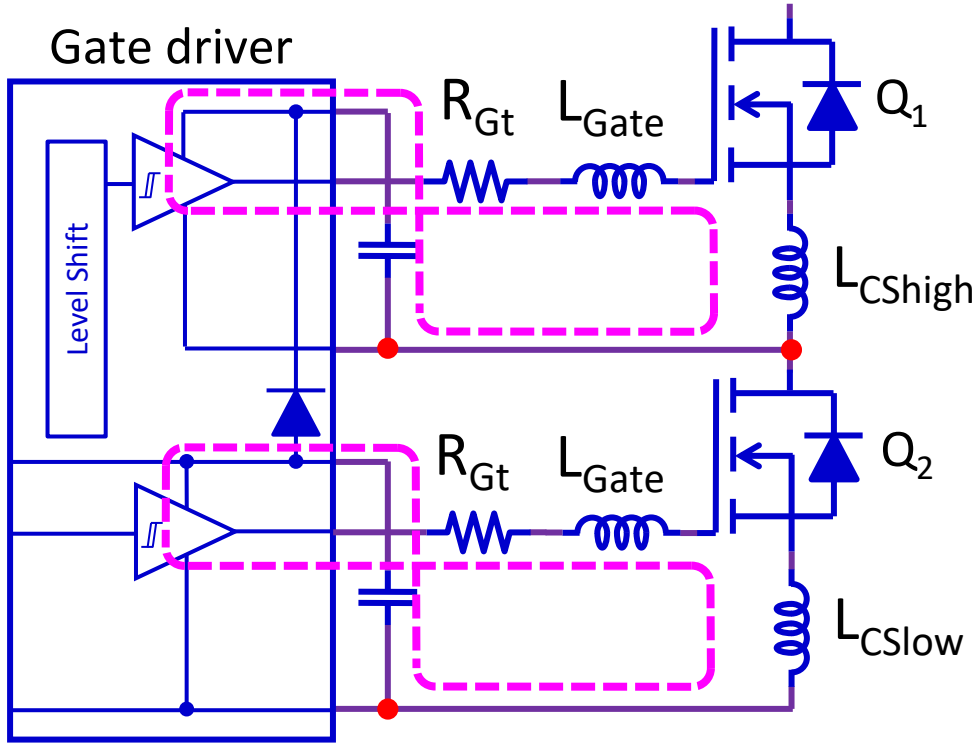


Impact of Gate Loop Inductance

- Two loops to consider: Turn-on & Turn-off
- L_{Gate} requires R_{Gt} to damp ringing overshoot
  - slows transition

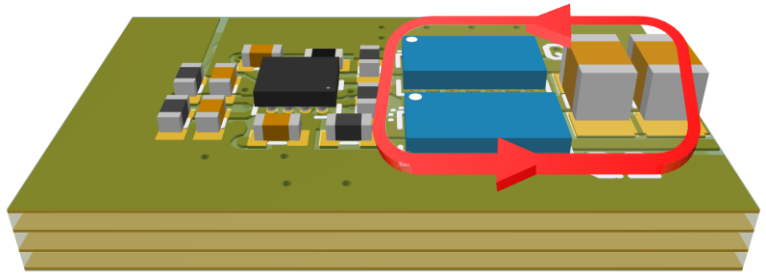


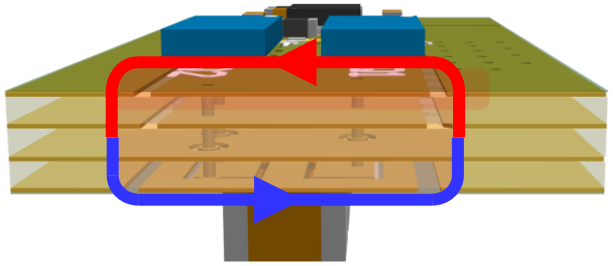
Turn Off

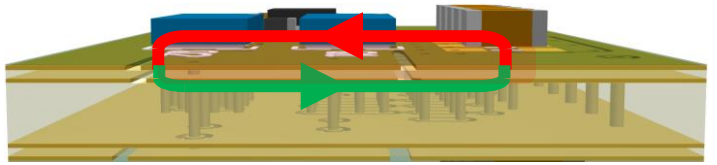


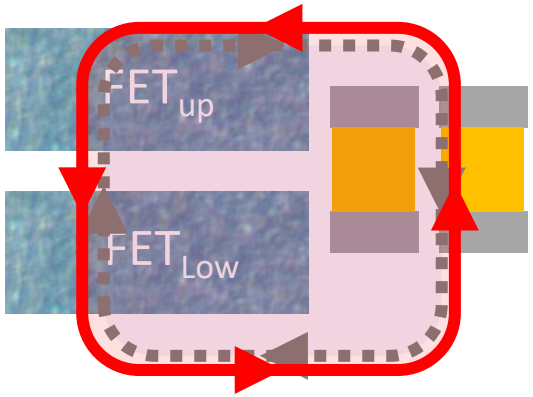
Turn On

Layout Comparisons

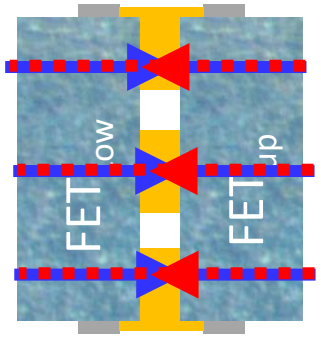






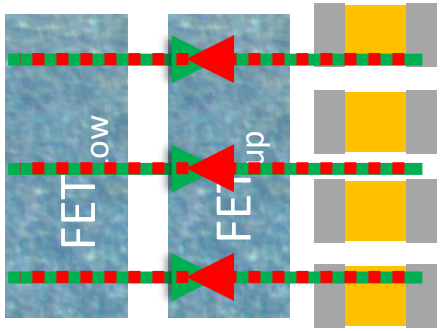


Top Layer
Mirror (Inner Layer 1)



Top Layer

Bottom Layer



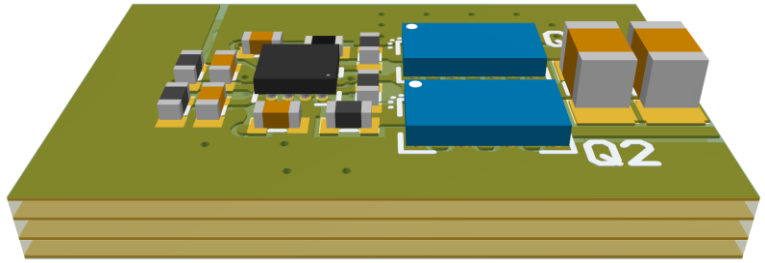
Top Layer
Inner Layer 1

Lateral

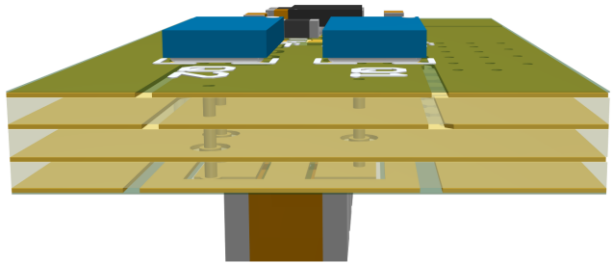
External Vertical

Internal Vertical

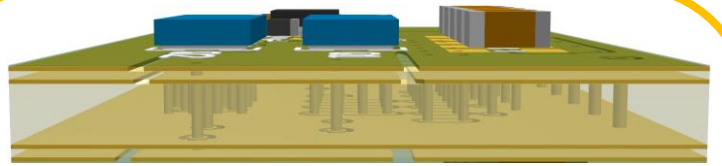
Layout Inductance Comparison



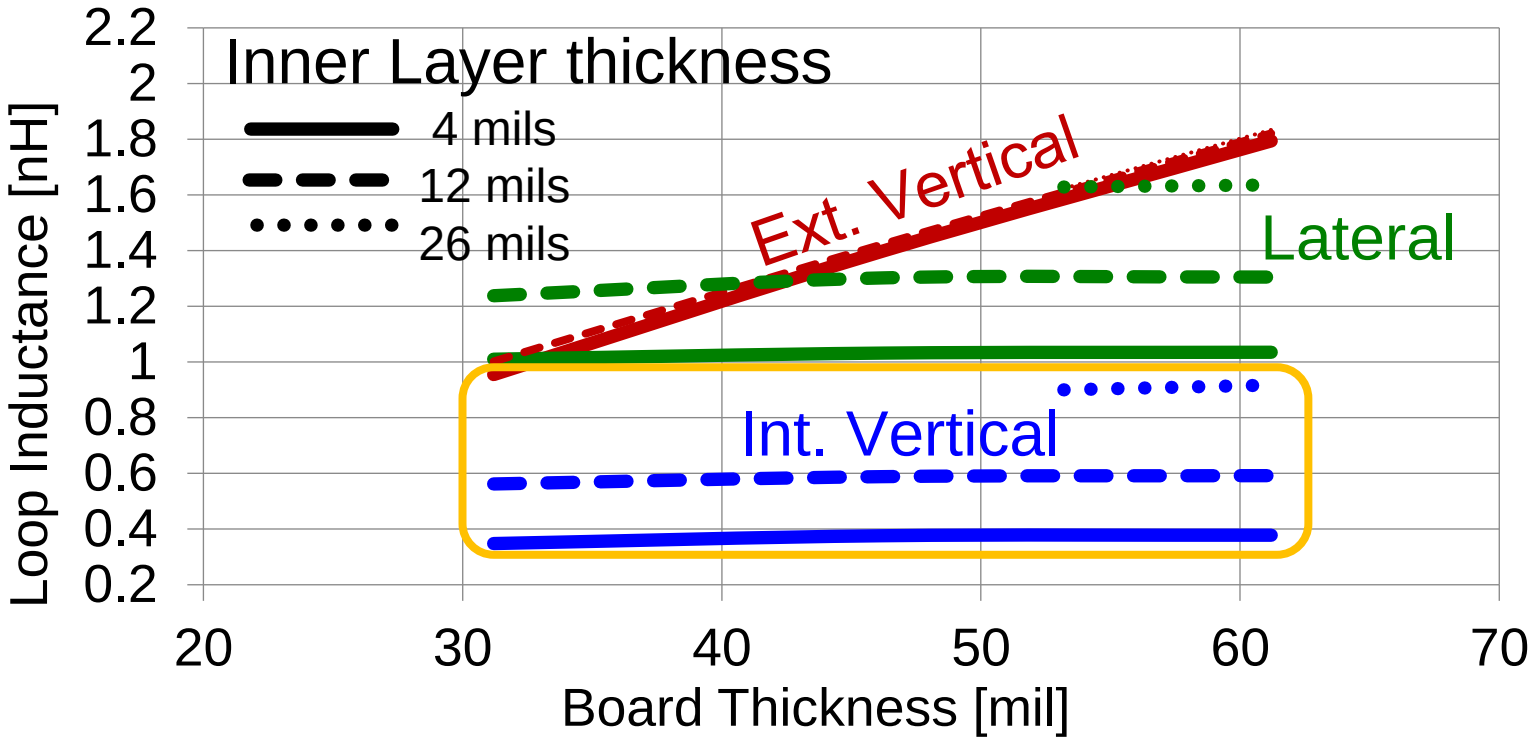
Lateral

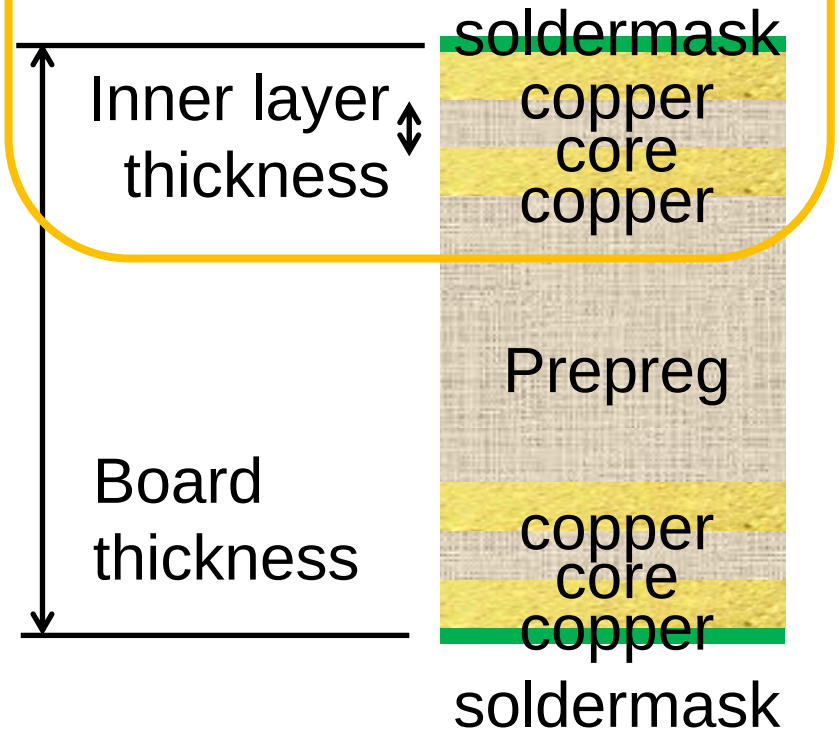


Ext. Vertical



Int. Vertical
Best Choice

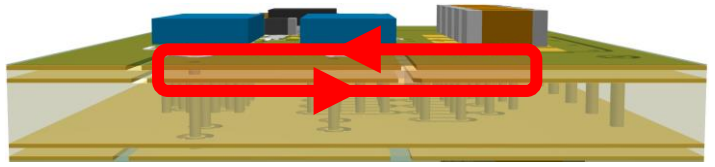




Designing a Low Inductance Layout

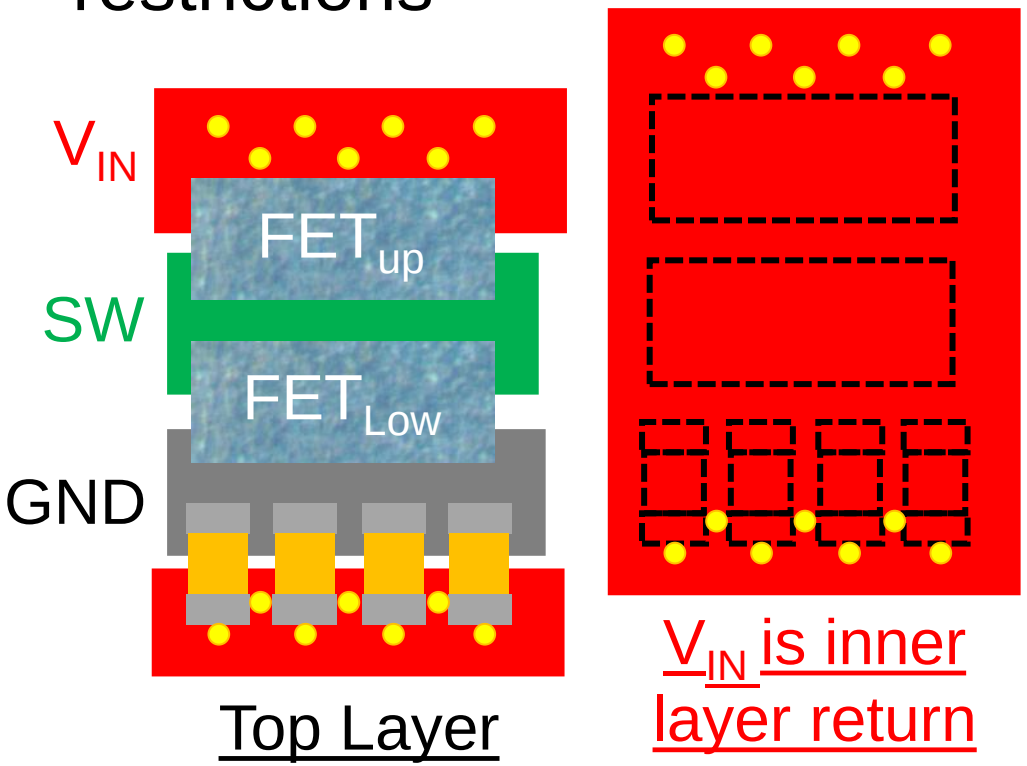
Internal vertical (optimal) power loop:

1. Pace components as close as possible
2. Place (many) vias as close to the innermost electrical connection
3. Thinnest permissible substrate thickness between outer and first inner layer
4. Spread out via connections at innermost connect
5. GND return does **not** need to carry the full current



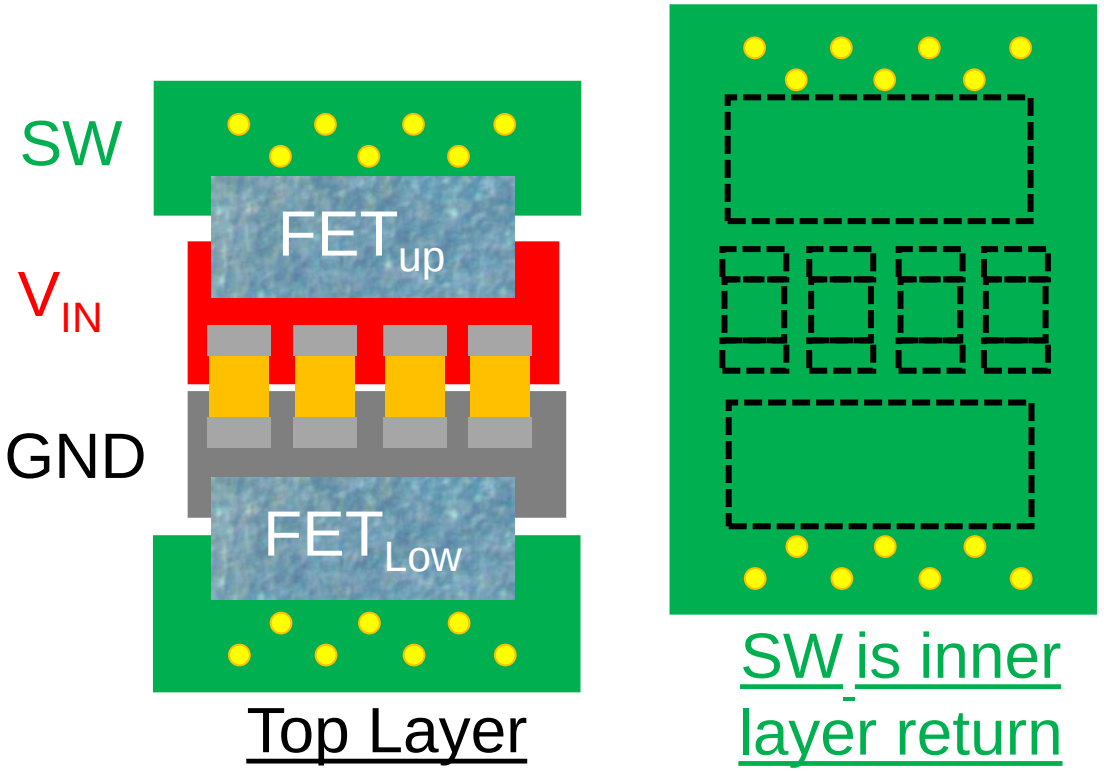
Alternative Layout Configurations

- Improves cooling for upper FET
- Useful for specific layout restrictions



Bus capacitors beside lower FET

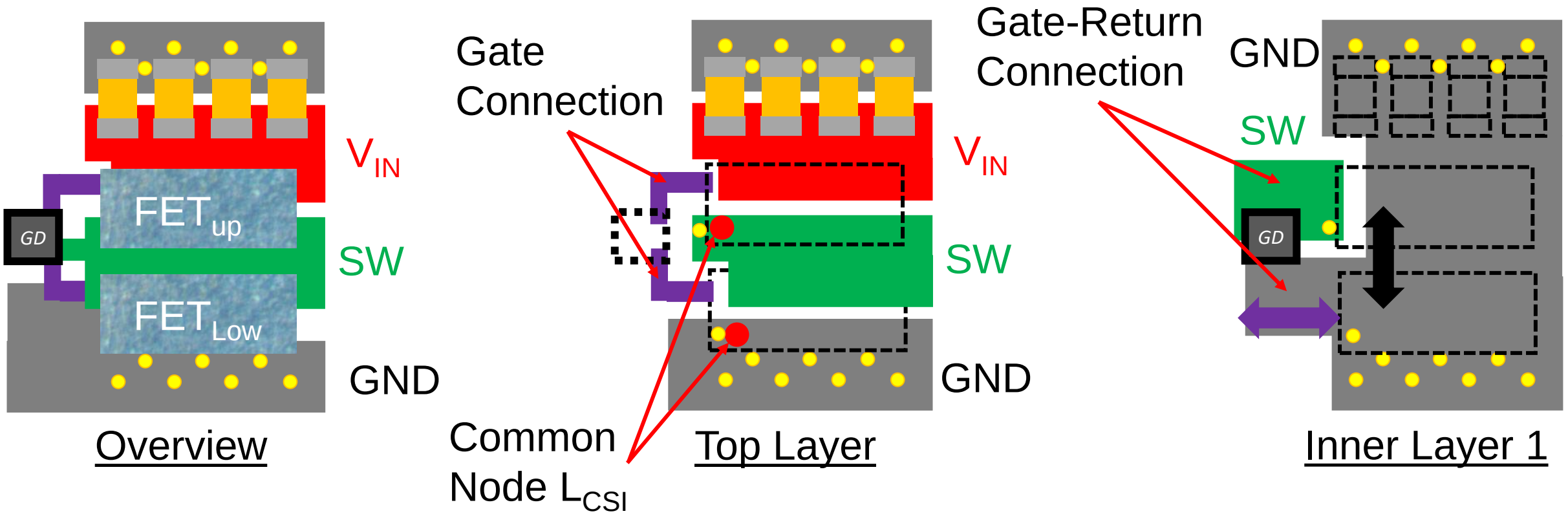
- Buries SW-node inside the board
  - Reduces E-field EMI



Bus capacitors between the FETs

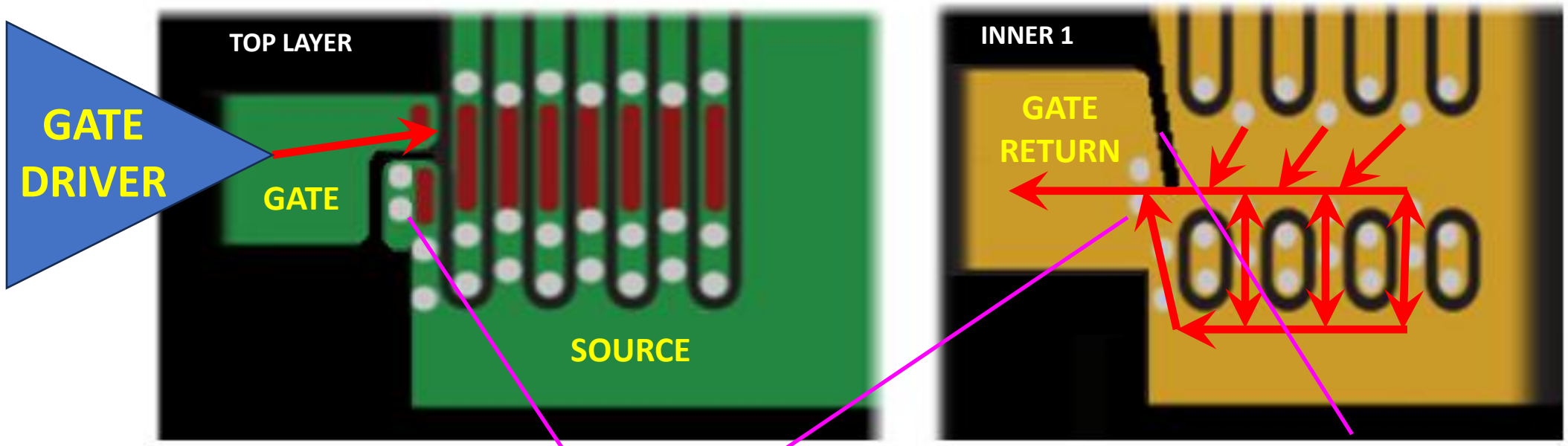
What About the Gate Connection

- Gate drive track with return polygon (its source!) on next layer
- Orthogonal gate to power connection reduces coupling between them



To Kelvin or not to Kelvin?

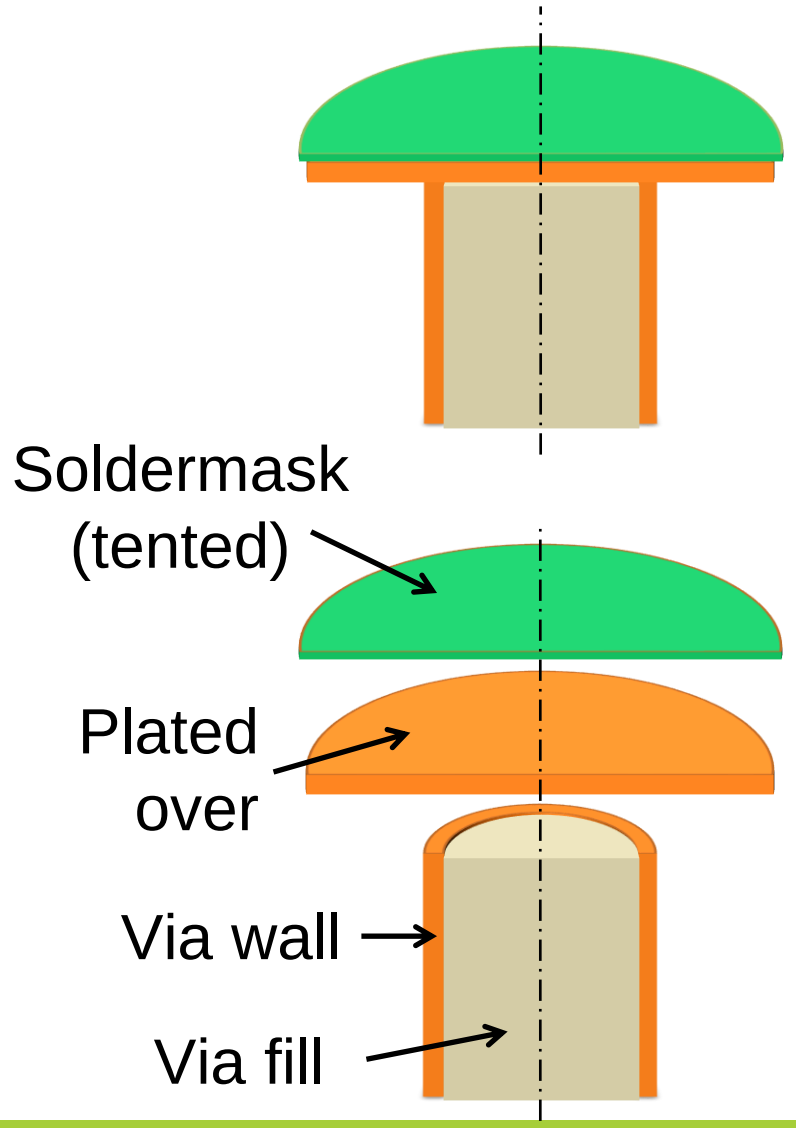
- Connect **ALL** the source pads together
- place one or few vias near to the source pad closest to the gate pad
- those vias will be the only connection between power loop and gate return polygon: this is the Kelvin connection



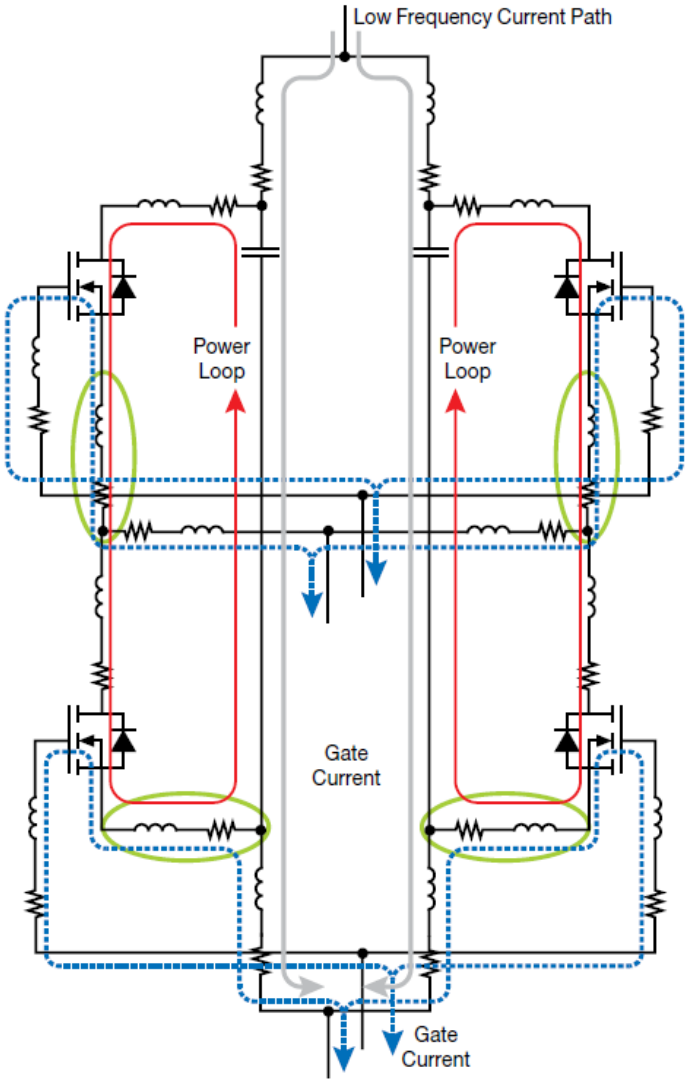
Via Construction

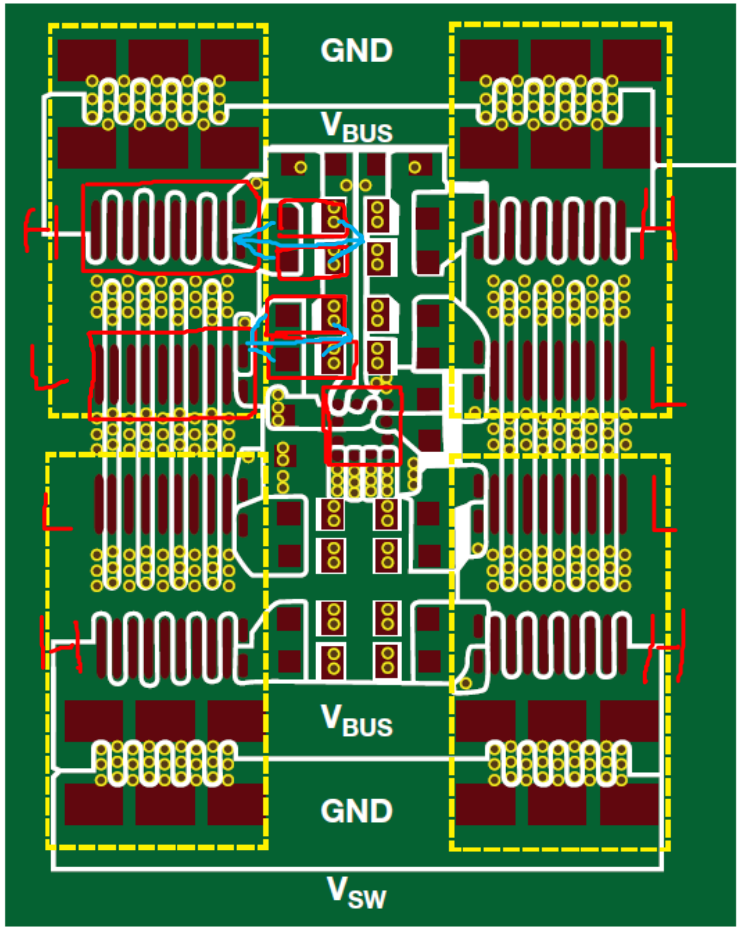
Via-In-Pad-Plated-Over (VIPPO)

- Wall thickness = 20 µm per IPC standard class 2
- Hole diameter (typical) = 0.2 mm
- Annular ring = 0.35 mm minimum
- Plated over
- Non-conductive filled
- Tented on both sides of the board
- Used for under bump and close to component pads
- Usable up to 2 oz (2.8 mil / 70 µm) copper thickness
- **IPC4761 Via Type VII**

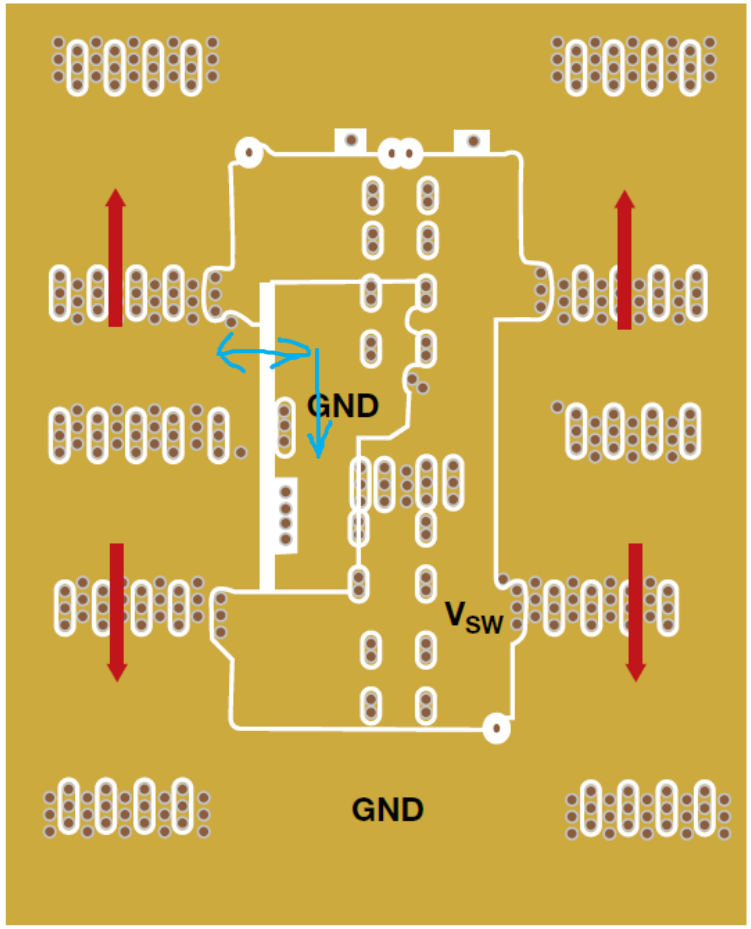


Layout – Parallel half bridges





(a) **Top layer**

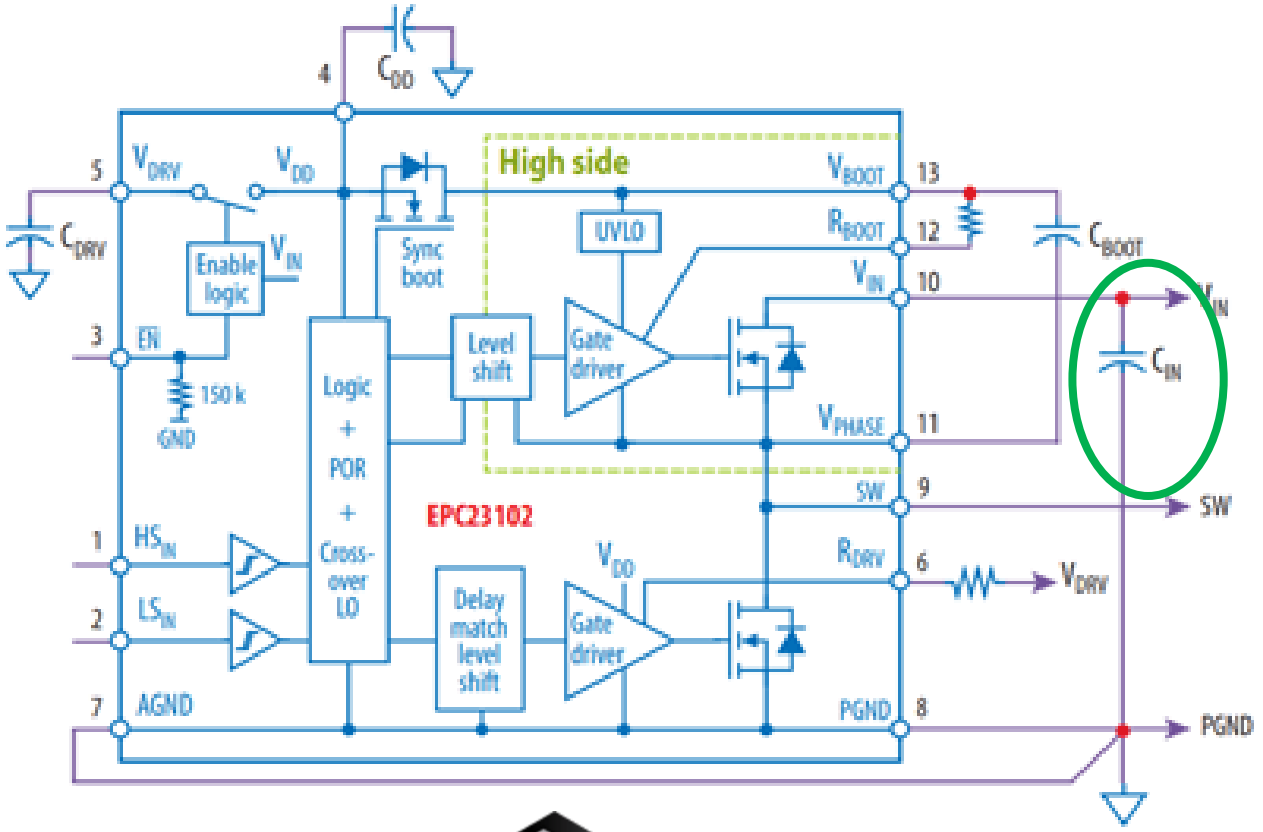


(b) **Second layer**

Layout Shortcuts
(how to cheat)

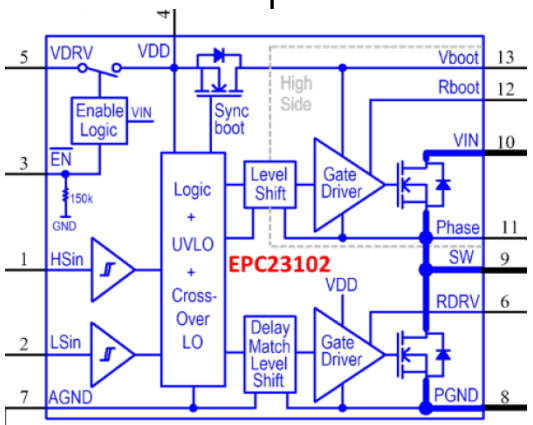
Shortcut #1

- Want to avoid most of the Power Loop and Gate Drive layout?
  - Yet get the benefits of good layout?
- EPC's new Power Stages
- Gate drive: internal
- Power Loop: mostly internal
- Remaining: decoupling capacitor

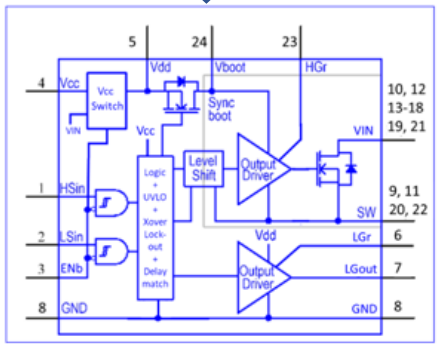


Power Stages in QFN

	EPC23102	EPC23103	EPC23104	EPC23101	EPC2302
V_{DS}	100 V	100 V	100 V	100 V	100 V
$R_{DSON\ (max)}$	6 mΩ	8 mΩ	10 mΩ	3.3 mΩ	1.8 mΩ
I_{DC}	35 A	20 A	15 A	65 A	101 A
Package	QFN 3.5mm x 5mm			QFN 3.5mm x 5mm	QFN 3mm x 5mm
Samples	Now	Now	Now	Now	Production



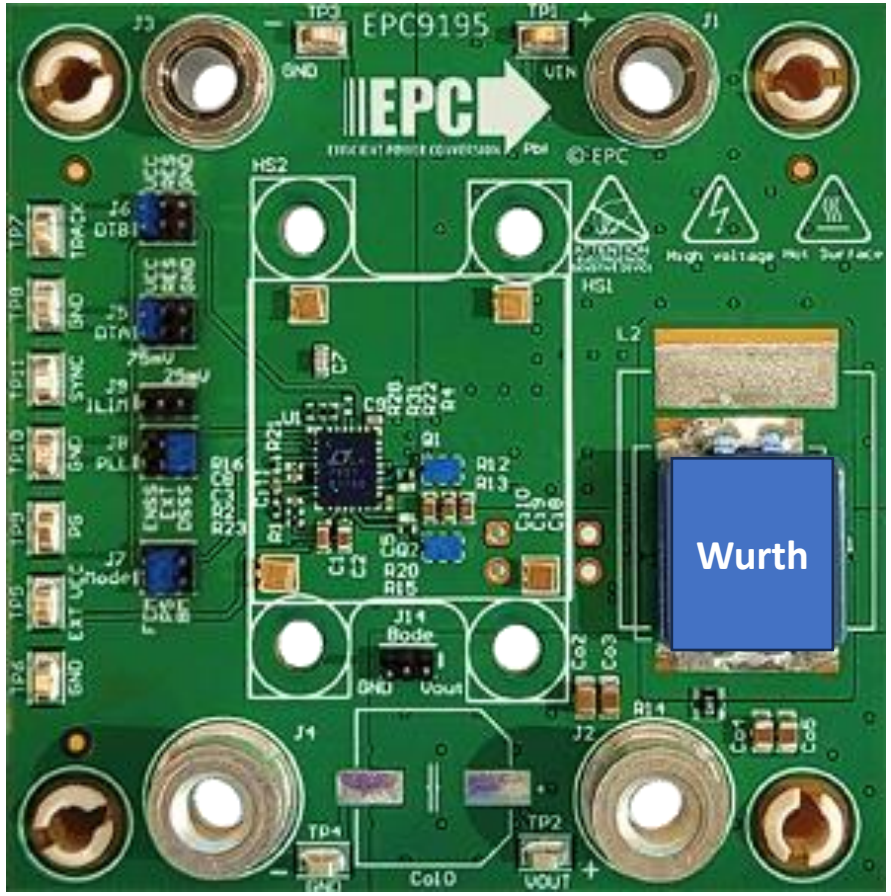
1 chip Power Stage



2 chip Power Stage

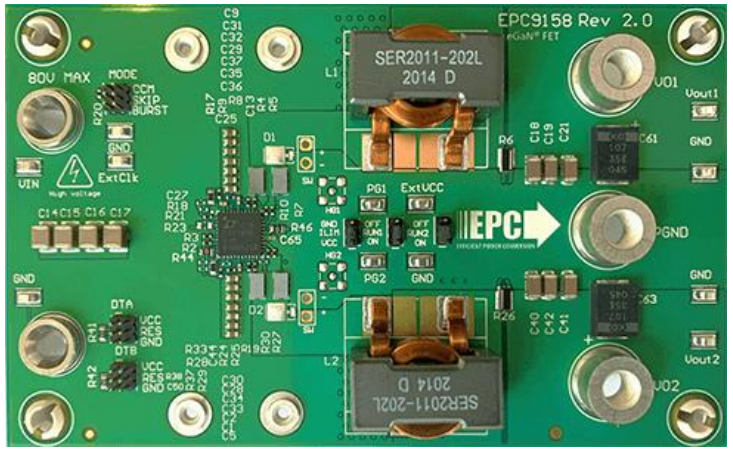
Shortcut #2

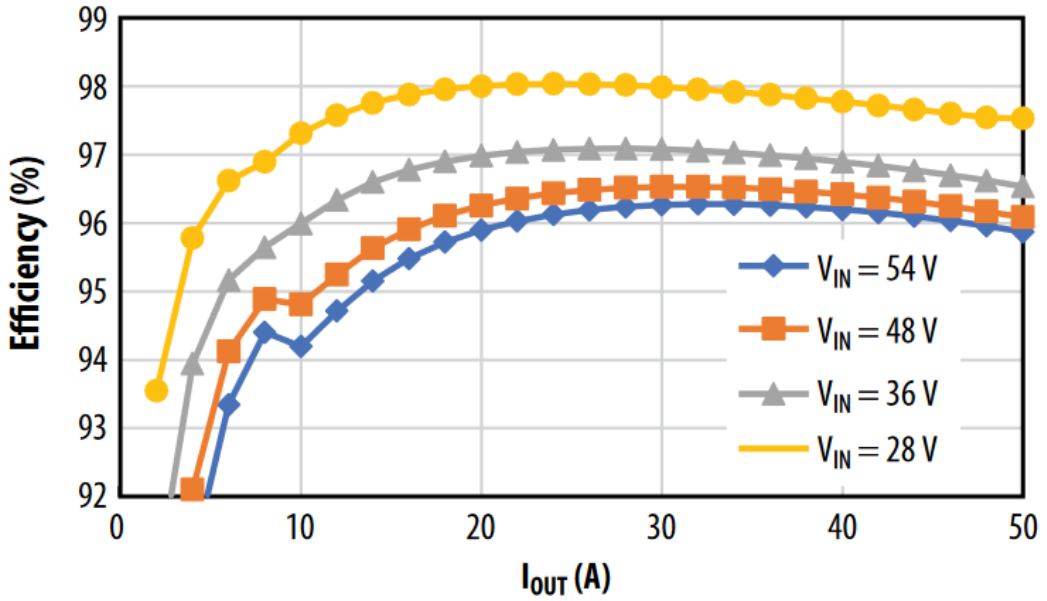
- Want to have a good layout, using discrete GaN FETs?
- Copy a reference design!
- Example: DC-DC
  - Board part # EPC9195
  - Input 36 – 60 V, output 13 V @ 16 A
- Online: Gerbers, schematics, etc.
  - Link to home page
  - Altium files available upon request



Buck Converter – ADI controller

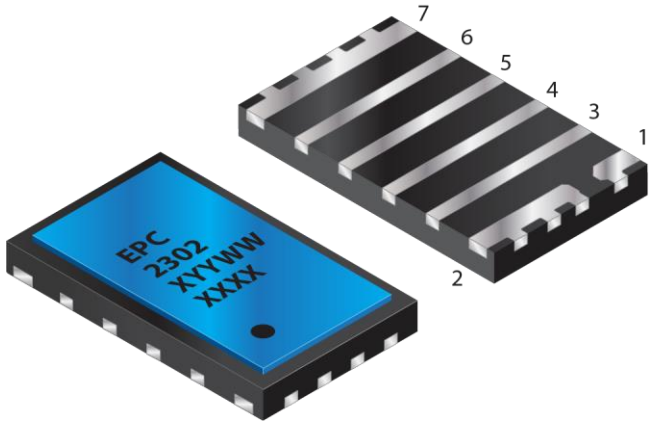
- EPC9158 -based
- 2-phase buck converter
- EPC9158: includes new, very efficient ADI controller
  - LTC7890
  - 500 kHz
  - Output power:
    - With FETs now on EPC9158 board: 600 W
    - FETs = Gen 5, EPC2218… better with Gen 6

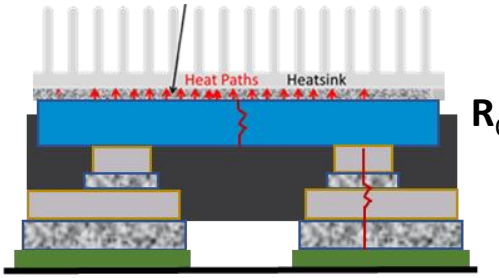




Other Topics

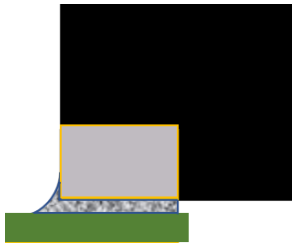
eGaN FETs in 3x5 mm QFN





R_{Θ},j-c (top)

R_{Θ},j-b (bottom) = 1.5 or 3 °C/W



Wettable Flanks

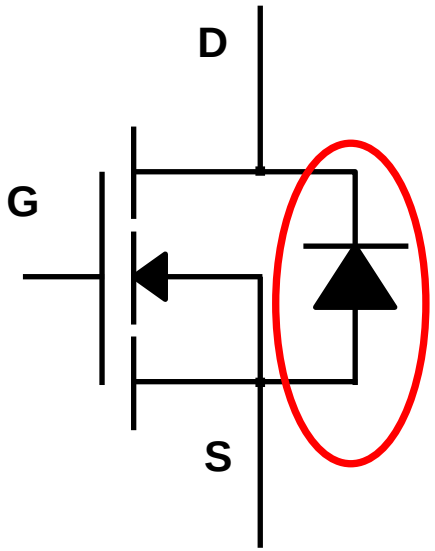
	EPC2361	EPC2302	EPC2306	EPC2305	EPC2308	*EPC2304*	*EPC2307*
V_{DS}	*100 V*	100 V	100 V	150 V	150 V	*200 V*	*200 V*
$V_{DS,\ transient}$	*120 V*	120 V	120 V	170 V	180 V	*240 V*	*240 V*
$R_{DS(on)}$ max		1.8 mΩ	3.1 mΩ	3 mΩ	6 mΩ		*10 mΩ*
$R_{DS(on)}$ typ	*1.0 mΩ*	1.4 mΩ	2.5 mΩ	2.2 mΩ	4.5 mΩ	*3.1 mΩ*	*8.2 mΩ*
Q_G typ	*28 nC*	23 nC	12.3 nC	22 nC	11.7 nC	*24 nC*	*10.6 nC*
Q_{GD} typ	*2.5 nC*	2.3 nC	1.1 nC	2.1 nC	1 nC	*2.5 nC*	*1.3 nC*
Q_{OSS}typ	*86 nC*	85 nC	44 nC	103 nC	50 nC	*116 nC*	*58 nC*
Q_{RR}typ	*0 nC*	0 nC	0 nC	0 nC	0 nC	*0 nC*	*0 nC*
$R_{\Theta JC}$	*0.2 °C/W*	0.2 °C/W	0.5 °C/W	0.2 °C/W	0.5 °C/W	*0.2 °C/W*	*0.5 °C/W*
I_D	*101 A*	101 A	62 A	102 A	63 A	*102 A*	*48 A*
Production	*Q2 2025*	**Now**	**Now**	**Now**	**Now**	*Q4 2024*	*Q4 2024*

note: preliminary specs in *italics*

rev. 9/19/2024
BDM

Synchronous Rectification

- Advantage of GaN FETs
  - Smaller
  - No reverse recovery (no Qrr)
  - Faster switching
- But what about EMI?



Synchronous Rectification

- dv/dt
  - But turn-on and turn-off of FETs at low voltage
- Ringing
  - No Crr (reverse recovery capacitance)
  - Shown to be an EMI concern for MOSFETs

- Size and Layout
  - Small size limits loop
  - GaN is lateral: active area nearest the board

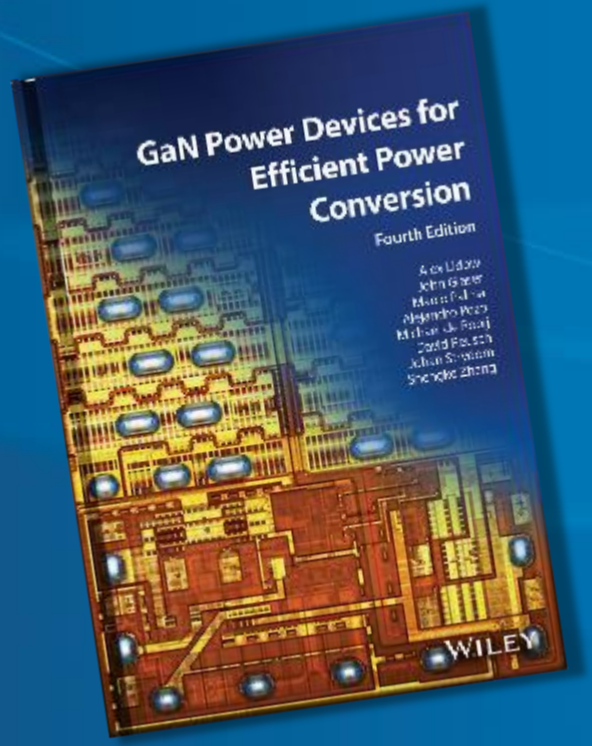
Summary

- Advantages of GaN FETs
  - Small, for good board placement
  - Lateral device, for current closer to the board
  - Higher frequency, for smaller EMI filters
  - No reverse recovery charge (no Qrr)
- Optimized Layout Benefits
- Layout Details
- Shortcuts: GaN power ICs, EPC reference designs

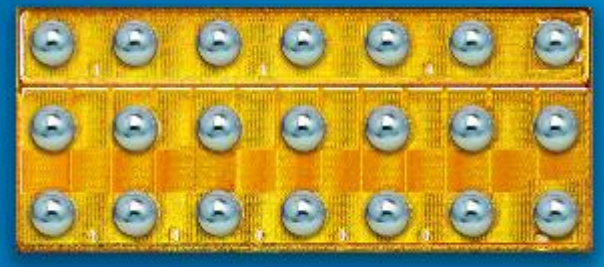
EFFICIENT POWER CONVERSION

Click on images to learn more

How To GaN Video Series

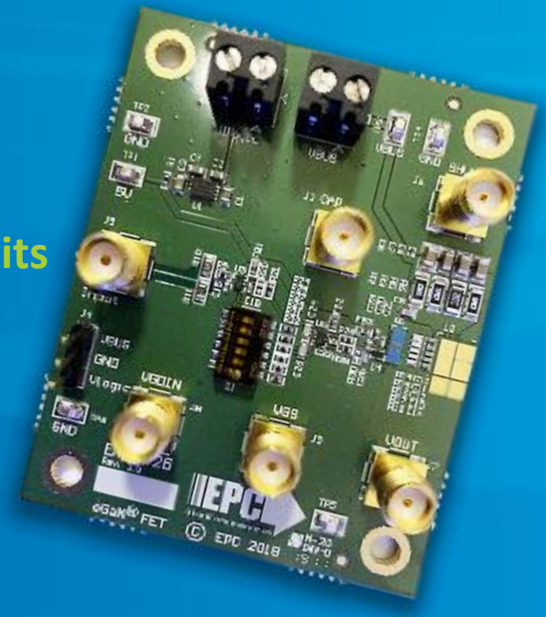


4th Edition Textbook



eGaN® FETs and ICs

Evaluation Kits



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