SEMINAR INVITATION

on 4th & 6th February 2025
in Son & Leuven

Partner:

LATTICE SEMICONDUCTOR

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

INVITATION TO THE SEMINARTOUR ON 4TH & 6TH FEBRUARY 2025 IN SON & LEUVEN

Advanced Techniques for designing FPGA systems, interfaces and power supply design: Efficiency and EMI optimizations!

Are you facing challenges in implementing 10Gbit data systems with FPGAs? Concerned about thermal noise impacting performance? We're here to help you tackle these issues and get your product to market efficiently!

Presented by:
Lattice Semiconductor – Leaders in low-power programmable solutions
Würth Elektronik – Experts in electronic and electro-mechanical components

What You'll Learn:
- FPGA Efficiency: Discover how FPGAs developed on the Lattice Nexus™ platform achieve a 100x lower Soft Error Rate (SER) and up to 75% lower power consumption ideal for safety-critical industrial and communication applications.
- Power Solutions: Gain insights into developing robust power module solutions tailored for FPGA systems.
- Ethernet applications: gain inside in timing, signal Integrity and Layout Techniques.

Why Attend?
- Expert Insights: Learn from industry leaders about best practices and innovative solutions.
- Q&A Session: Have your specific questions answered by experts in the field.
- Networking Opportunities: Connect with peers and industry professionals to share knowledge and experiences.

Date and locations:
This seminar takes place at the office from Würth Elektronik in Son (Eindhoven) on the 4th of February 2025 and in the Park Inn hotel in Leuven on the 6th of February 2025.

Please register by 21th of February 2025 as the number of participants is limited. You can find the registration here: www.we-online.com/seminar-registration

We look forward to seeing you there and helping you elevate your projects to new heights!

Kind regards,
Yours Lattice Semiconductor and Würth Elektronik team

AGENDA FOR THE SEMINARTOUR ON 4TH & 6TH FEBRUARY 2025 IN SON & LEUVEN

- **9.30 Welcome**

- **10.00 Next generation Low Power FPGAs for Industrial Solutions (Lattice Semiconductor)**
  "Lattice has driven innovation (low power, FDSOI) in the low density FPGA market with the Nexus platform.

  Meanwhile Lattice has entered the midrange with Avant and provides state of the art interfaces (25G transceivers) and hard IP features (PCIe Gen4, such as LPDDR4,DDR5).

  Still the low density market and the requirements of industrial customers will be key for Lattice strategically. In this slot we will provide an overview of the latest FPGA developments and our positioning and key differentiators vs. competition."

- **10.45 Short break**

- **11.00 FPGA Power Supplies: Efficiency, EMI, and Design Best Practice (Würth Elektronik / Alex Snijder)**
  In this session, we will cover the importance of power supplies, focusing specifically on the unique requirements of FPGA power supplies.

  We will delve into the critical role that passive components, such as capacitors and inductors, play in determining the overall efficiency of power supplies. Additionally, we will compare and contrast discrete solutions and modules for power supplies, highlighting their respective advantages and disadvantages. A significant emphasis will be placed on the importance of considering electromagnetic interference

  (EMI) in power supply design. By the end of this session, the audience will have gained a comprehensive understanding of how passive components influence power supply efficiency and will be equipped with best practices for designing efficient power supplies.

- **12.00 Lunch + product demonstrations**

- **13.00 Soft SOC (MCU) design for Industrial Ethernet (Ethercat) Protocols and Security (Lattice Semiconductor)**
  "With continuous advances in semiconductor manufacturing processes, processed, the technology that has been state of the art technology not even a decade ago (such as 16nm FinFet) has become an affordable solutions for lower density FPGAs.

  Thanks to advances in performance, power efficiency, and availability, modern FPGAs are now available at advanced nodes. In industrial applications, a mid-sized FPGA with sufficient I/Os is essential for optimal power efficiency and reliability. Often, the wafer space required is driven more by the number of I/Os than the FPGA core size, resulting in larger areas for cost-efficient logic densities.

  Despite their cost, FPGAs are essential for tasks requiring parallelism, throughput, and real-time data processing. To reduce costs, designers can add value by integrating functionality (e.g., real-time Ethernet) or using higher-level software, such as Soft-SoC systems with embedded Soft CPU cores (e.g., RISC-V). This approach, with enhanced capabilities, is ideal for real-time operating systems like FreeRTOS.

- **13.45 Short break**

- **14.00 Exploring Magnetic and Timing Products in Ethernet Applications: Impact on Signal Integrity and Layout Techniques (Würth Elektronik / Alex Snijder)**
  During this session, we will explore the various magnetic and timing products associated with Ethernet applications. You will gain a comprehensive understanding of the impact that magnetic components, traces and cable properties have on signal integrity.

  Additionally, we will delve deeper into the proper layout techniques for Ethernet and timing solutions, ensuring that you are well-equipped with the knowledge needed to optimize performance in these areas.

- **15.00 Ending**