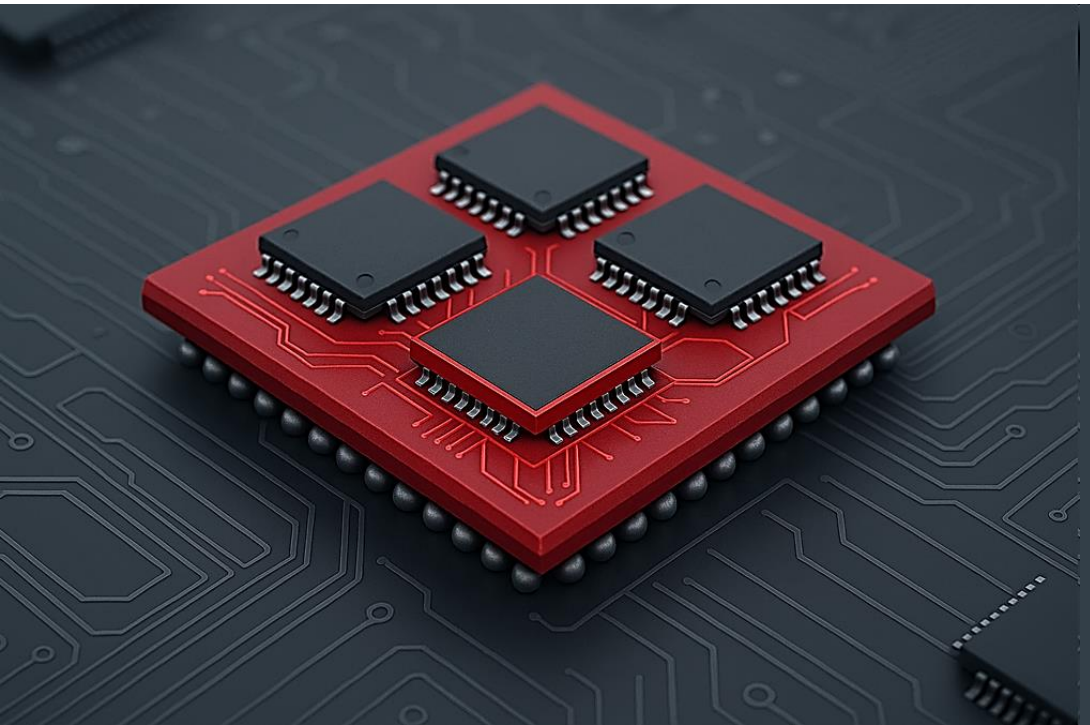


ADVANCED.HDI: PCB-DESIGN FÜR EINE SMARTWATCH - MIT SPECIAL GUEST LUKAS HENKEL (OV TECH GMBH)

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

AGENDA

PCB-Design für eine Smartwatch - mit Special Guest Lukas Henkel (OV Tech GmbH)

1. Einführung in die ADVANCED.hdi Technologie
   - Grundlagen
   - Herstellprozess

2. PCB-Design für eine Smartwatch – Lukas Henkel

3. ADVANCED.hdi Design Rules
4. Referenzprojekt
5. Handmuster

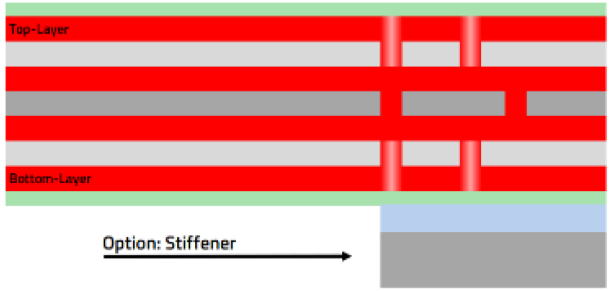
Advanced.hdi Team

- helene.stroebel@we-online.de
- michael.kress@we-online.de

HDI NÄCHSTE GENERATION: ADVANCED.HDI

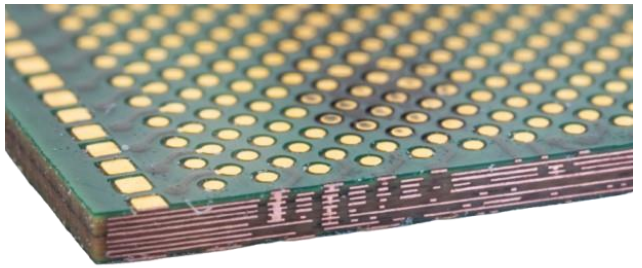
Steckbrief ADVANCED.**hdi**

- Anylayer-Microvia-Technologie
- Sehr dünne Materialien (ANSI GPY/42) → ultradünner Aufbau
- Lasergebohrte Microvias ∅ 70 µm im Pad ∅ 200 µm
- Sehr dünne Kupferschichtdicken auf den einzelnen Lagen
- Optimal für das Routing feinster BGA-Bauteile
- 75 µm Strukturen Standard, optional 50 µm
- Optionen
  - Impedanzdefiniertes Design
  - Stiffener
  - Lötträger



ADVANCED.hdi (1-2b-1)-Ri

Option: Lötträger



Quelle: OV Tech GmbH

ADVANCED.HDI

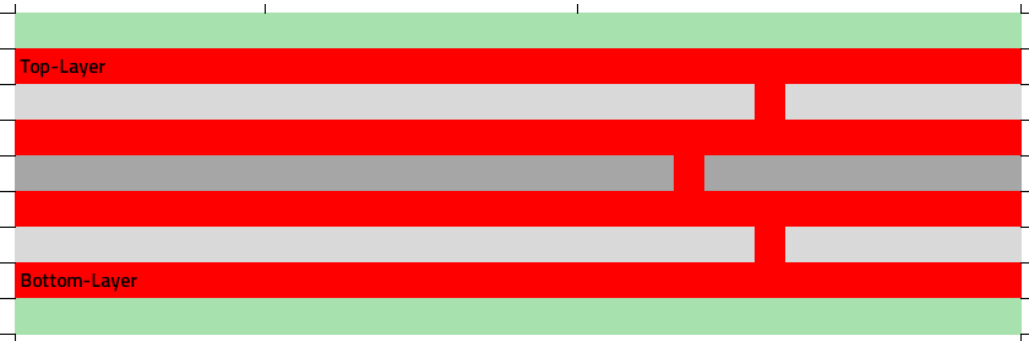
Herstellprozesse Anylayer-Microvia-Technologie ADVANCED.**hdi** 1-2b-1

- Innenlagenfertigung Kern mit lasergebohrten Microvias L2 - L3 + copperfilling
- Innenlagen ätzen bis max. 25 µm Kupferdicke

L2		**25**	
		50	GPY/42-core
L3		**25**	

- Verpressen zum 4-Lagen Multilayer
- Laserbohren Microvias Top - L2 und Bot - L3, plating und copperfilling
- Aussenlagen ätzen bis max. 35 µm Kupferdicke (nominal 25 µm)
- Aussenlagenfertigung mit Lötstopplack und Lötoberfläche

		20	Soldermask photosensitive
L1		**25**	9µm copper foil + plating
		35	GPY/42-prepreg
L2		**25**	
		50	GPY/42-core
L3		**25**	
		35	GPY/42-prepreg
L4		**25**	9µm copper foil + plating
		20	Soldermask photosensitive



ADVANCED.HDI

Standard Stackups

ADVANCED.hdi_ 4-2b-4

PCB Thickness : 0,62 mm +/-0,05mm

Rigid area Structure		Rigid area Thickness	Material description	rigid area		Viatypes	Layer usage
		20	Soldermask photosensitive				
L1		25	9µm copper foil + plating	Top-Layer			
		35	GPY/42-prepreg				
L2		25					
		35	GPY/42-prepreg				
L3		25					
		35	GPY/42-prepreg				
L4		25					
		35	GPY/42-prepreg				
L5		25					
		50	GPY/42-core				
L6		25					
		35	GPY/42-prepreg				
L7		25					
		35	GPY/42-prepreg				
L8		25					
		35	GPY/42-prepreg				
L9		25					
		35	GPY/42-prepreg				
L10		25	9µm copper foil + plating	Bottom-Layer			
		20	Soldermask photosensitive				

Materialien

- Auswahl Kernmaterial:
  - 0,05 mm, Kupferfolie 12 µm
  - 0,10 mm, Kupferfolie 12 µm
- Prepreg
  - 0,04 mm
- Kupferfolie
  - 9µm

- Enddicke nach Lagenanzahl

Lagenanzahl	Enddicke
4 Lagen 1-2b-1	0,25 mm
6 Lagen 2-2b-2	0,36 mm
8 Lagen 3-2b-3	0,47 mm
10 Lagen 4-2b-4	0,58 mm

ANWENDUNGSBEREICHE

OV Tech GmbH

Open-Source Smartwatch

Objective

Create the first **modular and community centric** consumer Smart Watch

How?

Publish Hardware and Firmware sources.
Hardware designed for right to repair.

- build an **open and high-trust** ecosystem
- **modular** and customizable
- custom code/hardware friendly
- community centric

Modular

Modularity for repairability and upgradability

Display Module

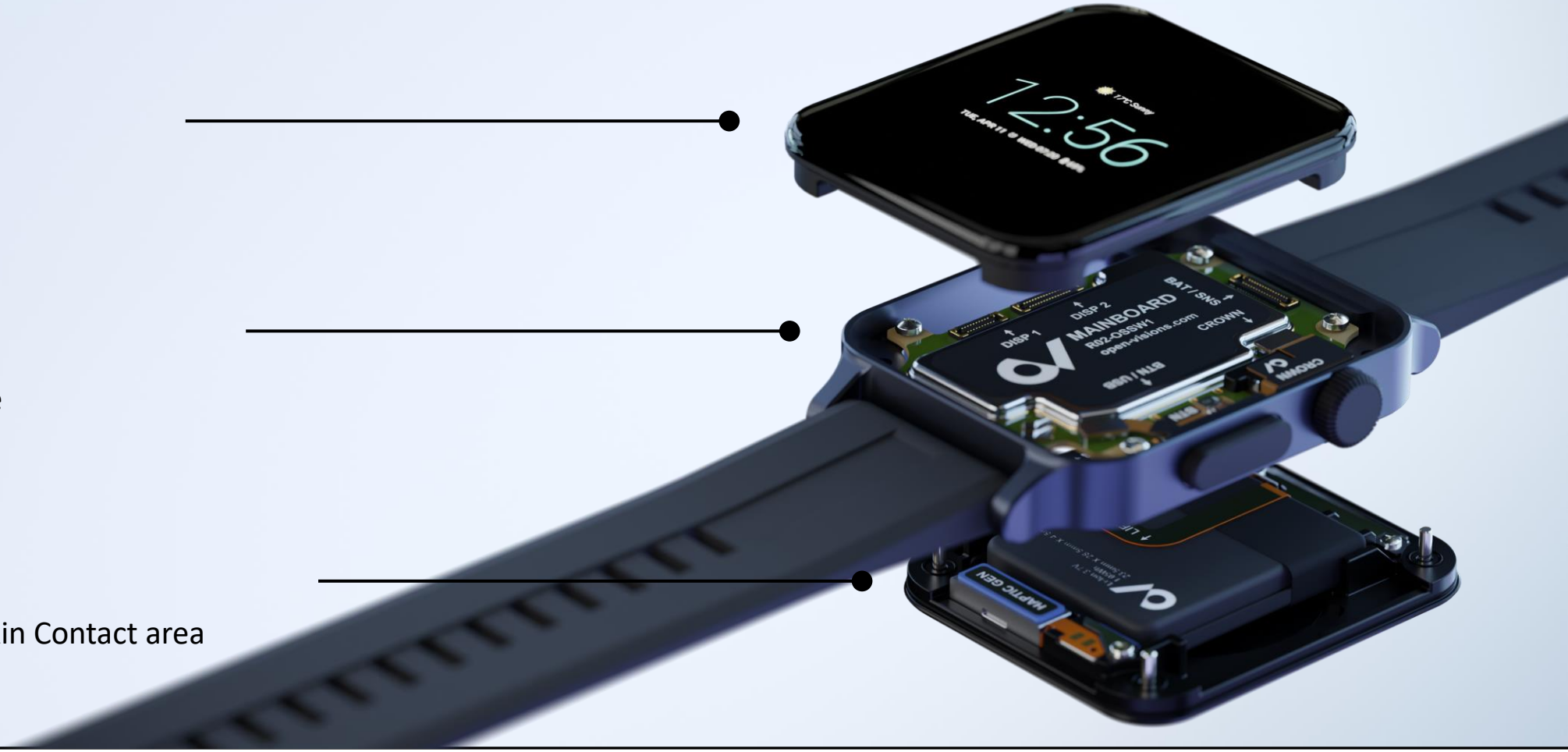
Touch AMOLED
Rounded Coverglass

Compute Module

Machined Aluminum Frame
Digital Crown
USB-C

Sensor Module

Smooth Glass and Plastic Skin Contact area



Hardware

Sensor Module

- **Heart rate** sensor
- **Blood oxygen** sensor
- **Pressure** sensor
- Haptic feedback
- Microphone
- **QI charging**
- **Speaker**

Compute Module

- **Dual Core A35** SoC @0.8GHz
- 2GB LPDDR4x
- **16GB eMMC** Storage
- **Digital Crown**
- User button
- **IMU**
- **Compass**

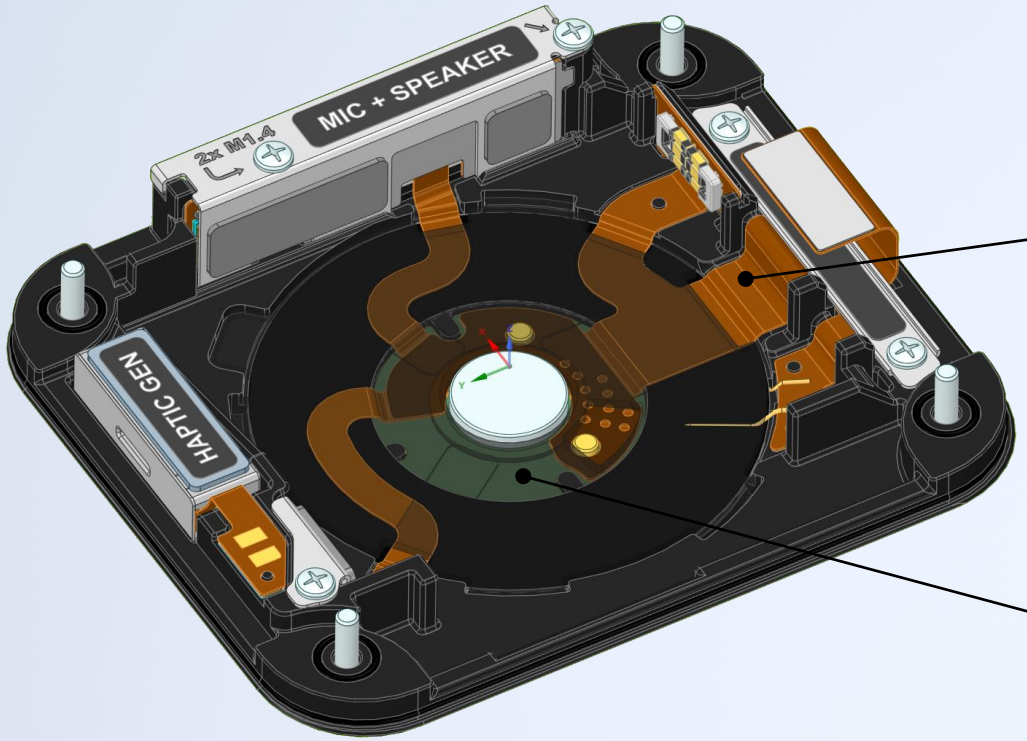
Display Module

- 386 x 448 AMOLED **Touchscreen**
- **NFC + WiFi/BLE** Antenna
- Ambient light sensor

Side View

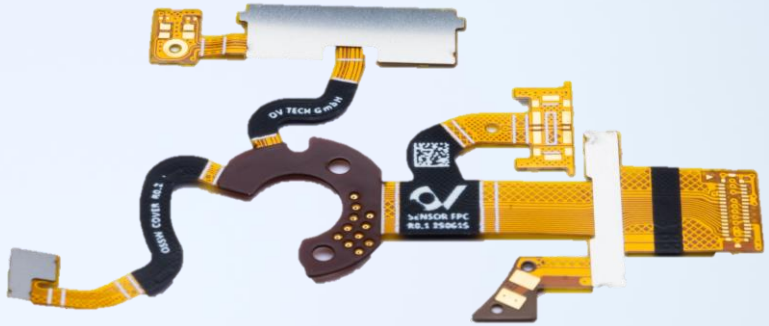
- **USB-C**

Modules – PCB Technologies



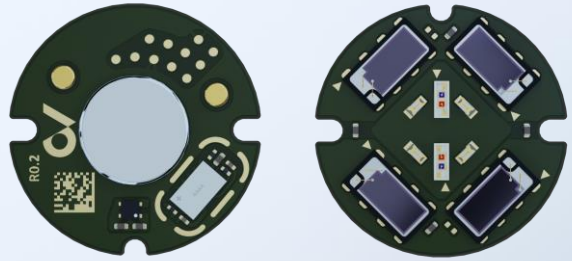
2-Layer FPC

- 0.35mm connectors
- 01005 passives

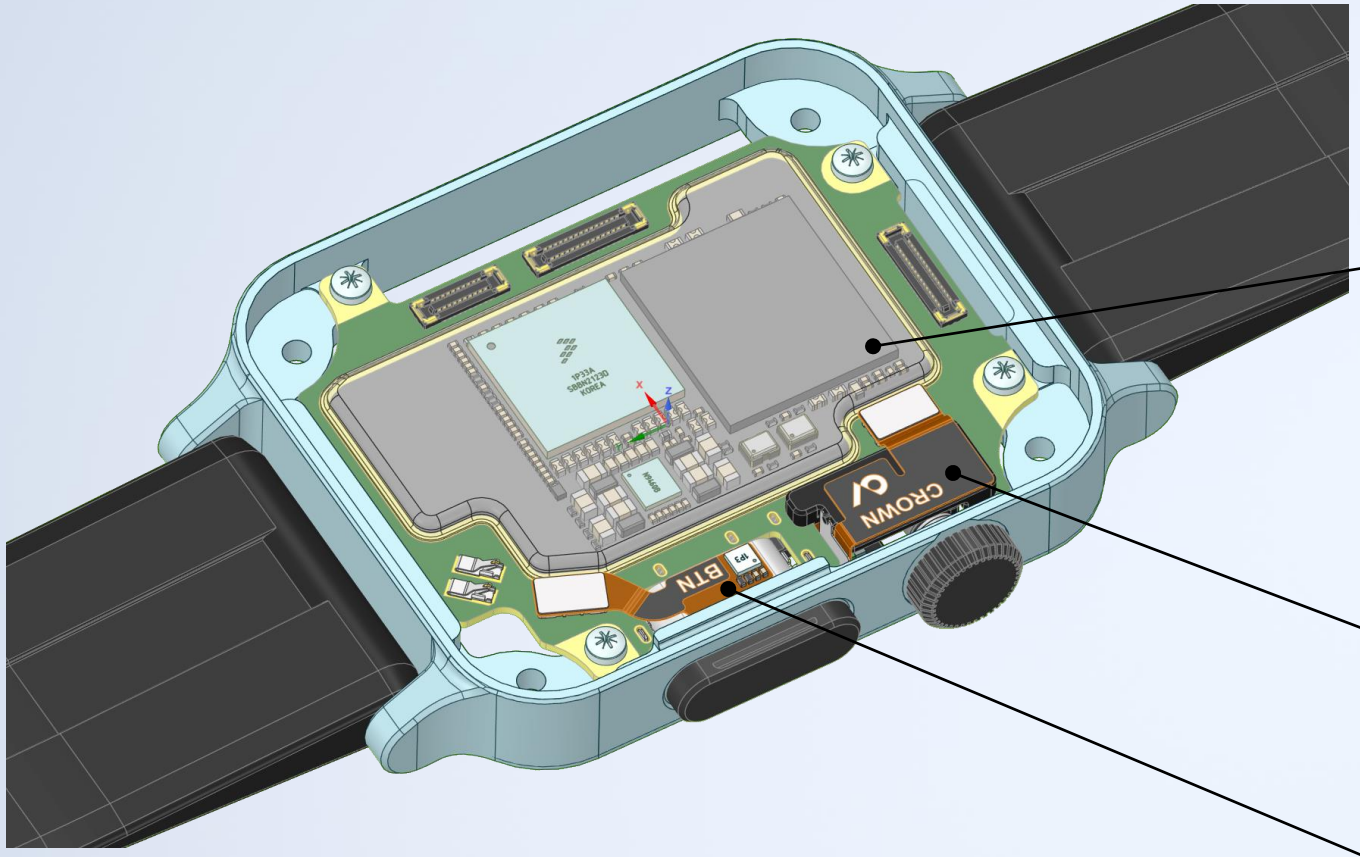


6-Layer ELIC

- 0.4mm WLCSP
- 01005 passives

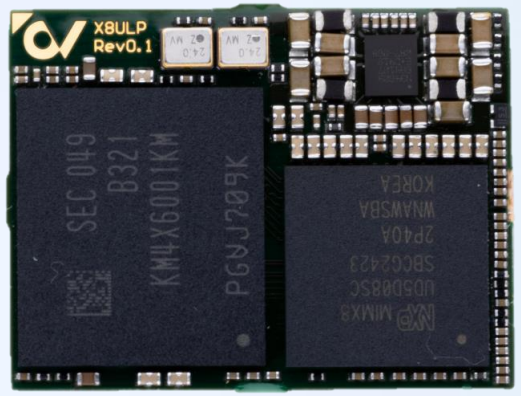


Modules – PCB Technologies



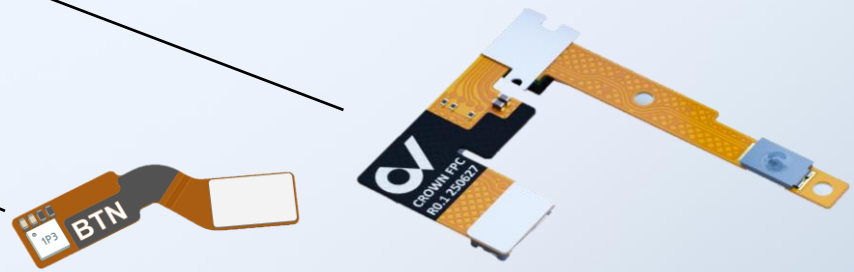
10-Layer ELIC

- 0.4mm WLCSP
- 0201 passives

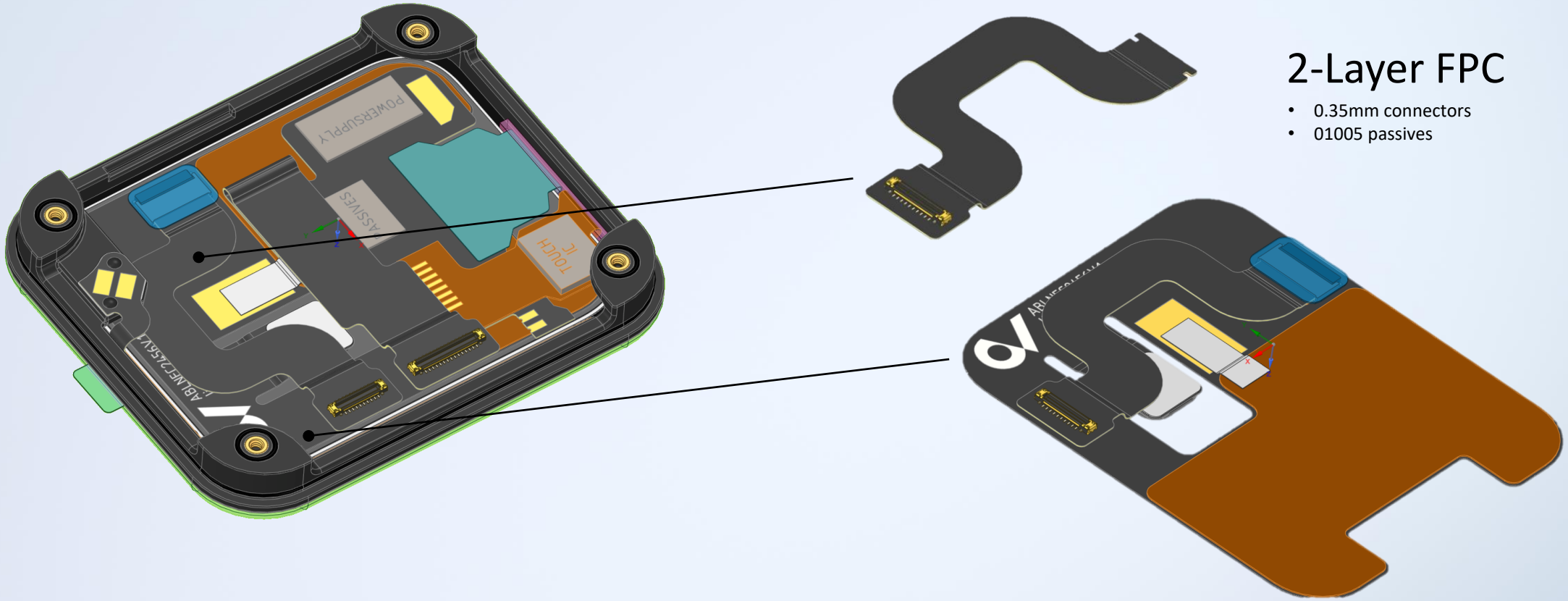


2-Layer FPC

- 0.35mm connectors
- 01005 passives



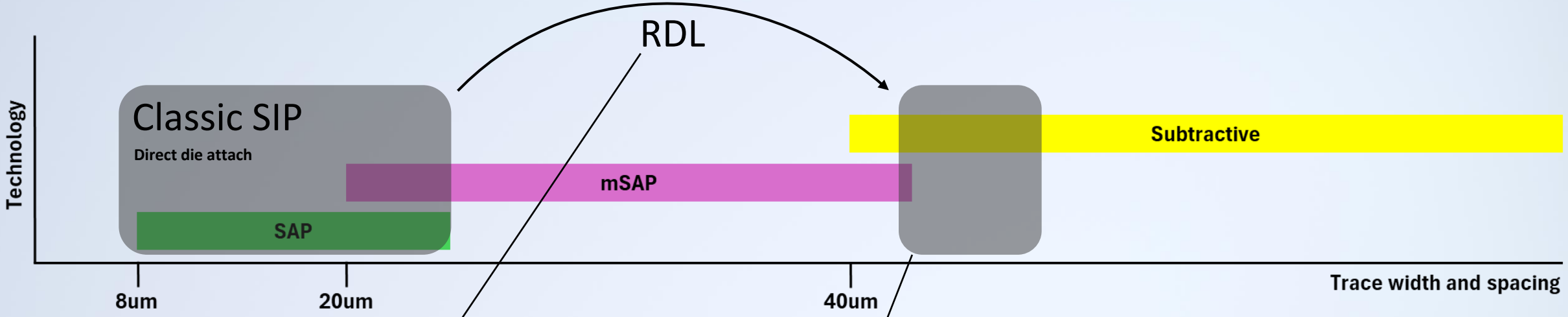
Modules – PCB Technologies

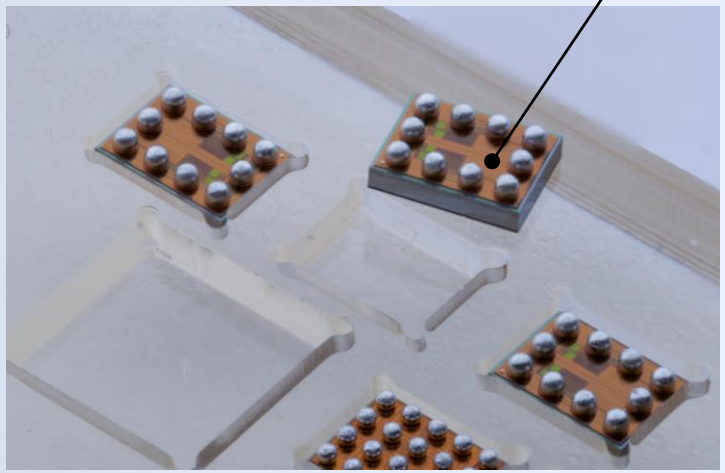


2-Layer FPC

- 0.35mm connectors
- 01005 passives

SiP Design – Manufacturing Technologies





WLCSPs

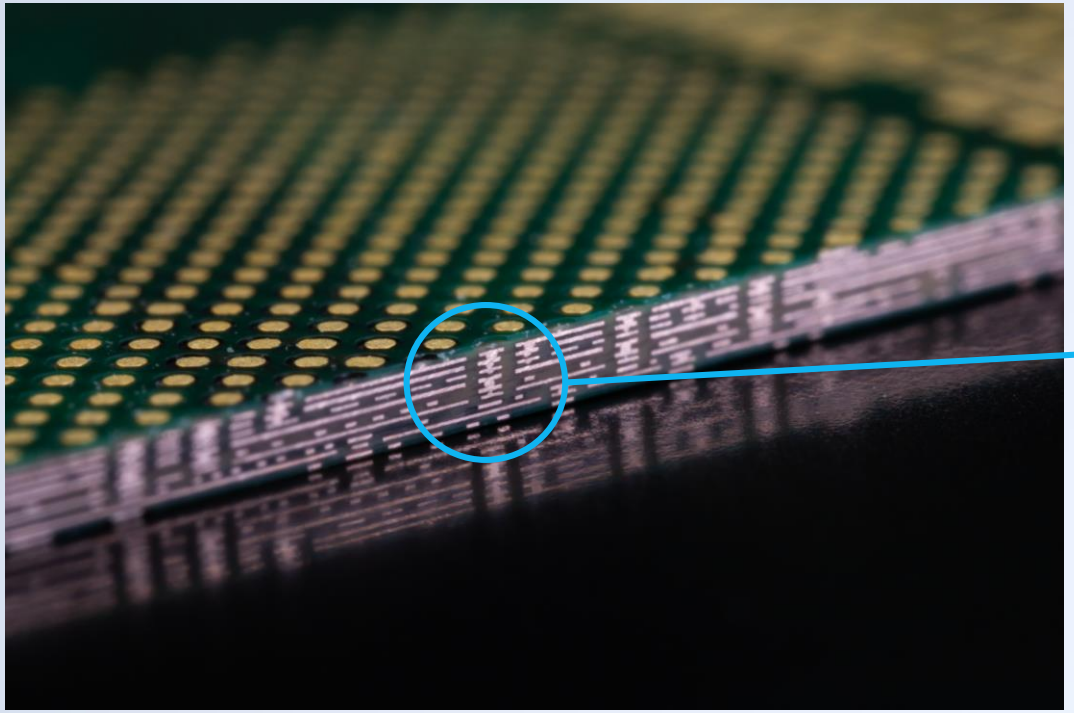
- **RDL interfaces with silicon**
- In classical SIPs the RDL is usually skipped

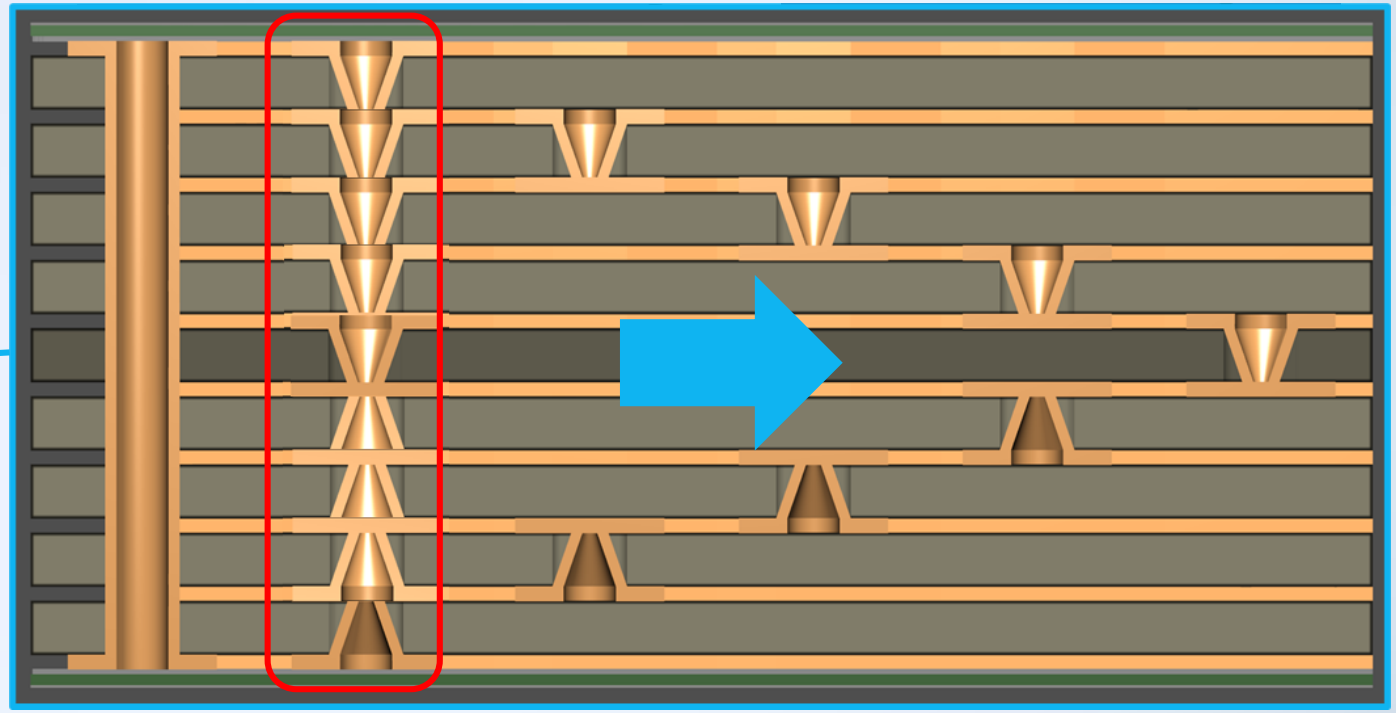
er ELIC

es with

Ps the
skipped

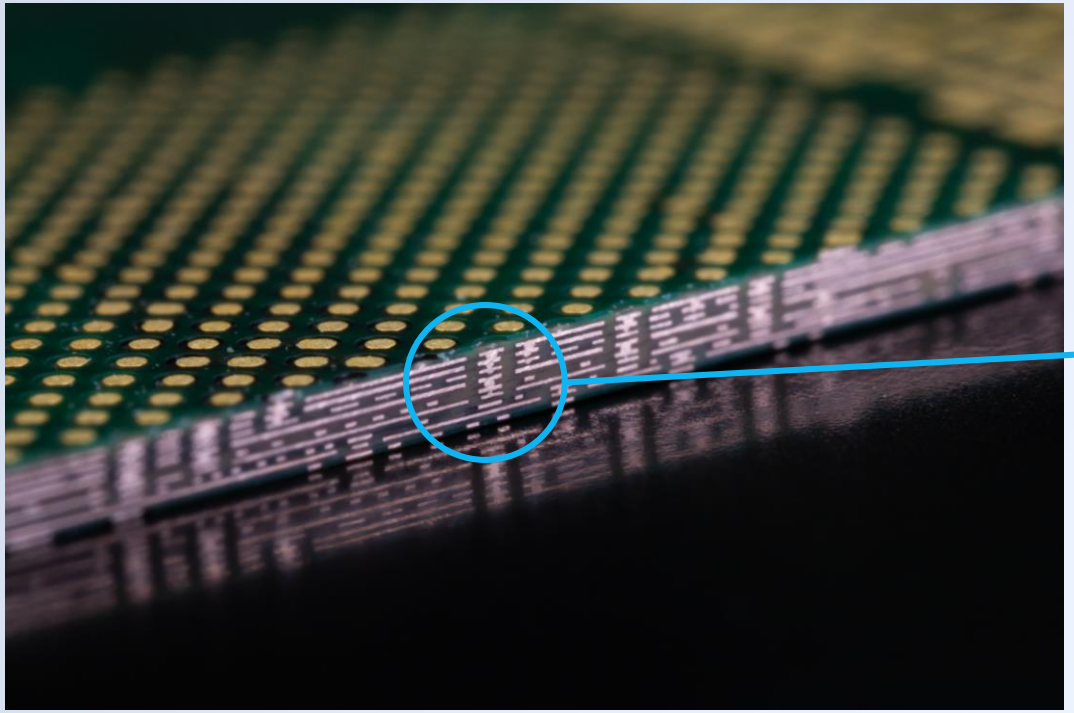
Space benefits – ADVANCED.hdi

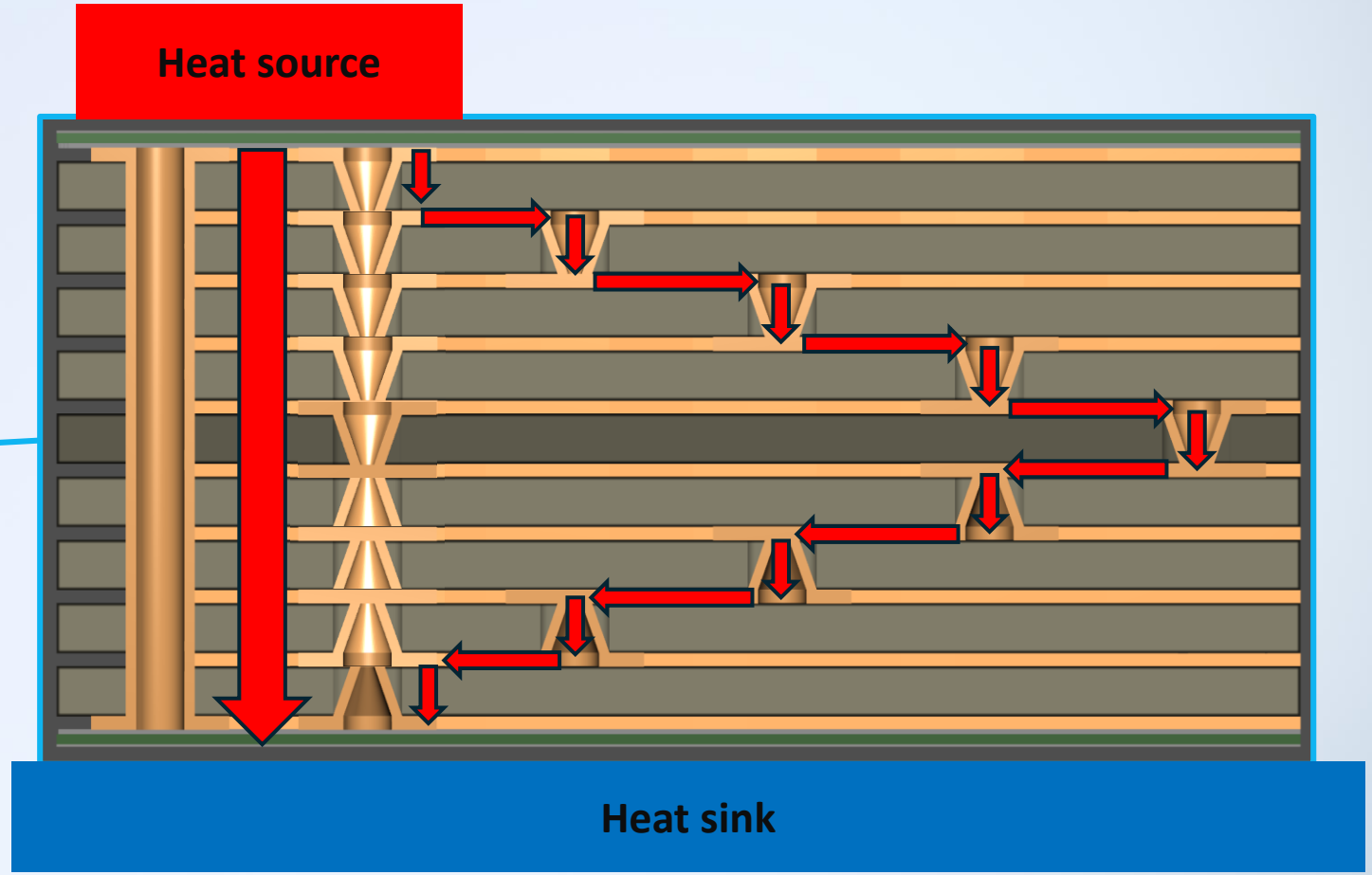




Staggered VIAs:
Require much space on inner layers
-> Not possible on full matrix 0.4mm BGAs

Thermal benefits – ADVANCED.hdi





Stacked VIAs:
Low thermal resistance

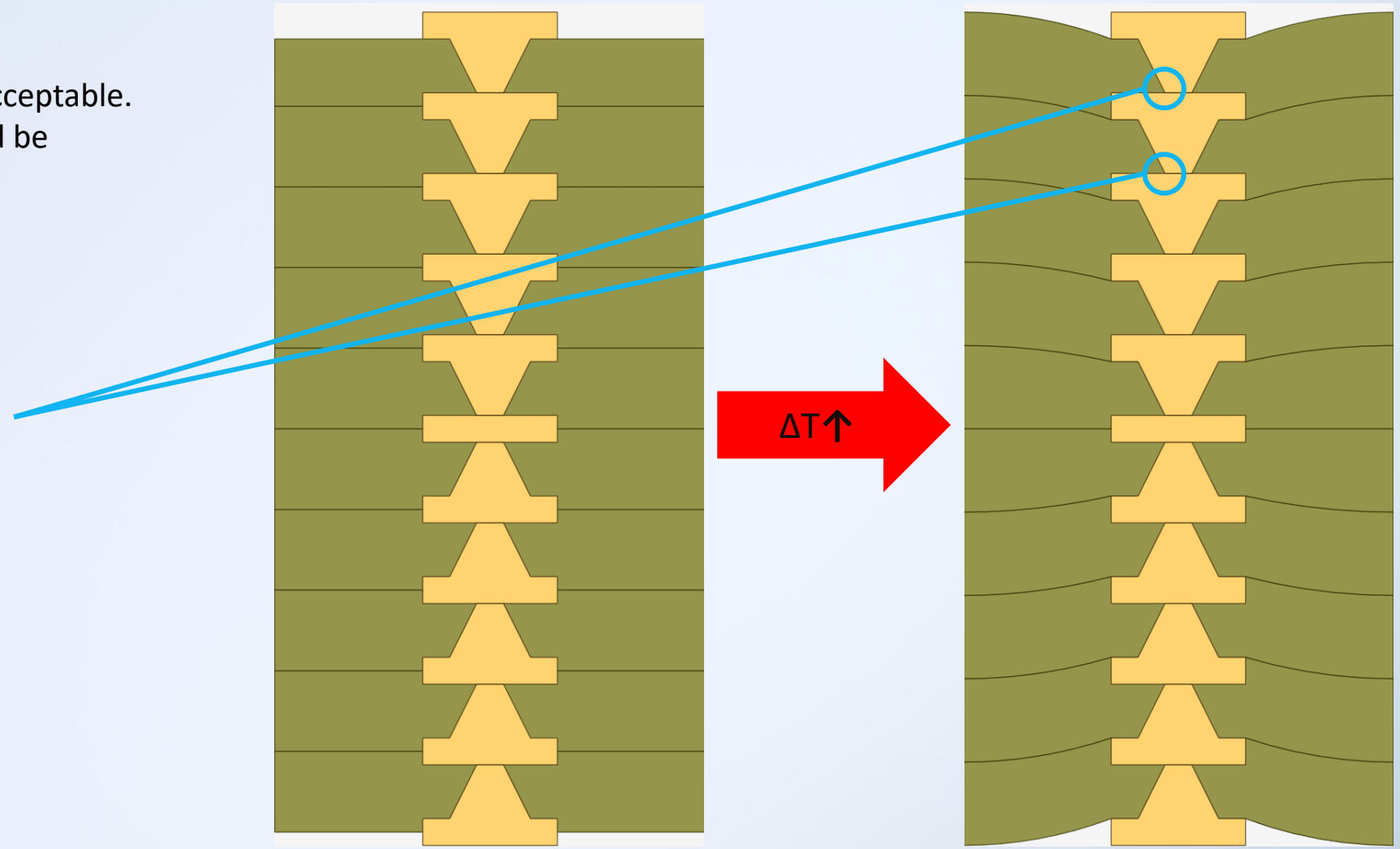
Staggered VIAs:
High thermal resistance along Z-axis

VIA reliability

IPC-2226, section 9.1.2:

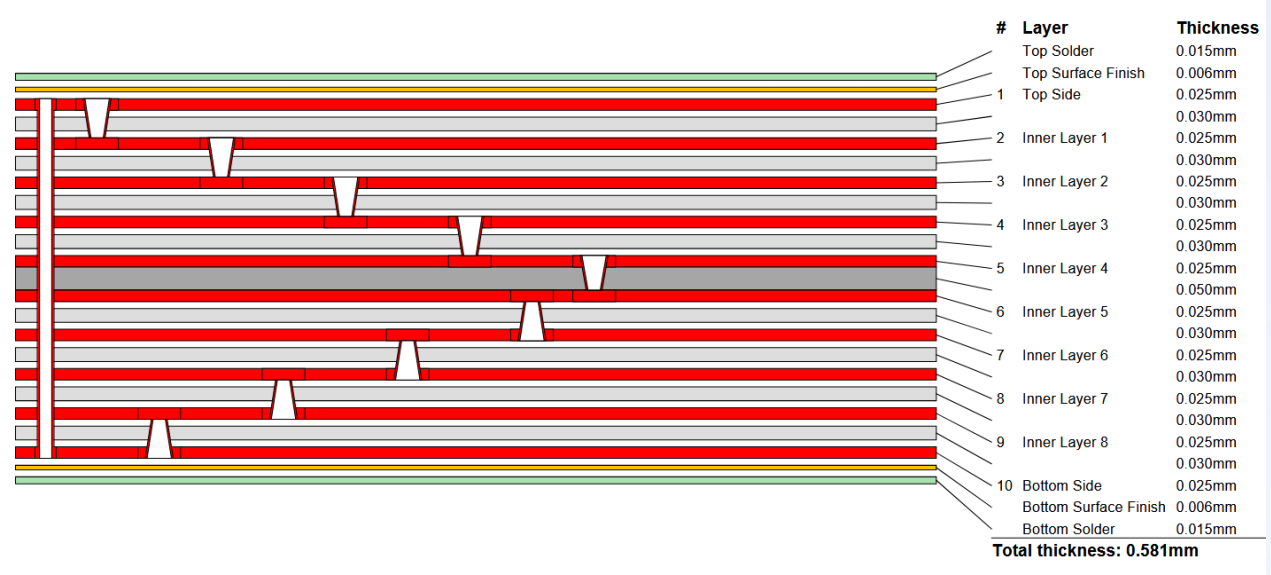
"Stacking of two microvias is generally acceptable. Stacking more than two microvias should be substantiated by reliability testing."

Stress concentration at VIA barrel edges



VIA reliability – ADVANCED.hdi

Stackup - HDI10_4-(2b)-4_058_25



Material used: GPY/42 Polyimide based

GPY/42 characteristics

Characteristics					
Item		Condition[3]	Unit	Actual Value ANSI: GPY/42	Reference (IPC-TM-650)
Tg	TMA method	A	°C	260-280	2.4.24
	DMA method	A		300-330	
CTE[1]	X (30-120 °C)	A	ppm/°C	4,0-6,0	
	Y (30-120°C)			4,0-6,0	
Solder Heat Resistance (260 °C)		A	sec.	>=300	
T260 (without cuopper)		A	min.	>=60	
T288 (without copper)				>=60	2.4.24.1
Decomposition Temperature (TGA methode, 5% Weight Loss)		A	°C	430-450	2.3.40
Heat Resistance for HDI Proces (Semi-Additive)		260°C Reflow	cycles	>=20	
Copper Peel Strength	12 µm	A	kN/m	0,7-0,9	2.4.8
	18 µm			0,8-1,0	
Surface Roughness (Ra)		A	µm	2-3	2.2.17
Flexural Modulus (Lengthwise)[4]		A	Gpa	30-32	
Dielectric Constant	10 GHz[2]	A		4.2-4.4	
Dissipation Factor	10 GHz[2]	A		0,006-0,008	
Volume Resistivity		C-96/40/90	Ω*cm	$1x10^{14}$ - $1x10^{16}$	2.5.17
Survace Resistance		C-96/40/90	Ω	$1x10^{13}$ - $1x10^{15}$	
Insulation Resistance		A	Ω	$1x10^{14}$ - $1x10^{16}$	
		D-2/100		$1x10^{12}$ - $1x10^{14}$	

High Modulus -> stiff material

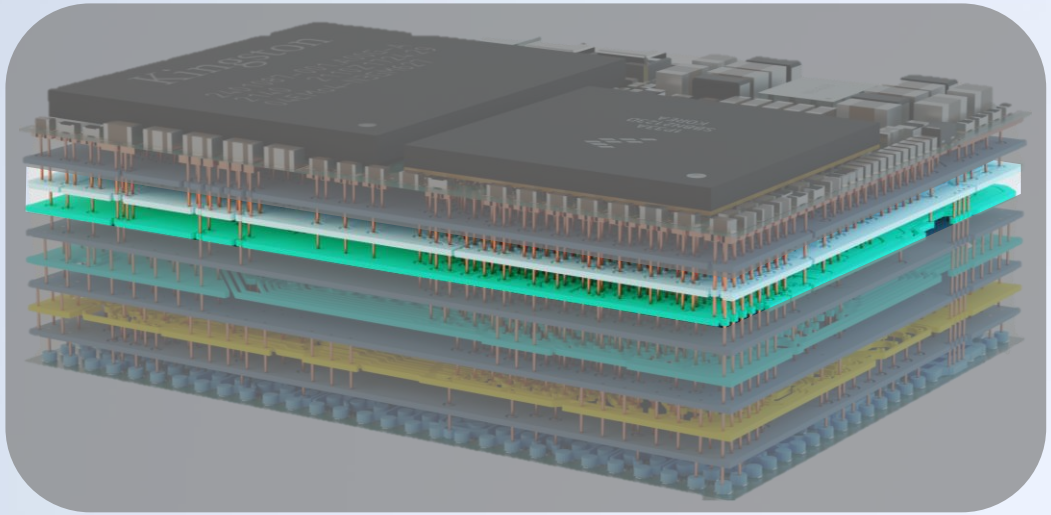
comparison FR4 17-24 GPa

Low CTE -> low thermal expansion

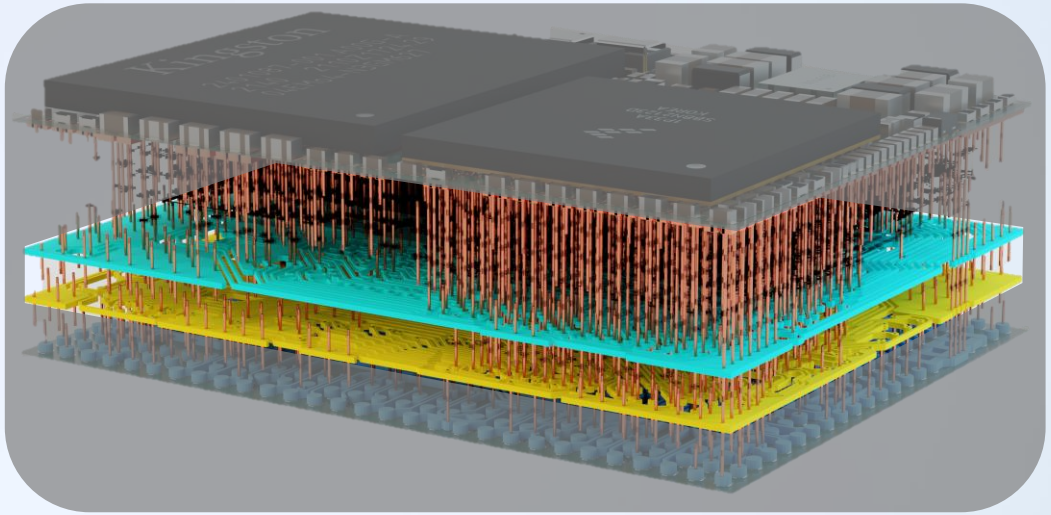
comparison FR4 13-18 ppm/°C

Low CTE + thin film thickness allows reliable VIA stacking

Asymmetric stackup – ADVANCED.hdi

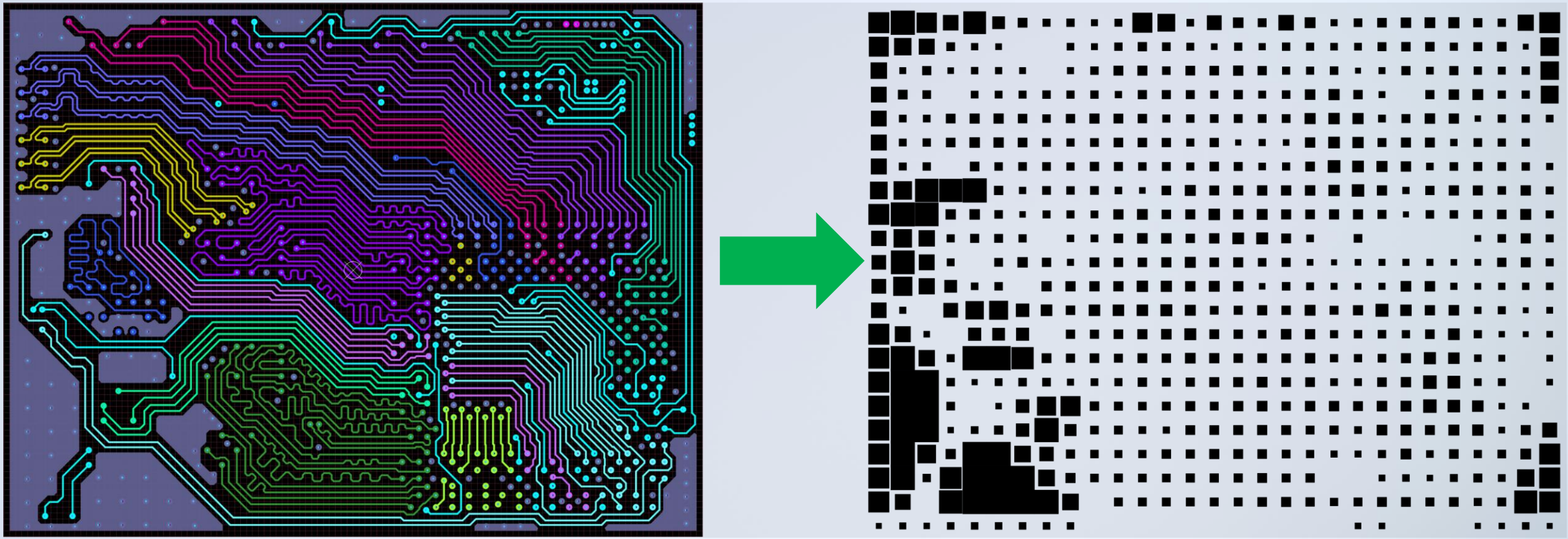


Power planes on L2/L3
-> Reduced inductance from capacitors on TOP layer to SoC



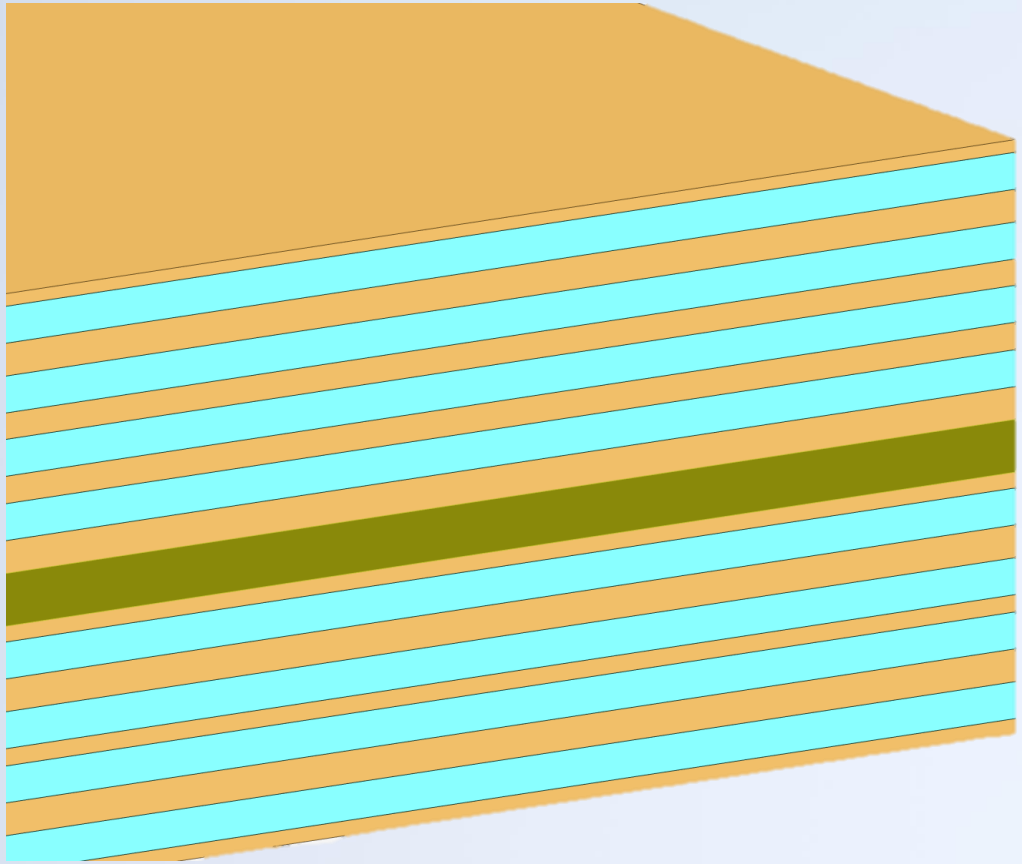
Signal layers on L7/L3
-> Copper fillfactor is asymmetric, risk of bow and twist!

Calculate bow and twist – ADVANCED.hdi

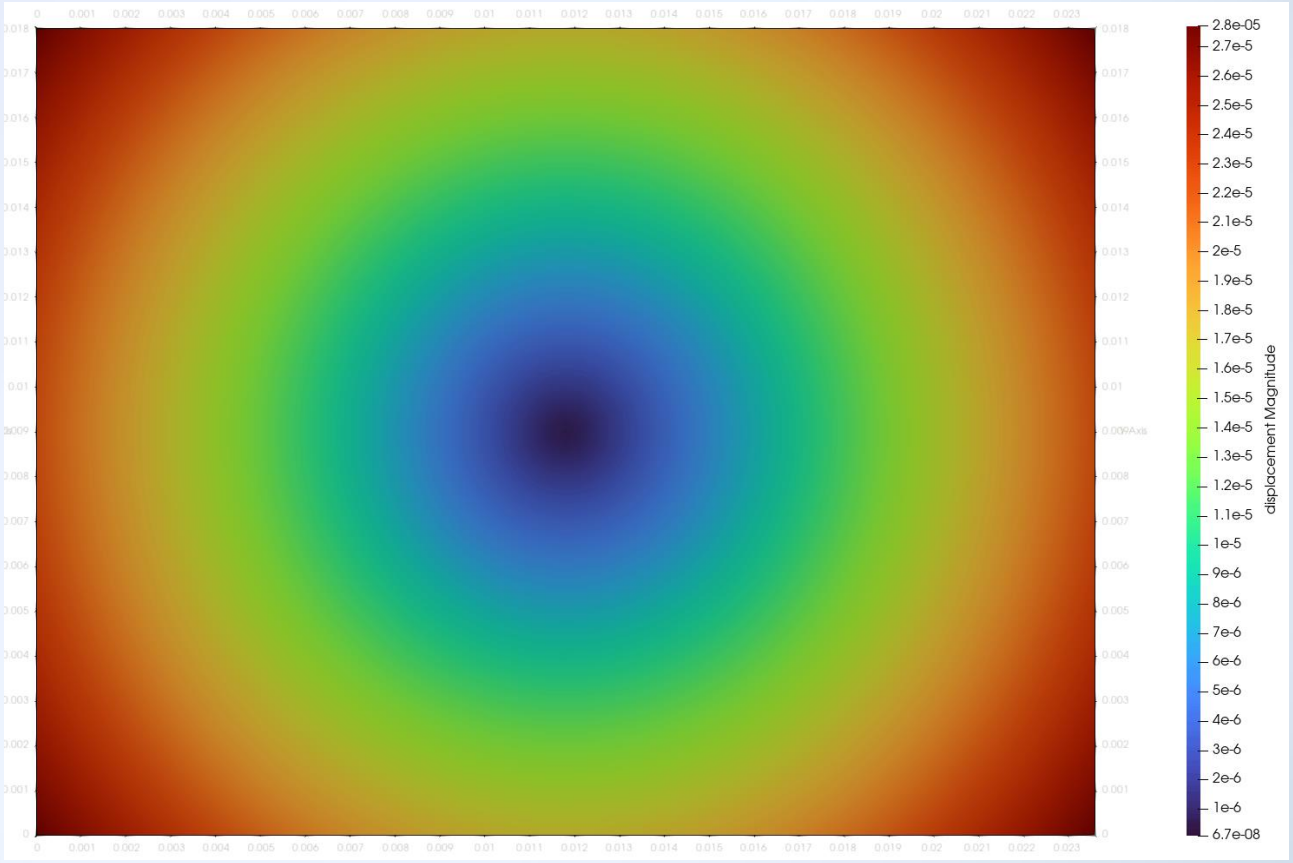


Generate density map from layout data to reduce mesh size

Calculate bow and twist – ADVANCED.hdi

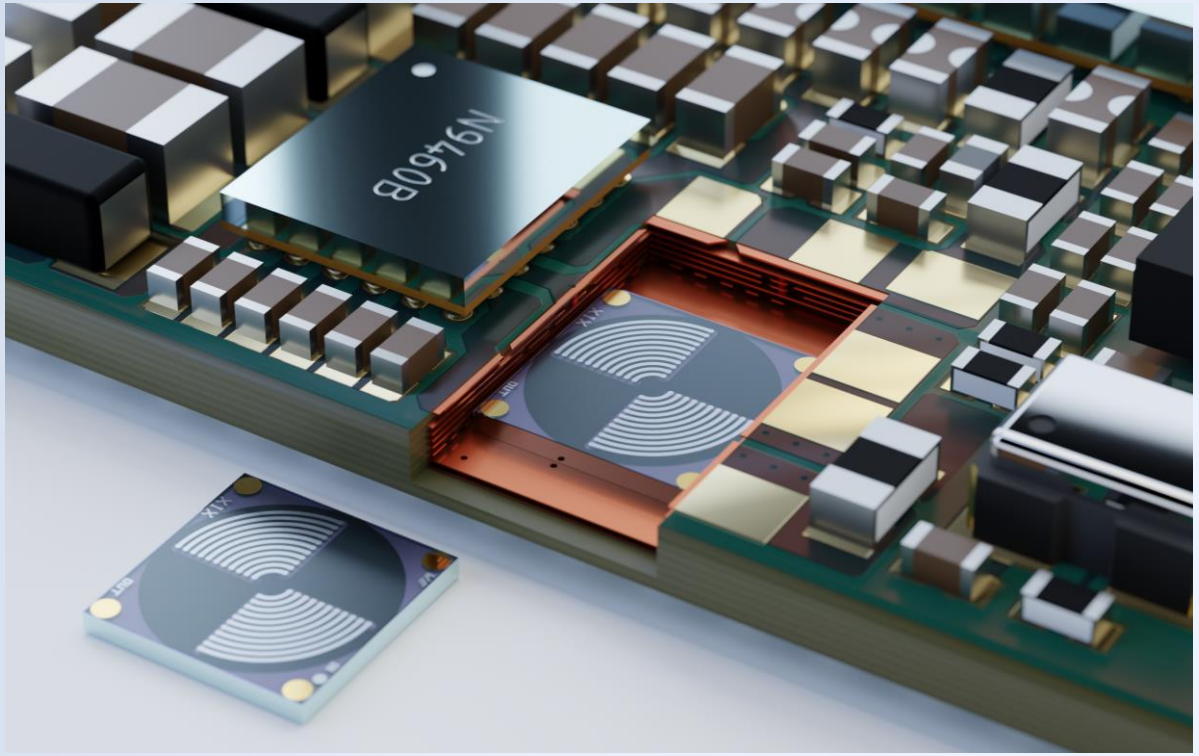


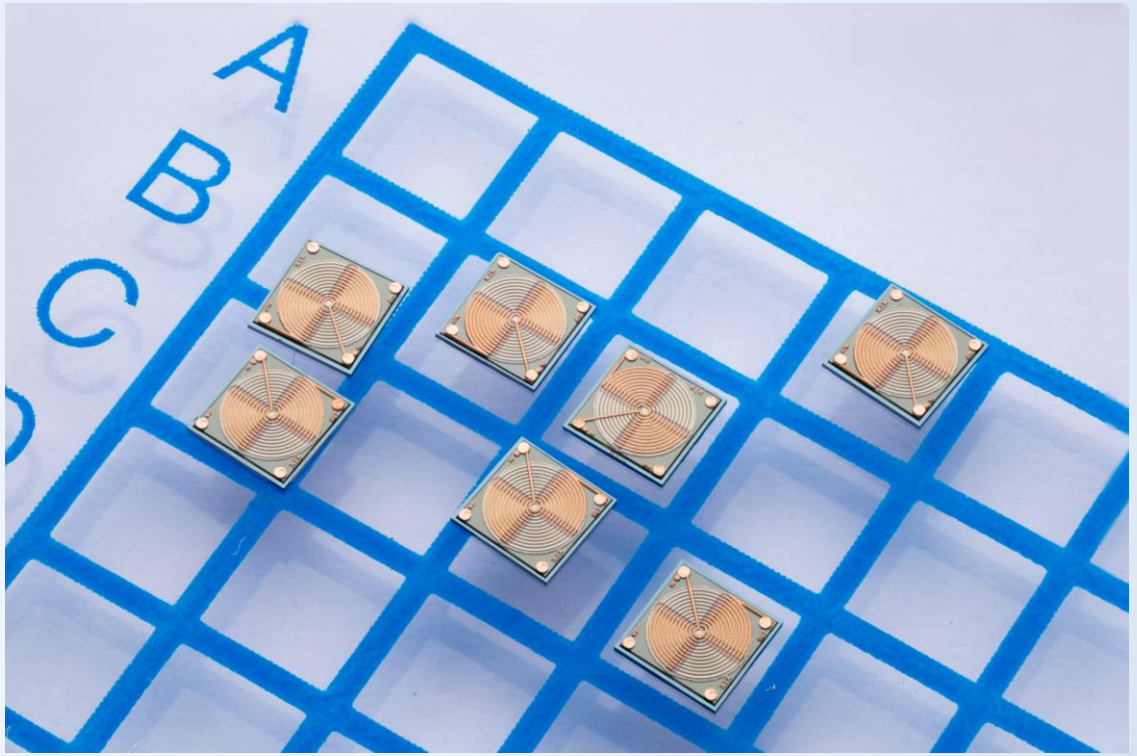
Normalized density representation



Simulation shows 28um displacement magnitude

Component embedding – ADVANCED.hdi





Next miniaturization step: embedded inductors

Component embedding – ADVANCED.hdi

Rigid area structure	Rigid area thickness [µm]	Info	Material description	Assembly/connection types	Viatypes # 1	# 2	# 3	# 4	# 5	# 6	# 7
Soldermask	15										
L1	25										
	40		FR4 PP TG250								
L2	25										
	40		FR4 PP TG250								
L3	25										
	292		FR4 PP TG250								
			FR4 TG250								
			FR4 PP TG250								
L4	25										
	40		FR4 PP TG250								
L5	25										
	40		FR4 PP TG250								
L6	25										
Soldermask	15										

Notes:

1 Burried via from L3 to L4 / can be filled&capped if needed

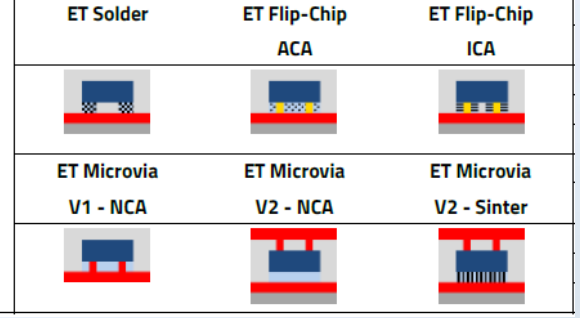
2 Micro via from L2 to L3 / L5 to L4 can be copper filled if needed

3 Micro via from L1 to L2 / L6 to L5 can be copper filled if needed

4 Standard via from L1 to L4

Component can also be on layer 4

Assembly types - definition of colours



Power Module Layerstack

MCAD & ECAD Desing Walkthrough

Q&A

Open-source hardware as a fundamental building block

The open-source Smart Watch hardware is the ideal starting point for customized wearable solutions. Contact us to discuss innovating in an open ecosystem!

Contact

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Germany

Lukas Henkel – CEO

Lukas is an experienced hardware designer with 10+ years experience in the industry. He has worked on and successfully brough to market complex board designs. His background as head of engineering has gained him valuable insights into marketing and communication strategies with international costumers.

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Markus Henkel – CFO

Markus holds a degree in business administration and has in-depth expertise in the field of corporate finance with a focus on real estate.
He started his career as a trainee in the banking sector in 2010 to 2014. Until 2017, he was responsible for the areas of financing, controlling and taxes at a medium-sized online retailer. Since 2017, he is responsible for corporate finance and project finance with a mezzanine and equity financier for real estate projects.

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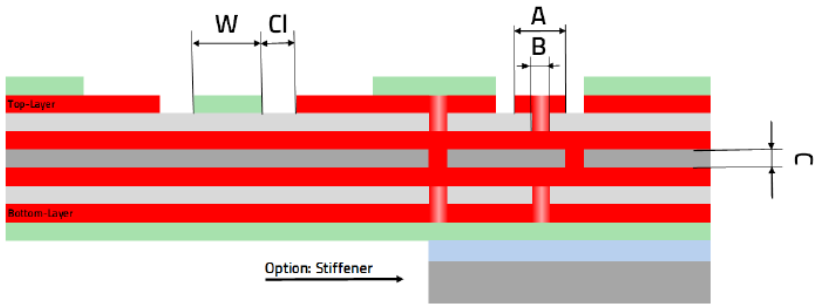
ADVANCED.HDI DESIGN RULES

Download hier: https://www.we-online.com/designrulesadvancedhdi-de

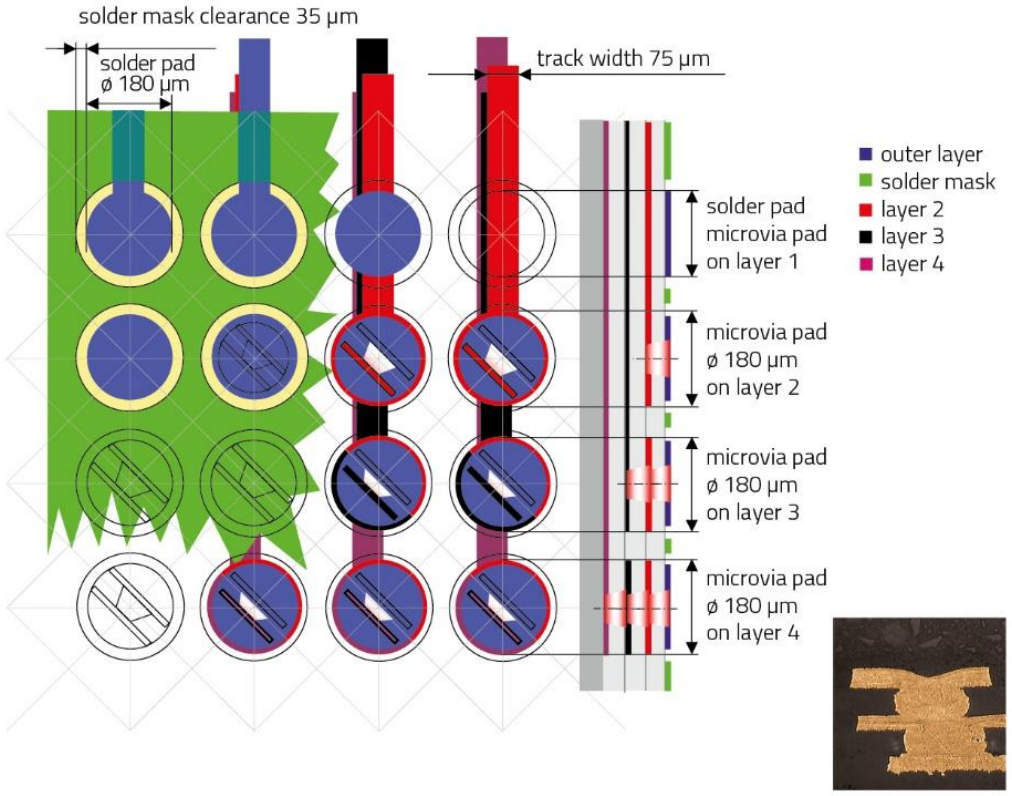
Stackup ADVANCED.**hdi (1-2b-1)-Ri**

Nur Microvias



Symbol	Beschreibung	Technischer Standard	Erhöhte Anforderung
	Leiterbreiten und -abstände → nur Microvias	75 µm / 75 µm	50 µm / 50 µm
A	Minimaler Paddurchmesser für Microvias	225 µm	200 µm
B	Bohrenddurchmesser gelaserter Microvias, typisch	85 µm	70 µm
	Für alle Padanbindungen werden Teardrops empfohlen!		
-	Abstand Kupfer zur Kontur	≥ 300 µm	≥ 225 µm
-	Anzahl der Kupferlagen insgesamt	4 bis 10	
C	Dicke des Kerns (ANSI GPY/42, halogenarm, gefüllt)	50 µm	
-	Dicke der kaltverklebten Verstärkung aus FR4.0-Material	0,8 mm	1,00 mm – 1,55 mm
	Dicke des Lötträgers aus FR4.0-Material	0,8 mm	0,8 mm
-	Dicke des Klebers für die Verstärkung und Lötträger	50 µm	
W	Minimale Breite Lötstoppmaskensteg	70 µm	50 µm
Cl	Minimale Lötstoppmaskenfreistellung, umlaufend	40 µm	35 µm

BGA 0.30 mm pitch

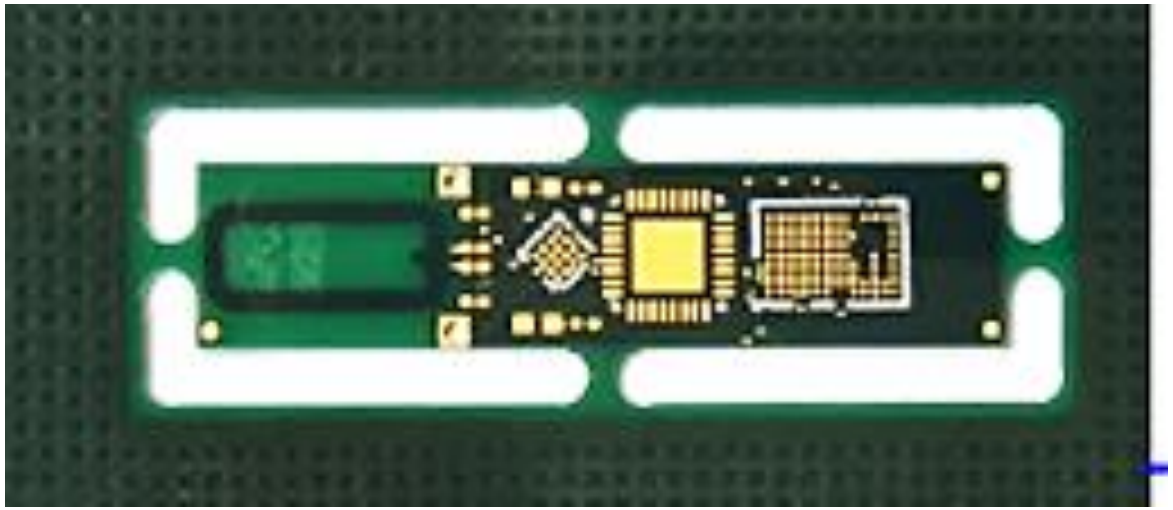


REFERENZPROJEKTE

NFC- Bezahlring

SLIM.hdi 1-2b-1 mit FR-4.1

- Klein, kompakt, kleinstes Gehäusevolumen
- Layout Design 75 µm / 75 µm
- Laser Microvias über alle Lagen (ELIC)
- BGA-Footprint Pitch 0,35 mm



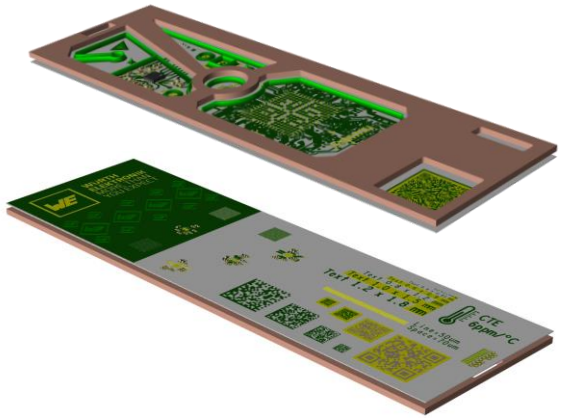
Quelle: Infineon Technologies

HANDMUSTER – COMING SOON

ADVANCED.hdi

Basismaterial

- ANSI GPY/42 für Interposer und Module
- Niedriger Ausdehnungskoeffizient: CTE(x,y) 4 bis 6 ppm/K
- Hohe Glasübergangstemperatur: Tg ≥ 260 °C
- Zersetzungstemperatur: ≥ 430 °C
- Erheblich reduzierte Verwindungs- und Wölbungsneigung
- Zyklenfest



HANDMUSTER ZUM BEGREIFEN

https://www.we-online.com/leiterplatten-handmuster - hier direkt bestellen!

WÜRTH ELEKTRONIK
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