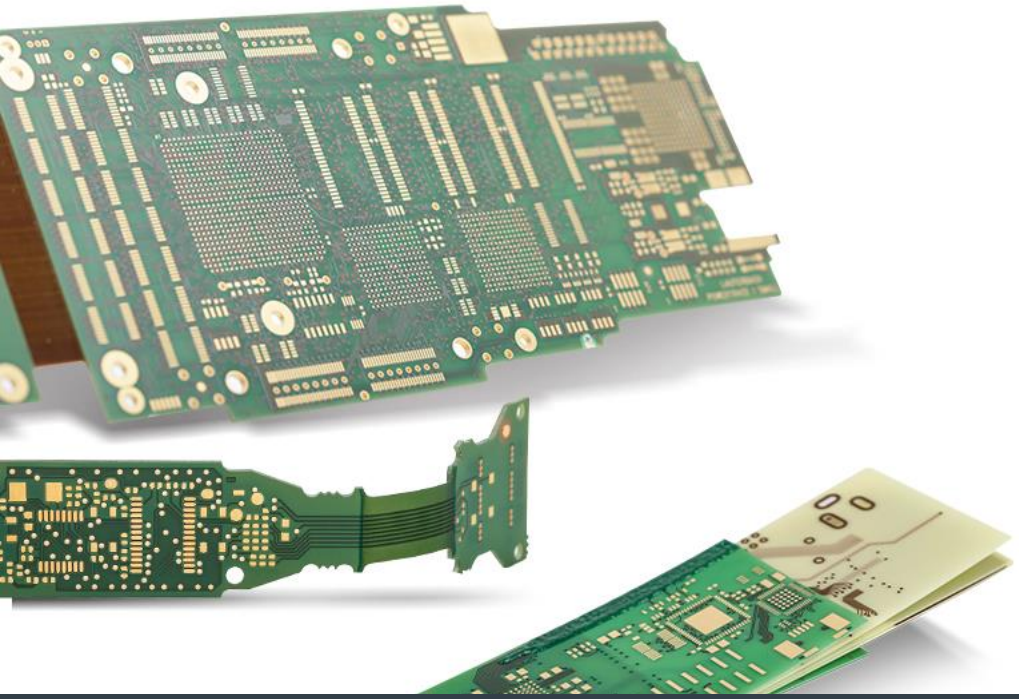
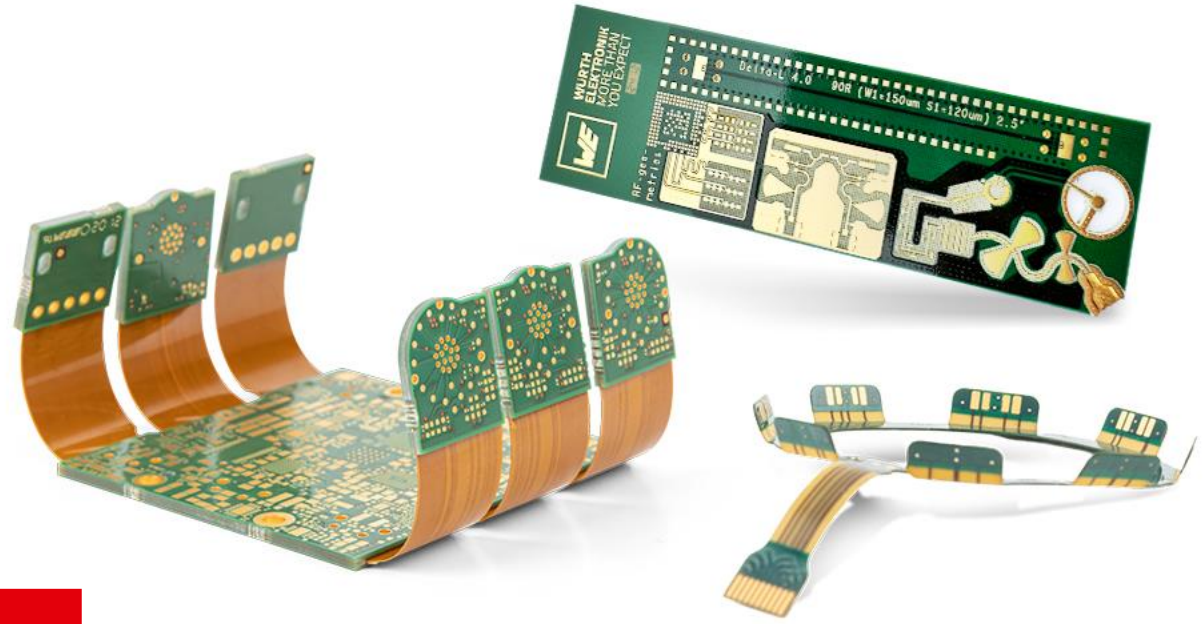




IMPEDANZ IST FÜR ALLE DA!

Andreas Dreher, FAE

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

SPEAKER INTRODUCTION

Andreas Dreher

Technical Project Management

- HDI-Design
- Signal Integrity & High Speed

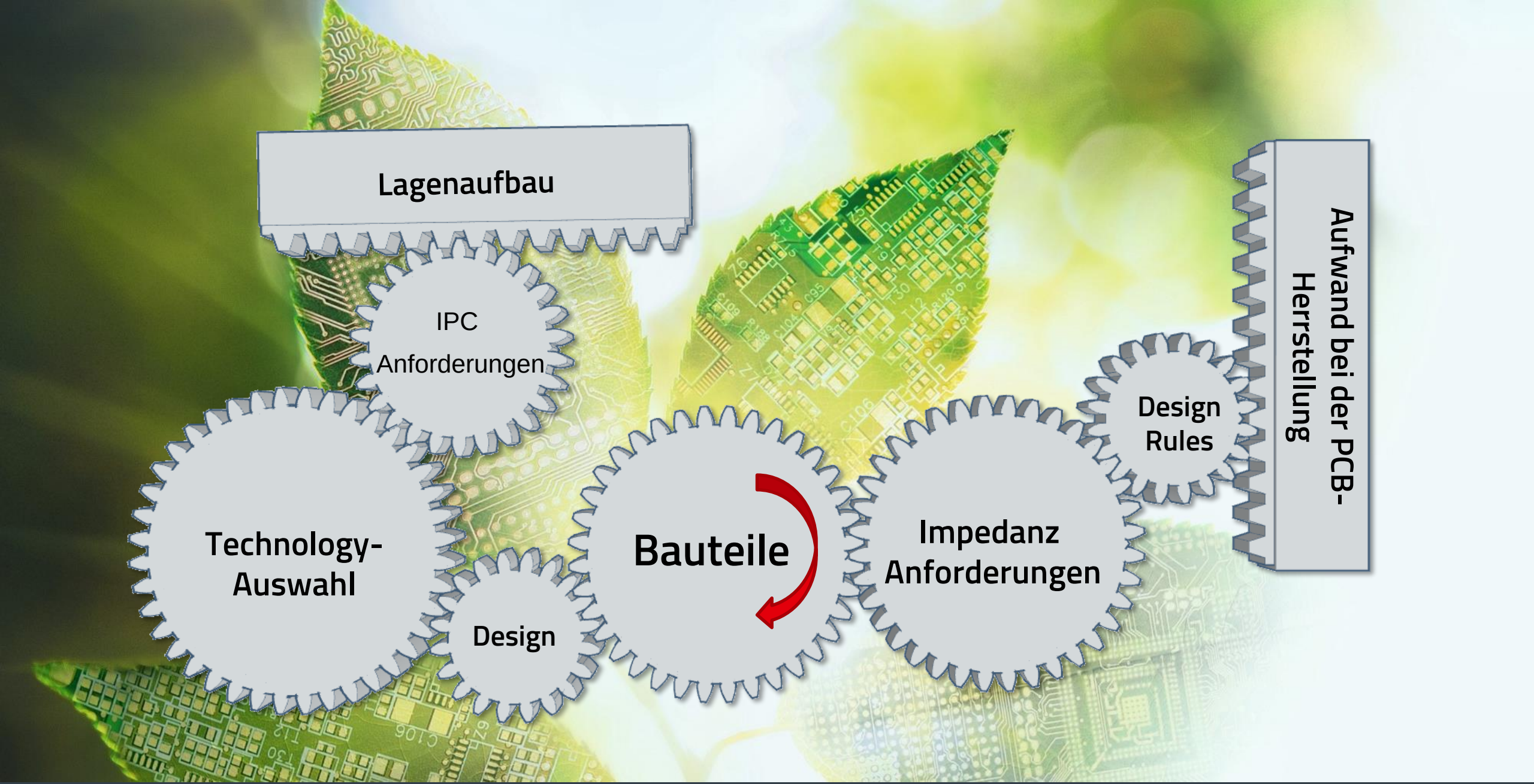
Since 2003 at Würth Elektronik CBT

Phone +49 7622 397-133
Mail andreas.dreher@we-online.com

Andreas Dreher
Field Application Engineer
Technical Project Management

AGENDA

1. Einführung in Impedanzen
2. Lagenaufbauten
3. High Speed Materialien
4. Best Practice Beispiele

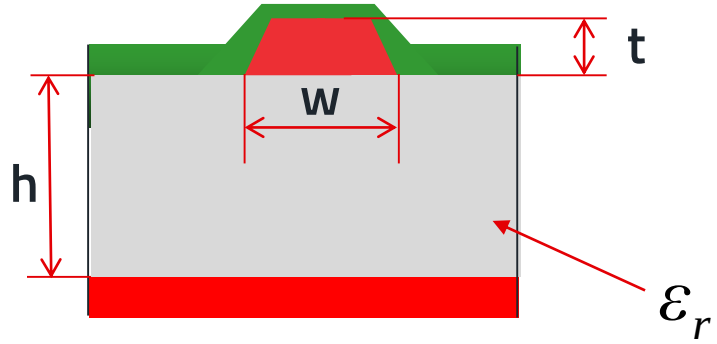

Lagenaufbau
IPC
Anforderungen
Technology-
Auswahl
Design
Bauteile
Impedanz
Anforderungen
Design
Rules
Aufwand bei der PCB-
Herrstellung

IMPEDANCE – INTRODUCTION

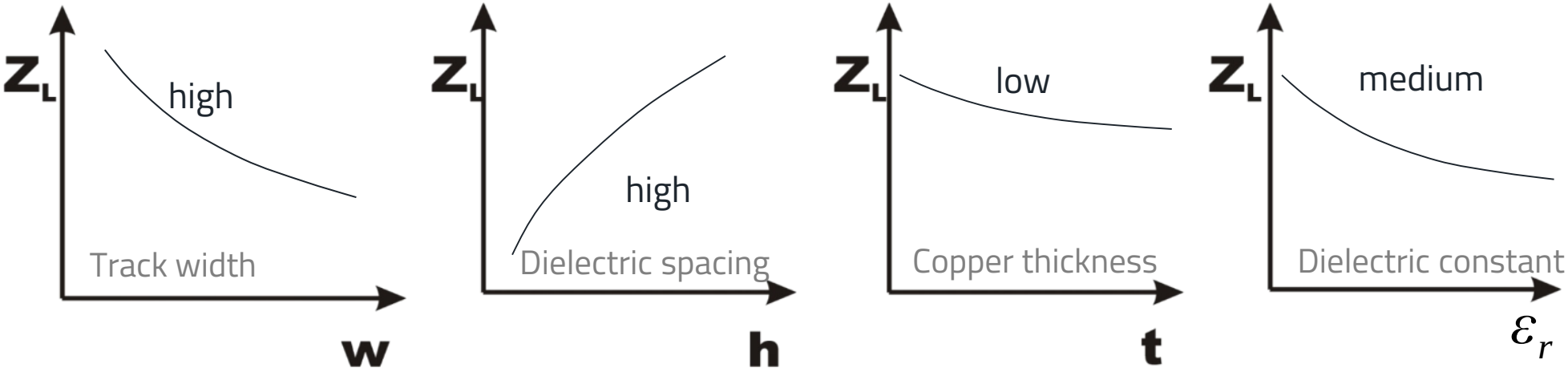
Surface Microstrip - IPC-2141

$$Z_0 = \frac{87.0}{(\varepsilon_r + 1.41)^{1/2}} \ln\left[\frac{5.98h}{0.8w + t}\right]$$

Z_0 = Impedance
E_r = Dk = Dielectric Constant
h = Dielectric Thickness
w = Track Width
t = Track Thickness



IMPEDANCE – INFLUENCING FACTORS



Z_L = Impedance
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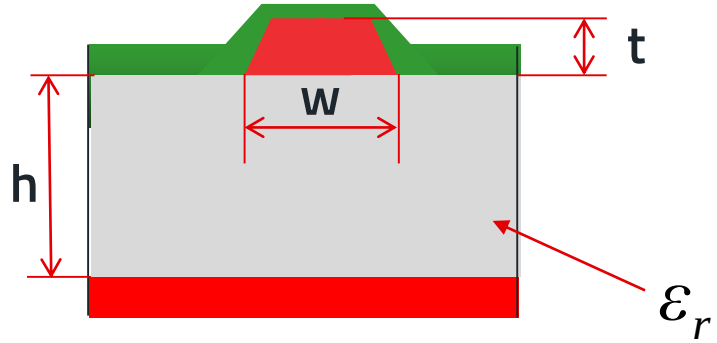


w+h = Designer + PCB manufacturer

t = Electroplating process, base copper

ε_r = Base Material

IMPEDANCE – INTRODUCTION

Types of Struktures

Single Ended
Coated Microstrip

Differential Pair
Edge Coupled Coated
Microstrip

Differential Pair
Embedded Coplanar Strips

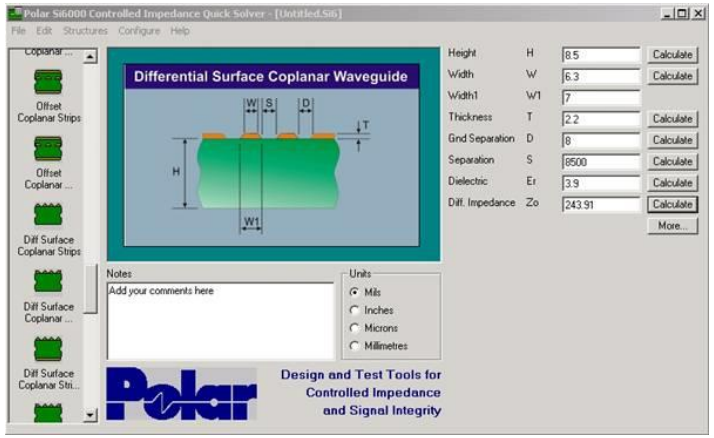
And many, many more…

SUPPORT: If you need an Impedance controlled Stack up feel free to contact us hdi@we-online.com

IMPEDANCE REQUIERMENTS

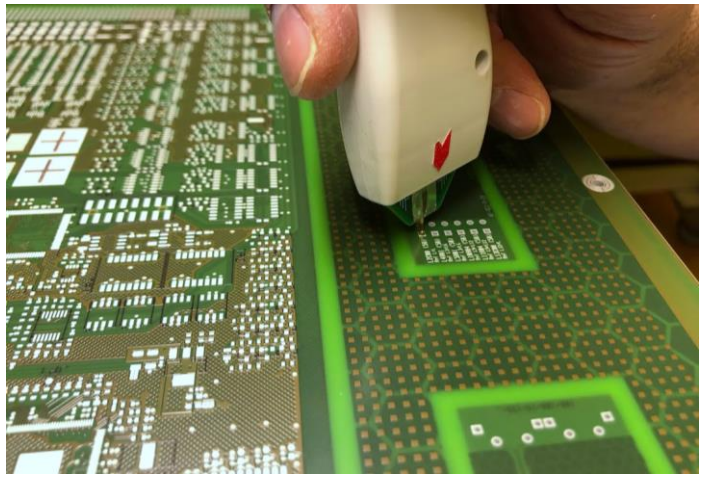
Defined by Component choice

- Impedance Calculation



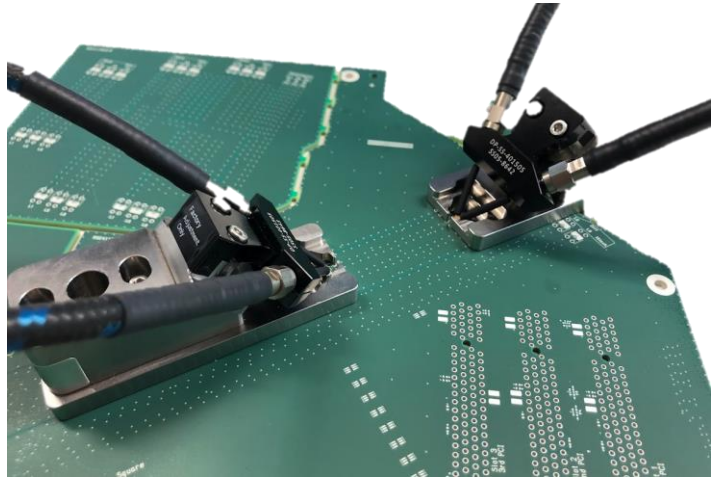
- Material Selection
- Design Rules
- Process Tolerance

- Impedance Measurement



- Process Control

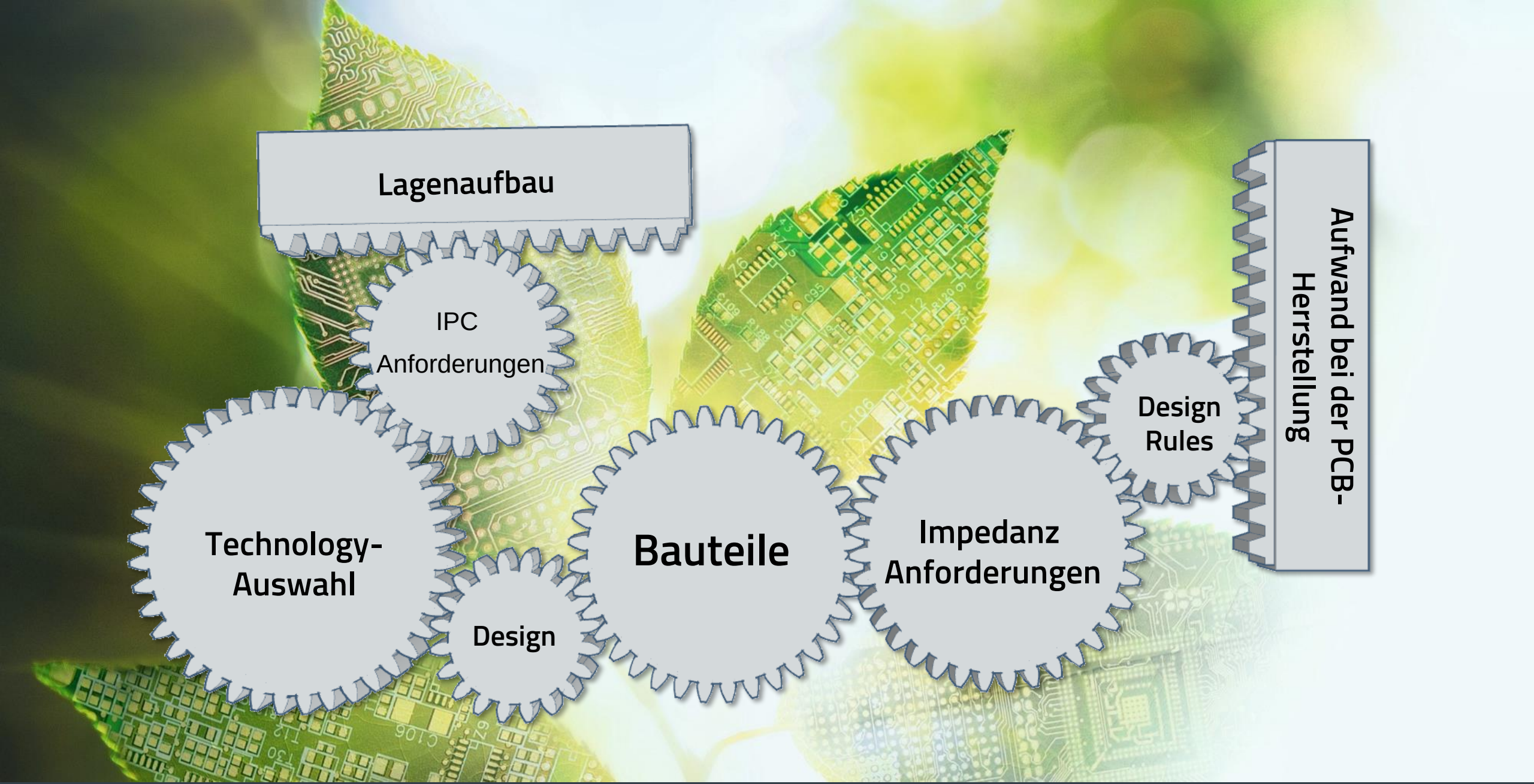
- HIGHSPEED Measurement „Atlas“



- Helping customer with
  - Material Choice
  - Design Rules
- Research & Development

AGENDA

1. Einführung in Impedanzen
2. Lagenaufbauten
3. High Speed Materialien
4. Best Practice Beispiele


Lagenaufbau
IPC
Anforderungen
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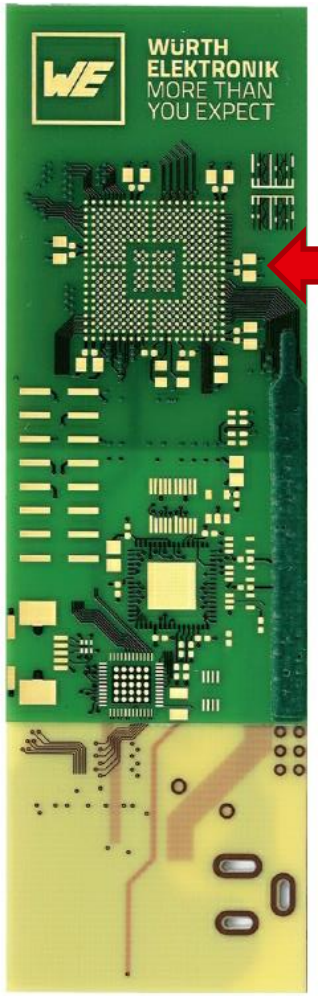
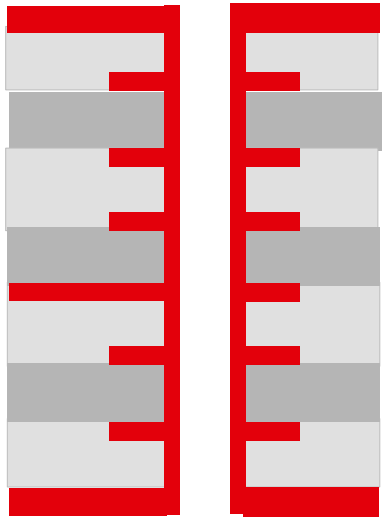
Design
Bauteile
Impedanz
Anforderungen
Design
Rules
Aufwand bei der PCB-
Herrstellung

ENTFLECHTUNG BGA

WE.fan

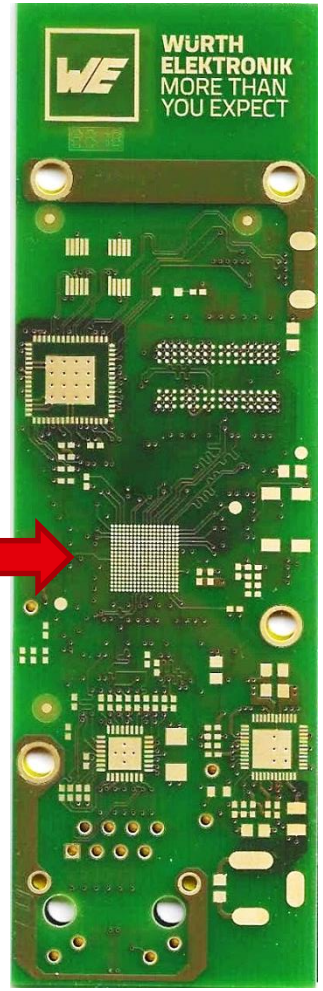


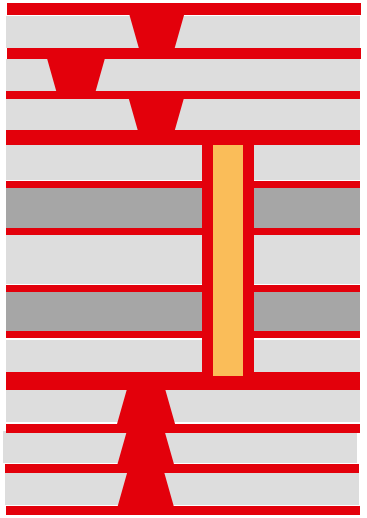
BGA
Pitch 0,80 mm



WE.microbga

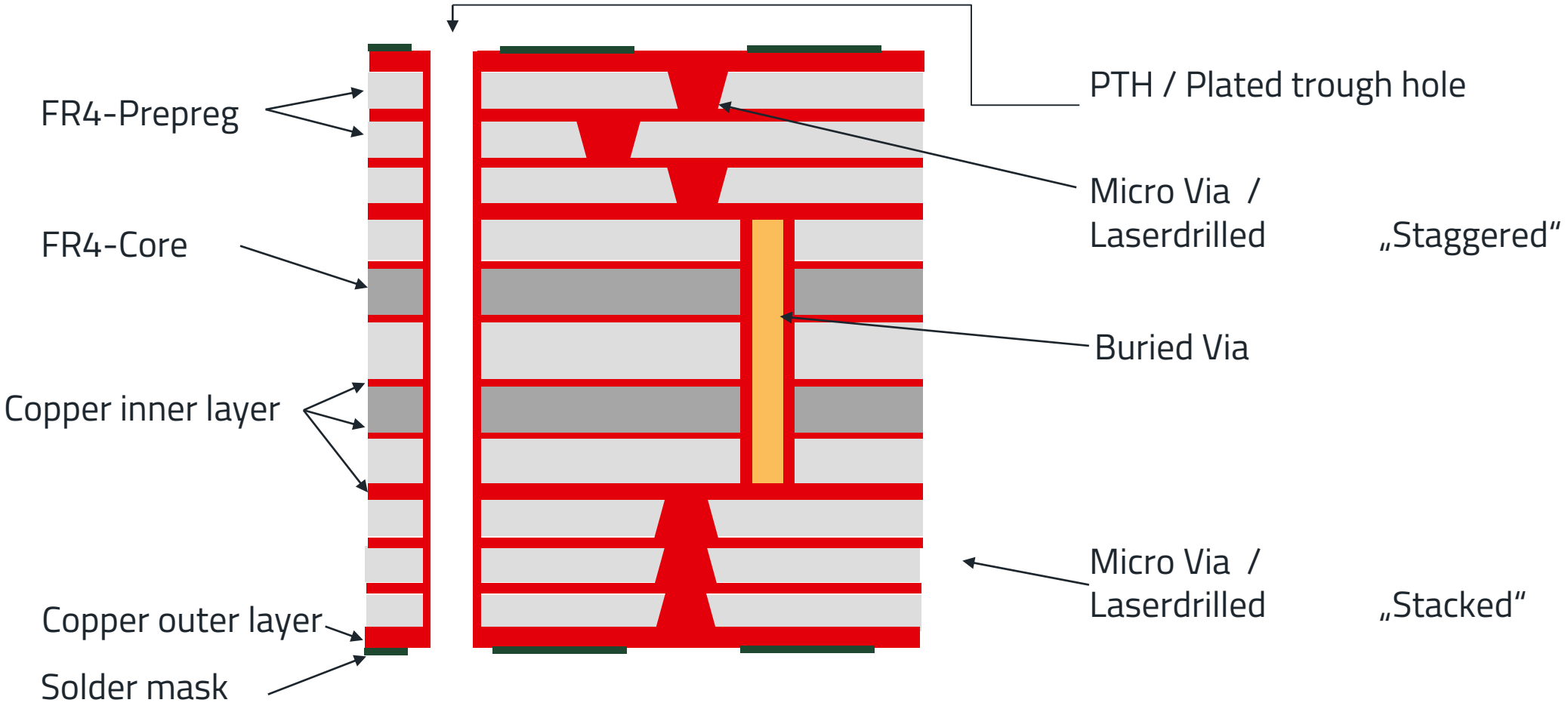
BGA
Pitch 0,40 mm





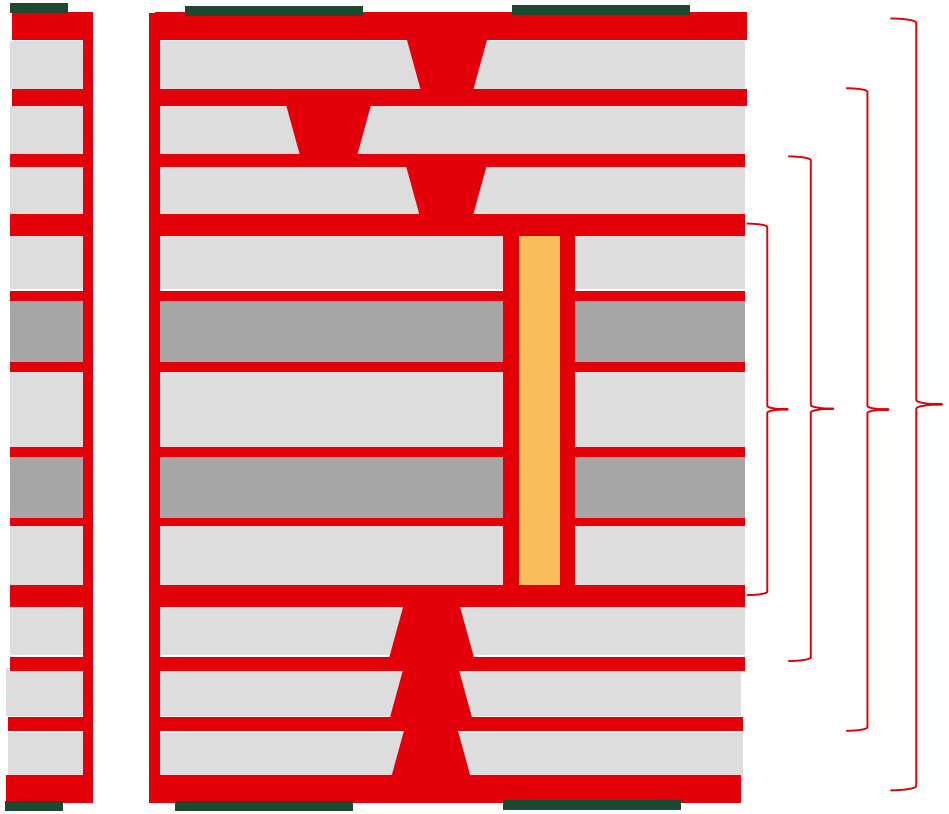
OVERVIEW STACKUP

HDI12 **3-6b-3**



CONSTRUCTION OF A HDI PCB

HDI12 **3-6b-3**



6x Galvanic Processes

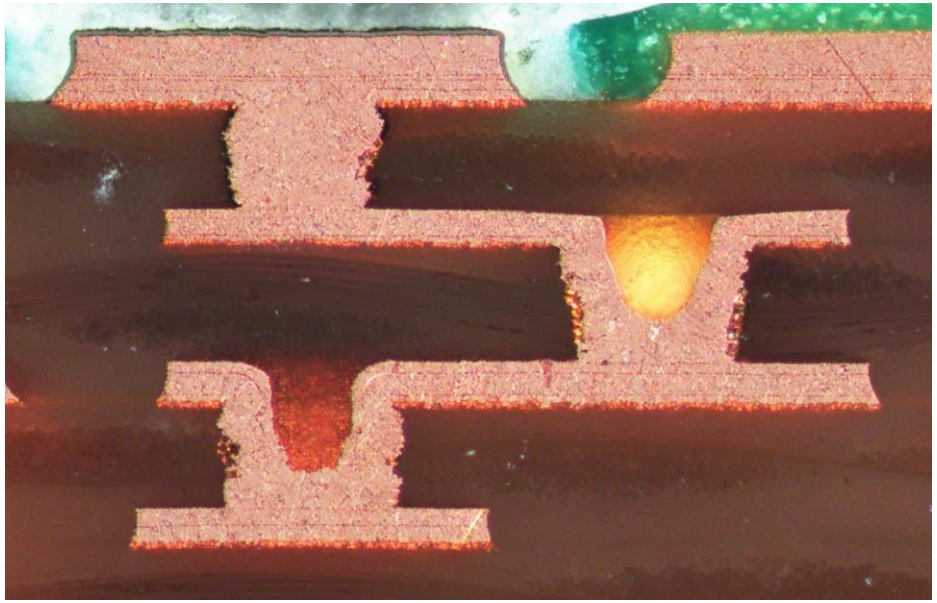
5x Photo Processes

4x Press cycles

HDI MICRO VIA

Technology Choice

„Staggered“ Micro Via

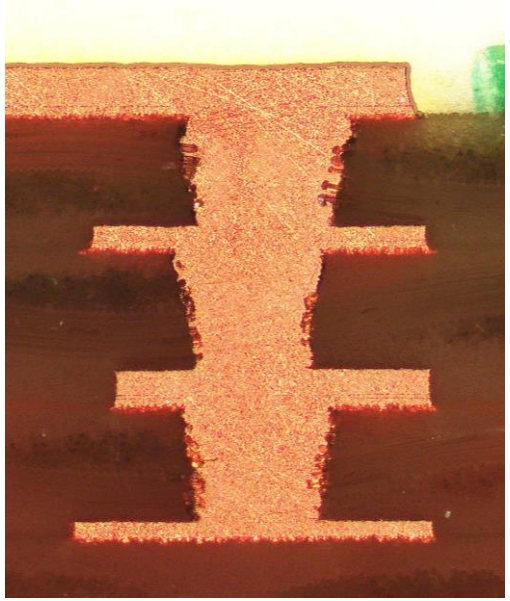


Copper filled

Filling Resin filled

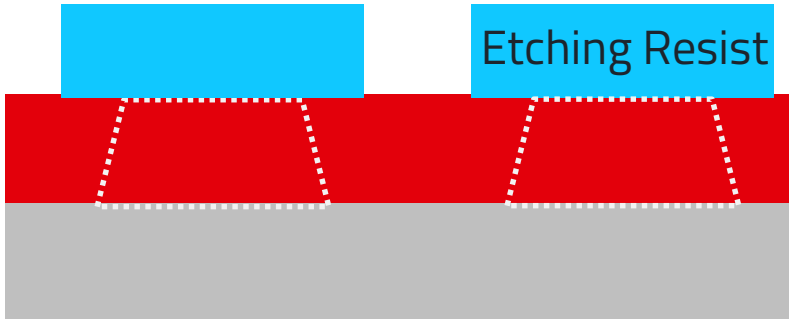
Prepreg Resin filled

„Stacked“ Micro Via

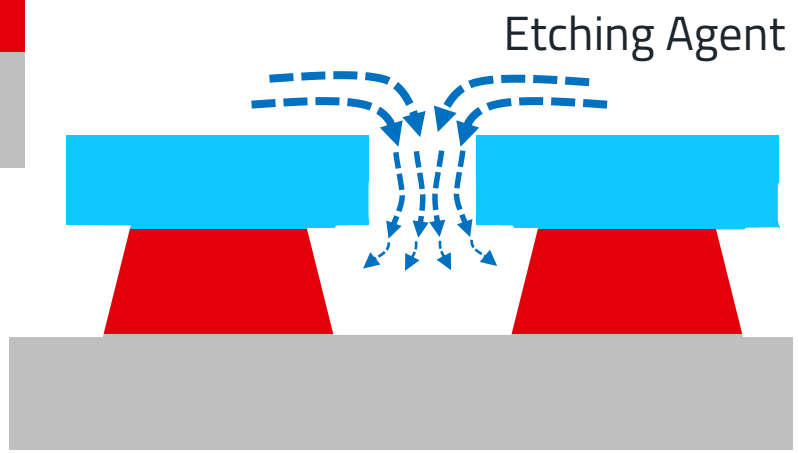


Early discussion between Project Partners results in Potential multiplication

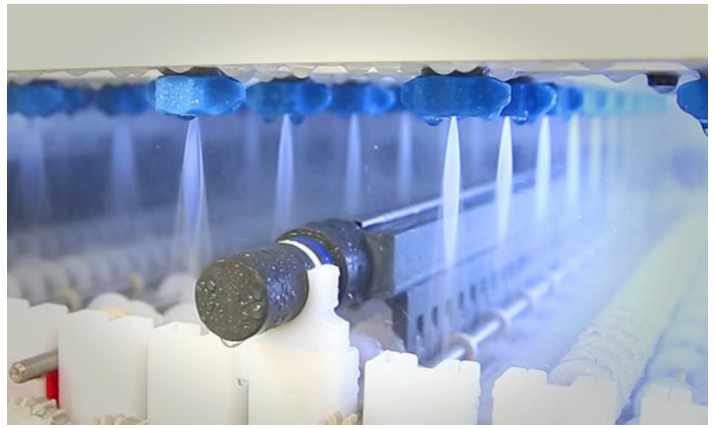
BASICS: PRODUCTION OF A PCB – INNER LAYERS



Lamination of Resist & Develop



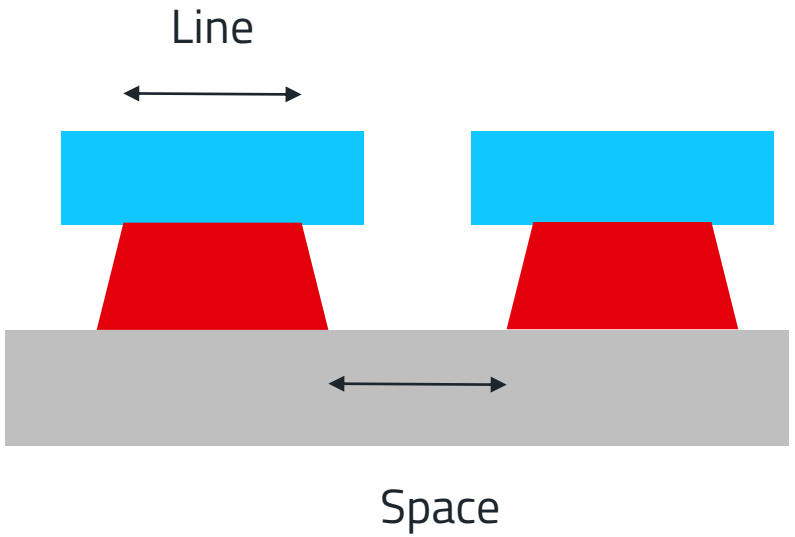
Etching



Quelle schmid-group.com

Stripping

CORELATION BETWEEN COPPER THICKNESS AND LINE WIDTH

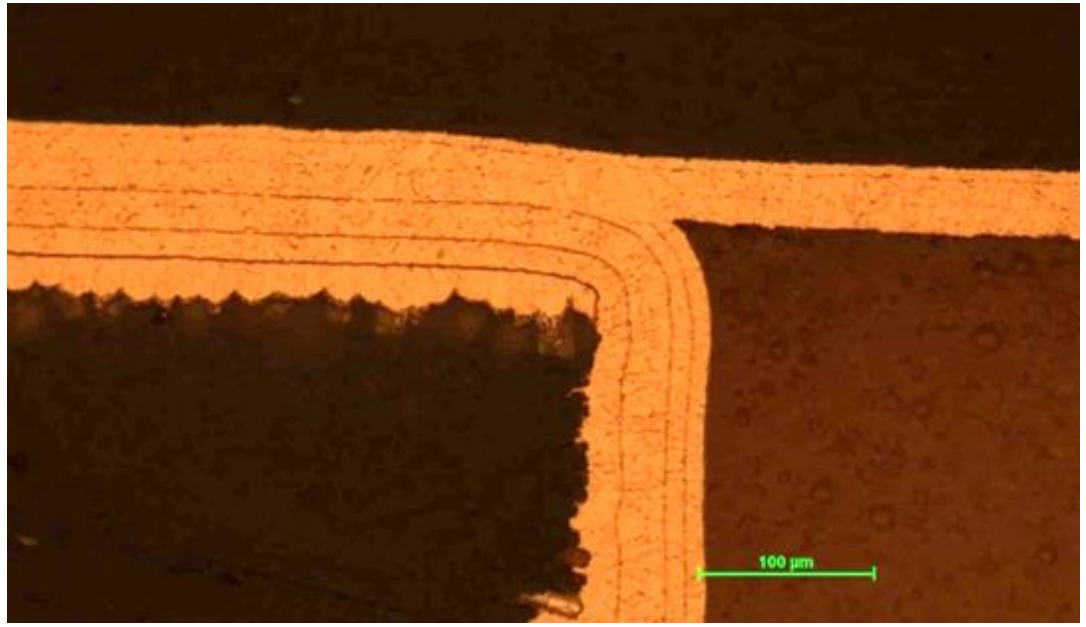


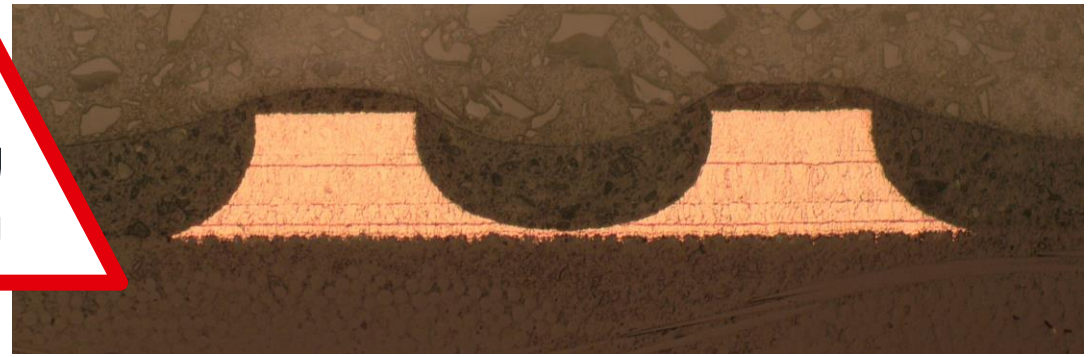
Outer layers – conductor spacing					
Starting foil thickness	**Minimum copper thickness[1]**		**Nominal final thickness**	**Minimum conductor spacing Standard**	**Minimum conductor spacing Advanced**
	IPC-class 1, 2	IPC-class 3			
8,5 µm [1/4 oz.][2]	26,2 µm	31,2 µm		100 µm	75 µm
12 µm [3/8 oz.][2]	29,3 µm	34,3 µm		100 µm	80 µm
17,1 µm [1/2 oz.]	33,4 µm	38,4 µm	35 µm	120 µm	100 µm
34,3 µm [1 oz.]	47,9 µm	52,9 µm	70 µm	180 µm	160 µm
68,6 µm [2 oz.]	78,7 µm	83,7 µm	105 µm	275 µm	225 µm
102,9 µm [3 oz.]	108,6 µm	113,6 µm		390 µm	320 µm
1) IPC-6012E-EN Table 3-15: External Conductior Thickness after Plating					
2) Extra cost: No standard copper foil					
3) Outer layers: only possible with uniform circuit layout					

Inner layers - conductor spacing					
Starting foil thickness	**Minimum copper thickness[4]**			**Minimum conductor spacing Standard**	**Minimum conductor spacing Advanced**
	IPC-class 1, 2, 3				
17,1 µm [1/2 oz.]	11,4 µm			100 µm	75 µm
34,3 µm [1 oz.]	24,9 µm			120 µm	100 µm
68,6 µm [2 oz.]	55,7 µm			180 µm	150 µm
102,9 µm [3 oz.]	86,6 µm			250 µm	225 µm
4) IPC-6012E-EN Table 3-14: Internal Layer Foil Thickness after Processing					

FILLED VIA – TECHNOLOGY COMBINATION

Limitations with fine line structures

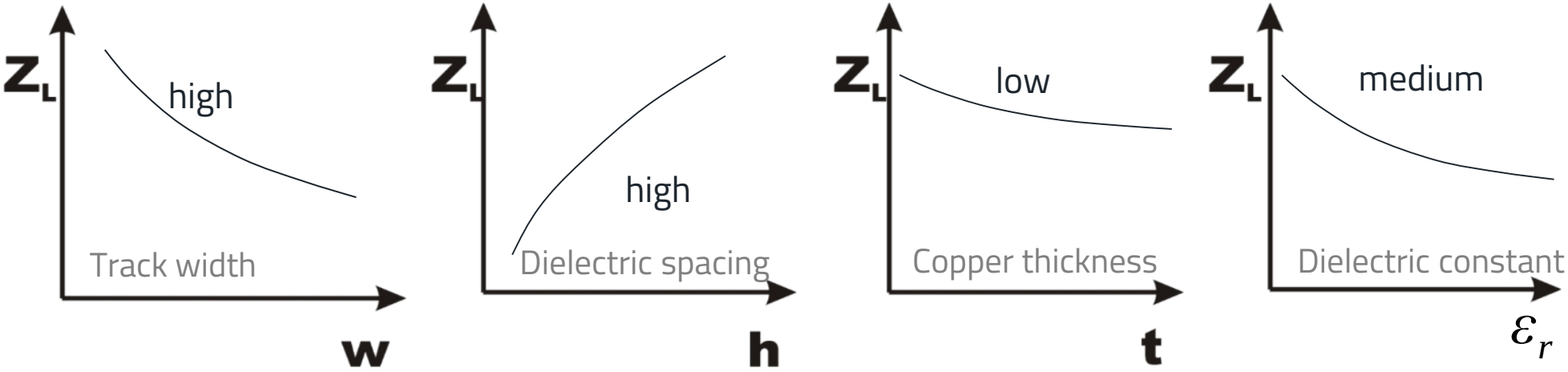




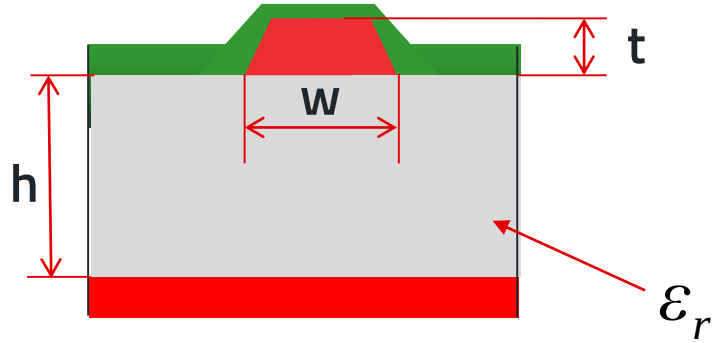
Due to repeated electroplating, the copper rises on the surface. This means that compromises in the structure sizes are sometimes necessary.

Typical design parameters depending on the Cu thickness		
Copper-Thickness	Line width	Space
~ 30 µm	100 µm	100 µm
~ 40 µm	125 µm	120 µm
~ 50 µm	150 µm	180 µm

IMPEDANCE – INFLUENCING FACTORS



Z_L = Impedance
E_r = Dk = Dielectric Constant
h = Dielectric Thickness
w = Track Width
t = Track Thickness



w+h = Designer + PCB manufacturer

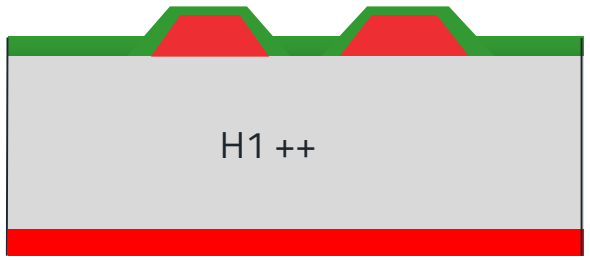
t = Electroplating process, base copper

ε_r = Base Material

BEST COMBINATION ?

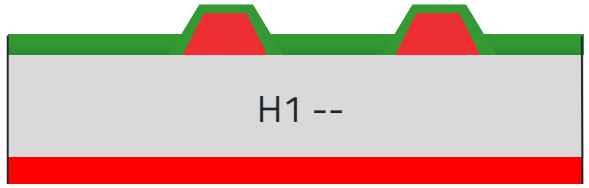
100 Ω

W1++ & D1--



100 Ω

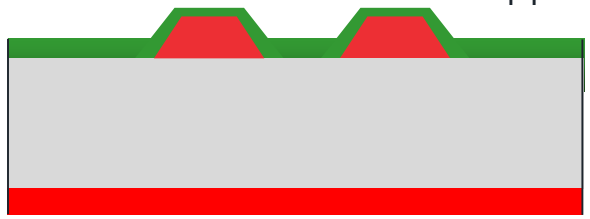
W1-- & D1++



100 Ω

D1+

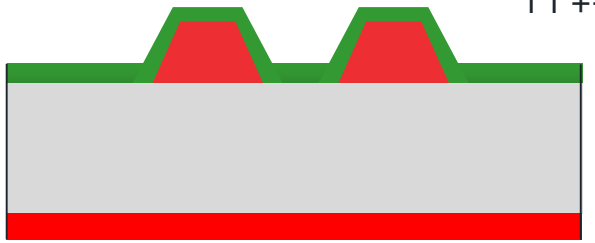
T1 --



100 Ω

D1-

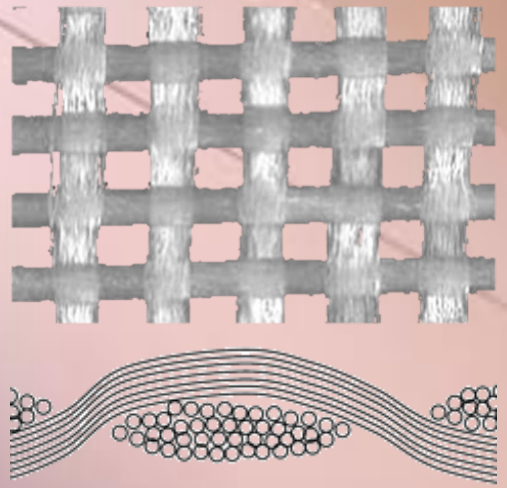
T1 ++

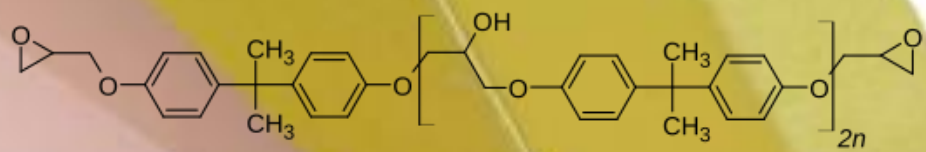


AGENDA

1. Einführung in Impedanzen
2. Lagenaufbauten
3. High Speed Materialien
4. Best Practice Beispiele

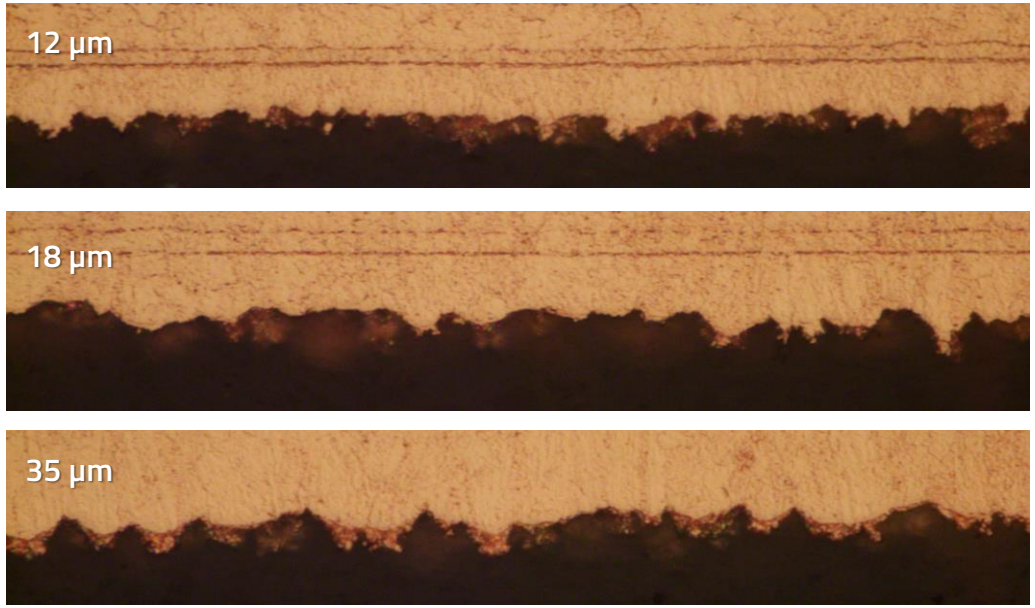
BASE MATERIAL FR4



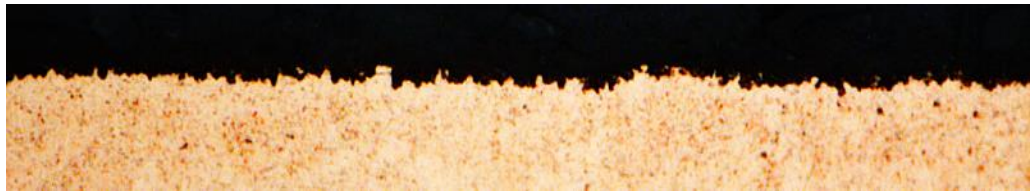


COPPERFOIL ROUGHNESS

- **Treatment**



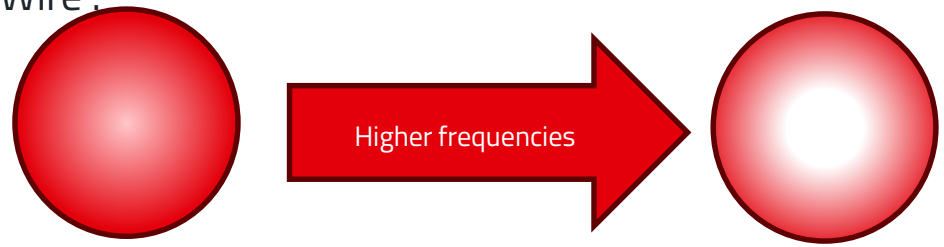
- **Shine + Adhesion Promoter**



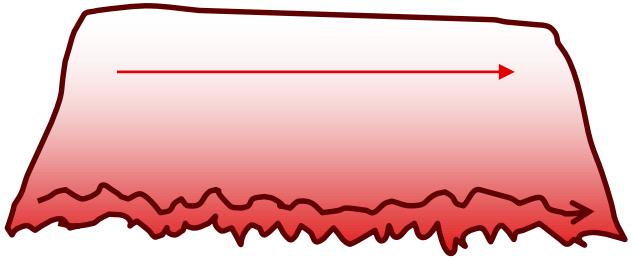
- **Skin-Effect**

In simple terms, the skin effect is the tendency for alternating current (AC) to flow mostly near the outer surface (or "skin") of a conductor, rather than throughout its entire cross-section, especially at higher frequencies ~ 3 Ghz and more.

Wire :



Trace:



CONSTRUCTION OF PREPREG

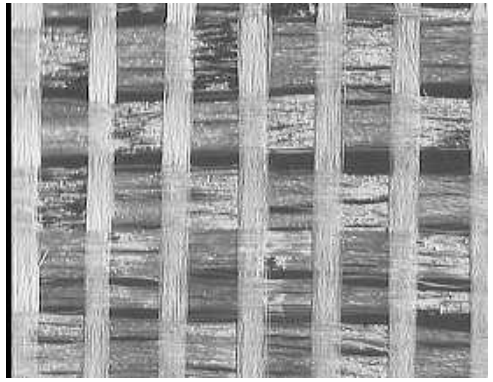
Example values

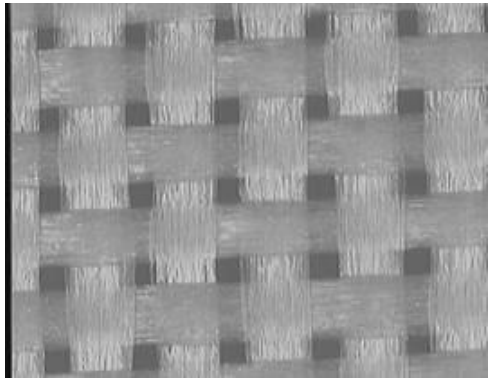
FR4 Prepreg 106

Thickness 50 µm

ε_r = 2,8 – 3,7

Resin content ~70%





FR4 Prepreg 2116

Thickness 90 – 110 µm

ε_r = 3,6 – 3,8

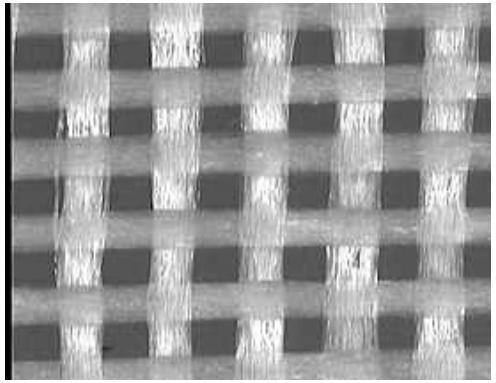
Resin content ~50%

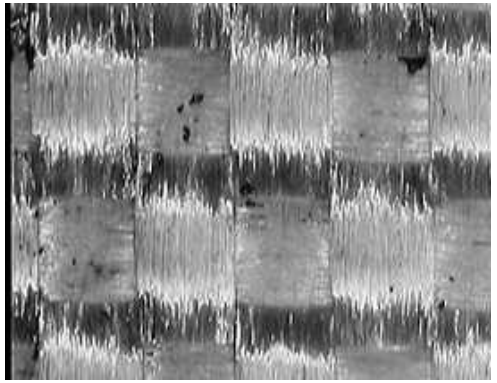
FR4 Prepreg 1080

Thickness 60 - 70 µm

ε_r = 3,2 – 3,7

Resin content ~60%





FR4 Prepreg 7628

Thickness 170 – 190 µm

ε_r = 4,1 – 4,6

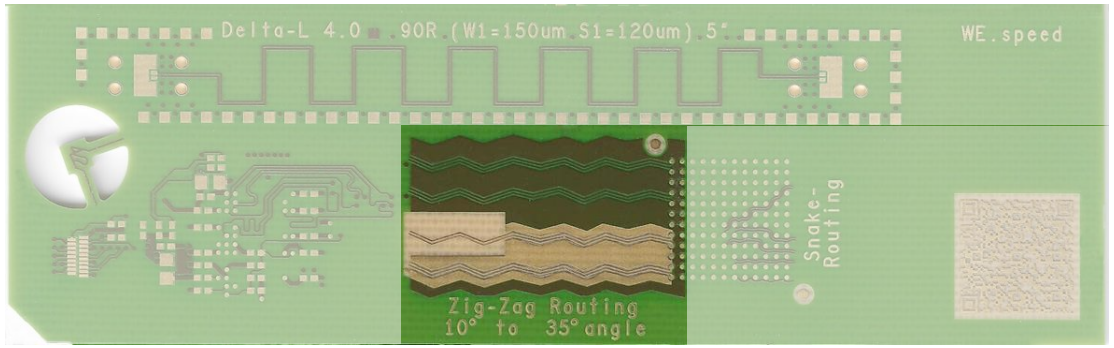
Resin content ~45%

glass εr ~6,1 / resin εr ~3,2

Cores are laminated Prepreg

HIGH.SPEED PHYSICAL PCB SAMPLE

Zig-Zag Routing

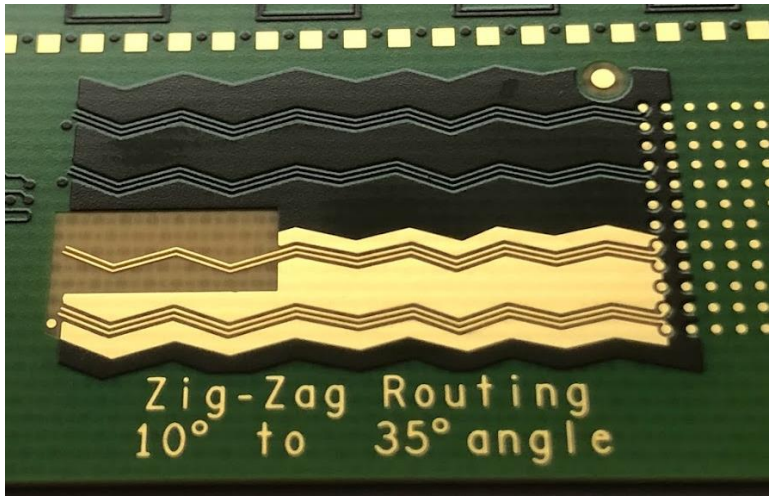


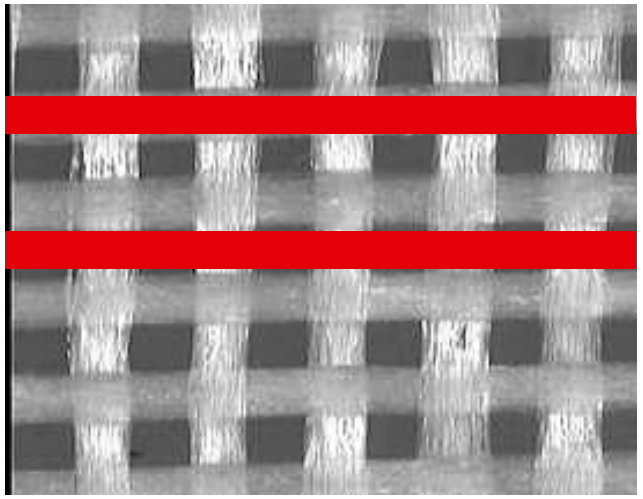
- kleinerer Fiber-Weave Effect

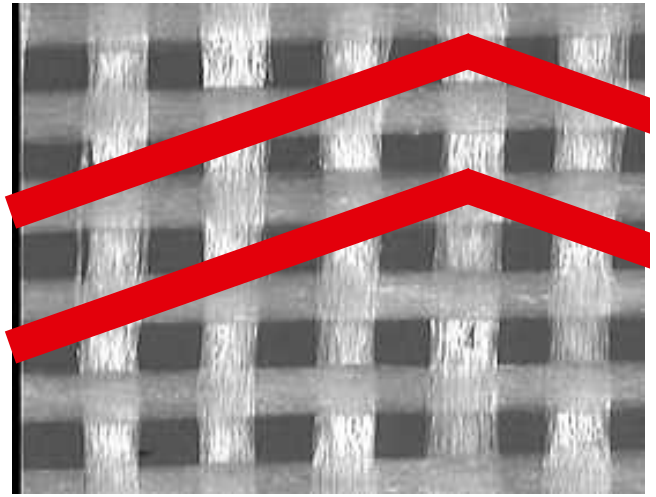
  Dk / E_R Glas ~6.1

  Dk / E_R Fr4-Resin ~3.2

- Used in Customer application **WEdesign** Team 20-22-GHz

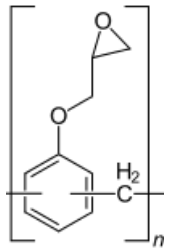




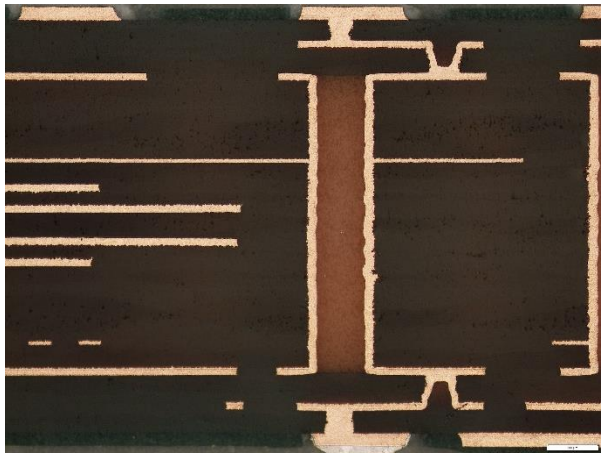


MATERIAL COMPARISION

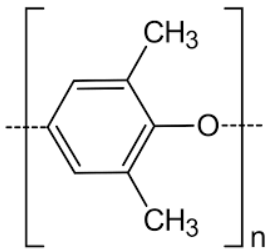
FR4 Epoxy-Resin



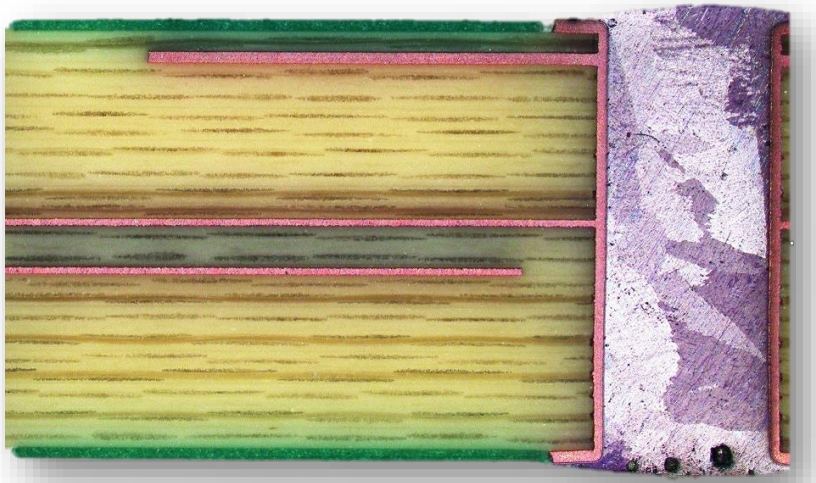
- Tg 130 – 180°C
- Dk 4.37 Df 0.022 at 1 GHz
- Without or with Fillers



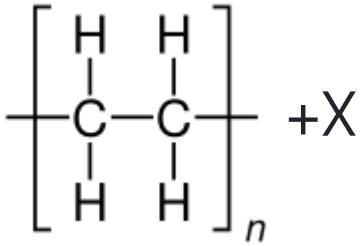
Megtron 6 PPE-Resin



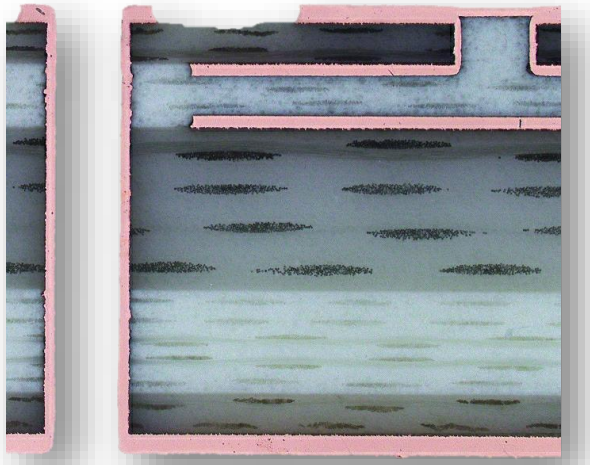
- Tg 185°C
- Dk 3.61 Df 0.0040 at 10 GHz
- With Fillers



Rogers Hydrocabon-Resin



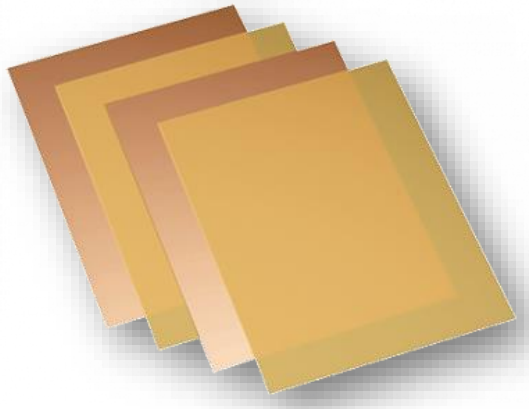
- Tg > 280°C
- Dk 3.48 Df 0.0037 at 10 GHz
- With ceramic Fillers



MATERIAL VERGLEICH

Einfluss neuerer Basismaterialien

Roh-Material

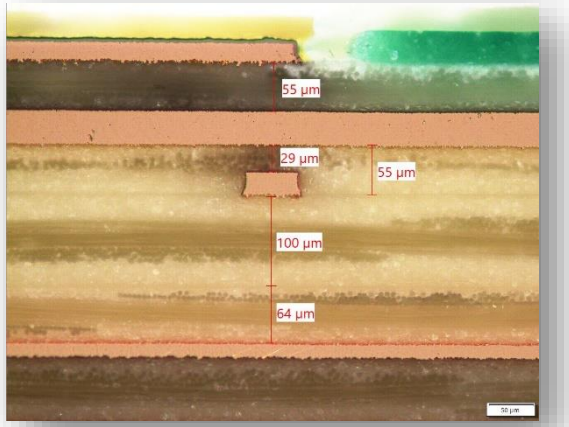


Beschaffungspreis
4x - 20x
zu Tg150 Material

Nass-Prozesse

Aggressive Chemie
notwendig

Multilayer Verpressen

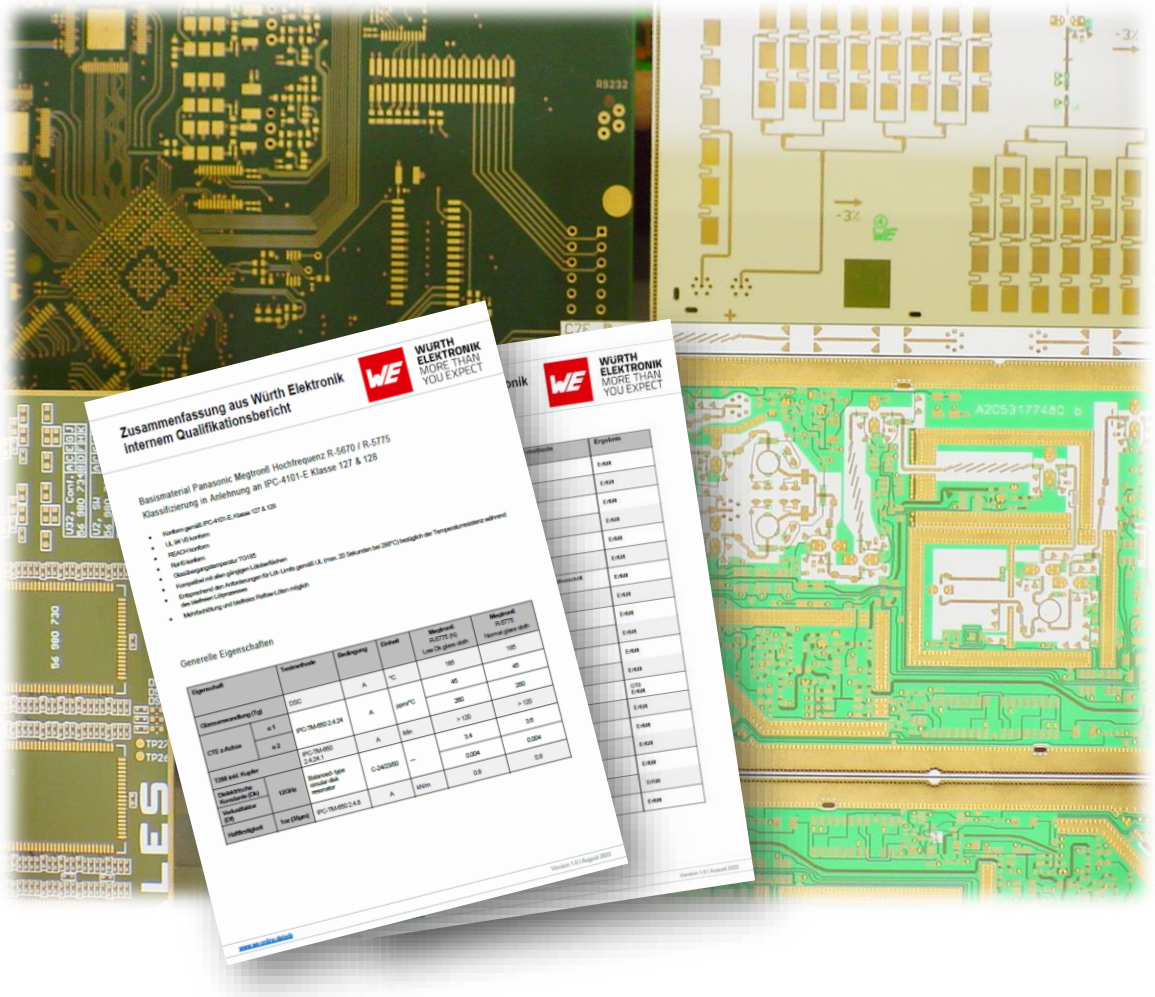


Höhere Temperaturen
und mehr Zeit notwending

Mech. Parameter

Mehr
Werkzeugverschleiß

QUALIFIED MATERIALS



For analog and digital High Speed applications

Panasonic

MEGTRON6

Dk 3.61

Dissipation factor 0.0040 at 10 GHz

UL LISTED

For special applications

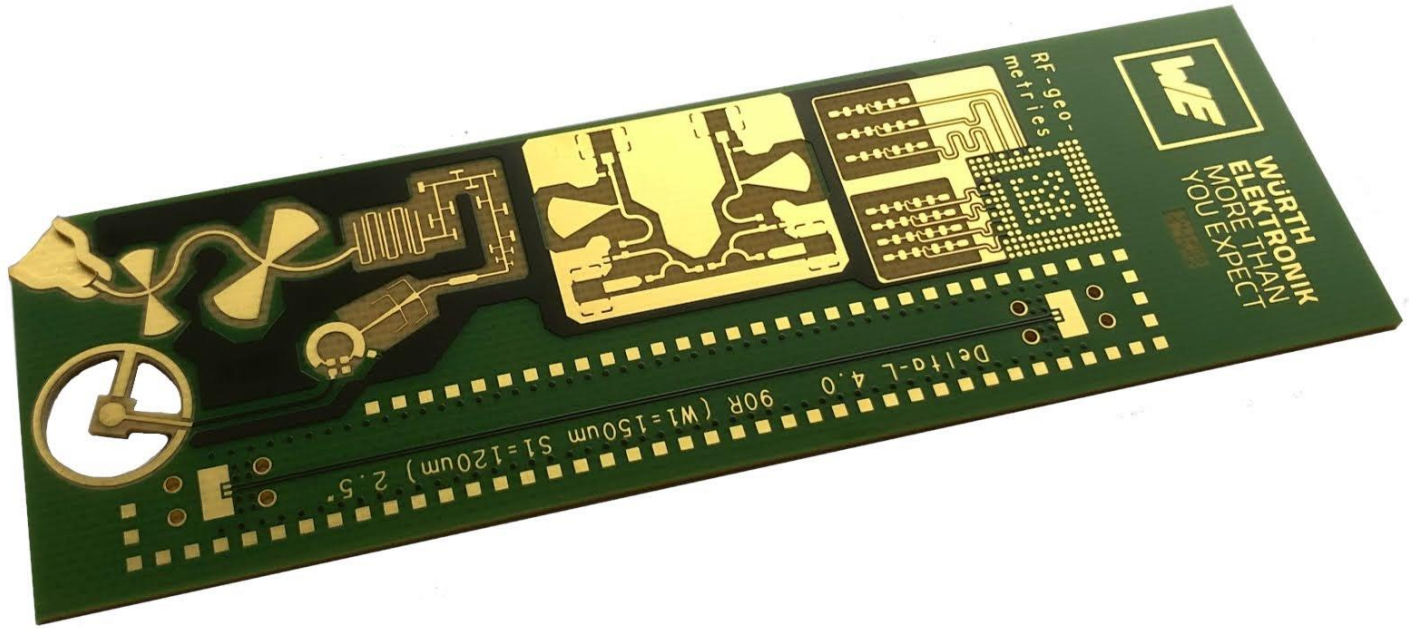
ROGERS CORPORATION

4000-Family

Dk of 3.48

Dissipation factor of 0.0037 @10 GHz

HIGH.SPEED PHYSICAL PCB SAMPLE



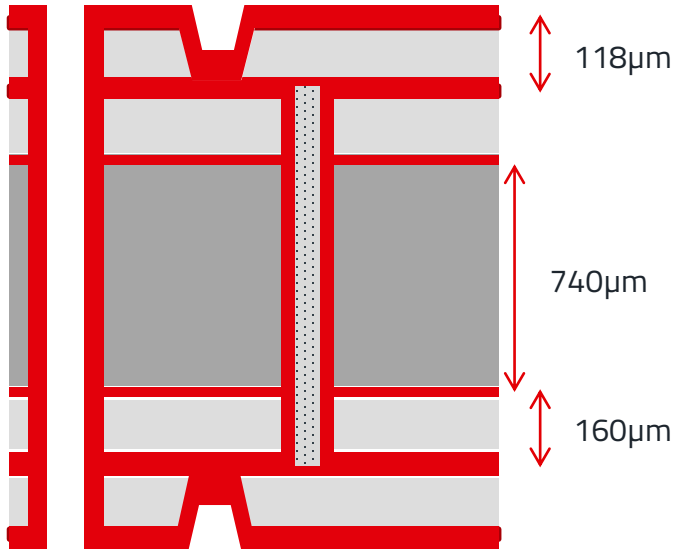
Bestellen Sie ihr kostenloses Muster heute !

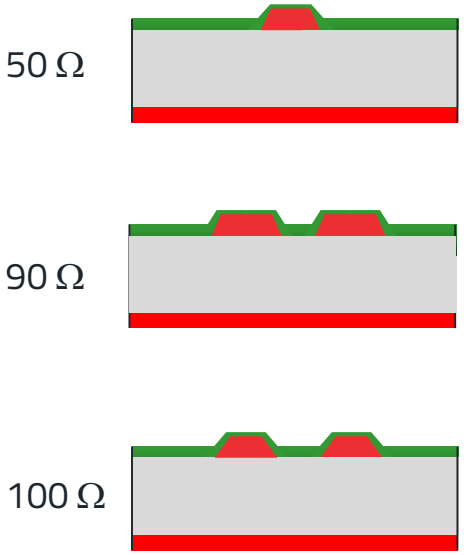
https://www.we-online.com/we-speed

HIGH.SPEED PHYSICAL PCB SAMPLE

Stackup

1+4b+1





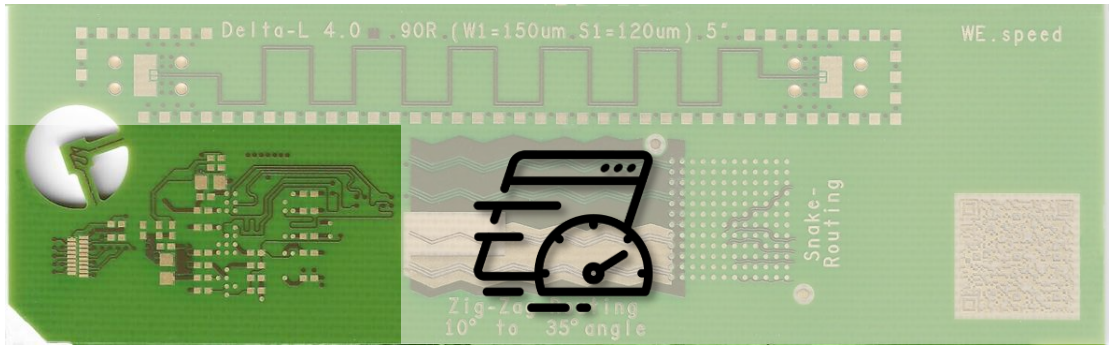
	Line Width	Line Space
Single Ended Coated Microstrip	208 µm	
Differential Pair Edge Coupled Coated Microstrip	150 µm	120 µm
Differential Pair Edge Coupled Coated Microstrip	123 µm	138 µm

Base material: Panasonic Megtron 6

SUPPORT: If you need an Impedance controlled Stack up feel free to contact us hdi@we-online.com

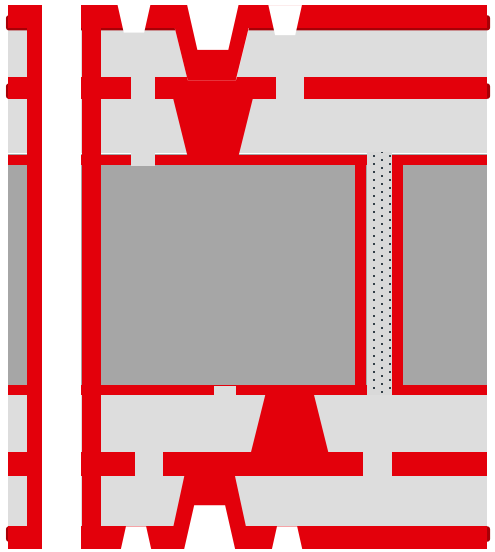
HIGH.SPEED PHYSICAL PCB SAMPLE

HDI-Design

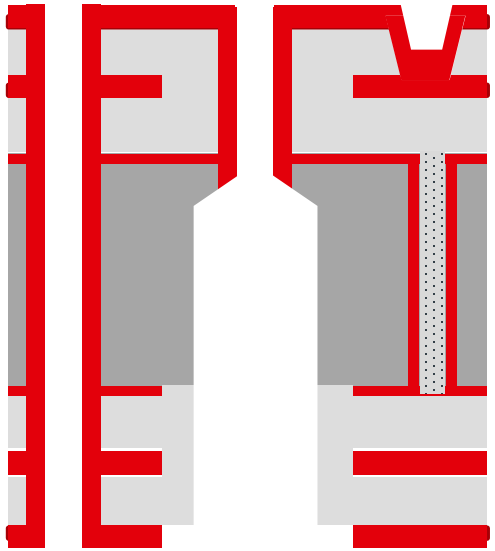


Use Micro Via as much as possible

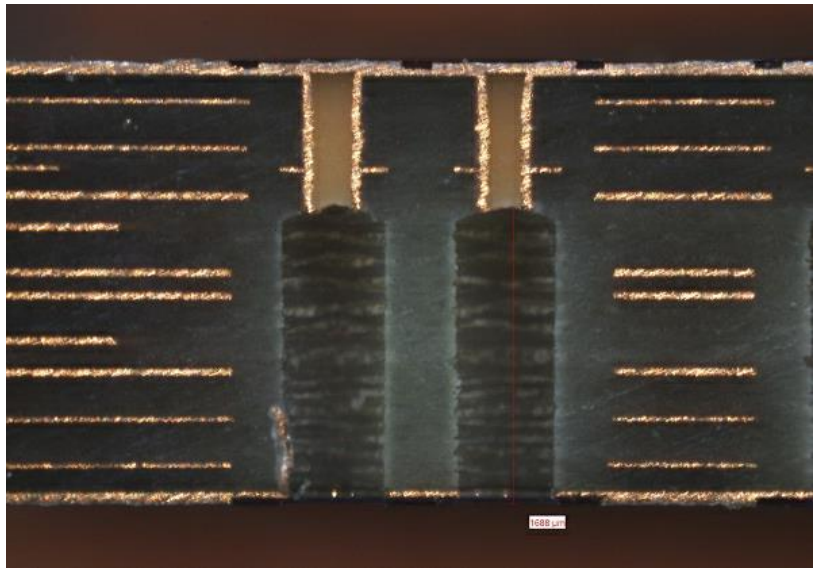
- Small footprint
- Short stub length
- In volume minimal extra cost → Stitching Via
- More reliable than Back Drilling



HDI- Approach

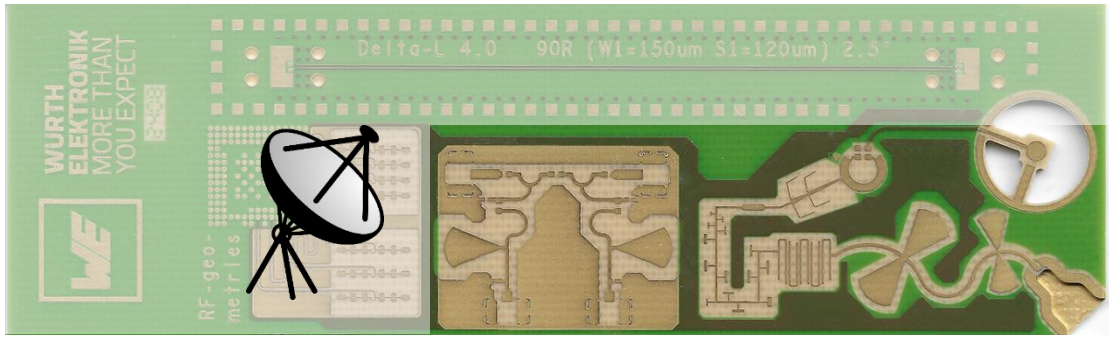


Back Drilling



HIGH.SPEED PHYSICAL PCB SAMPLE

RF Filters & Antennas



- Be creative!

Possible Connection for a waveguide

Depth Milling

Edge Metallisation

Etching

AGENDA

1. Einführung in Impedanzen
2. Lagenaufbauten
3. High Speed Materialien
4. Best Practice Beispiele

LINE/SPACE DEPENDENCY - PRACTICAL EXAMPLE

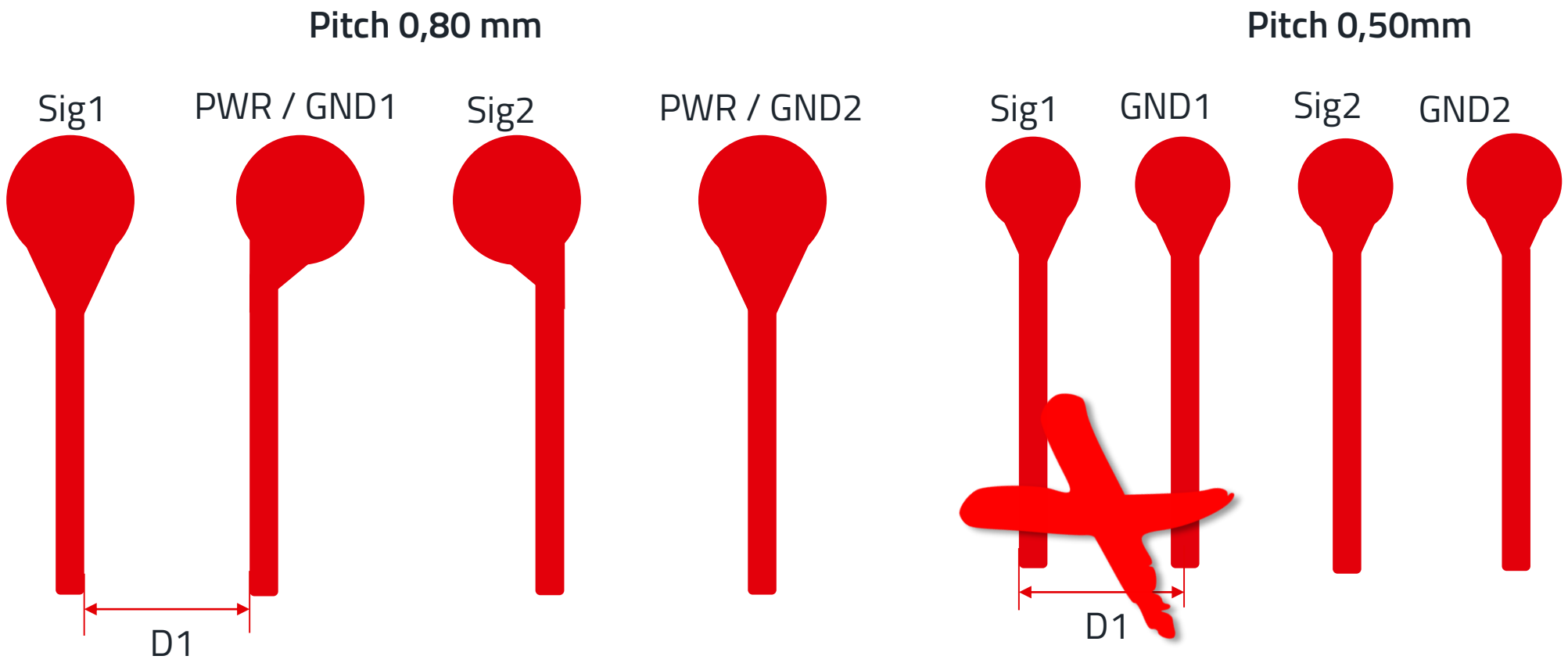
In narrow spaces: small conductor spacing

Rest of the layout: generous spacing
New data formats: Use attributes

Asymmetric layout definition

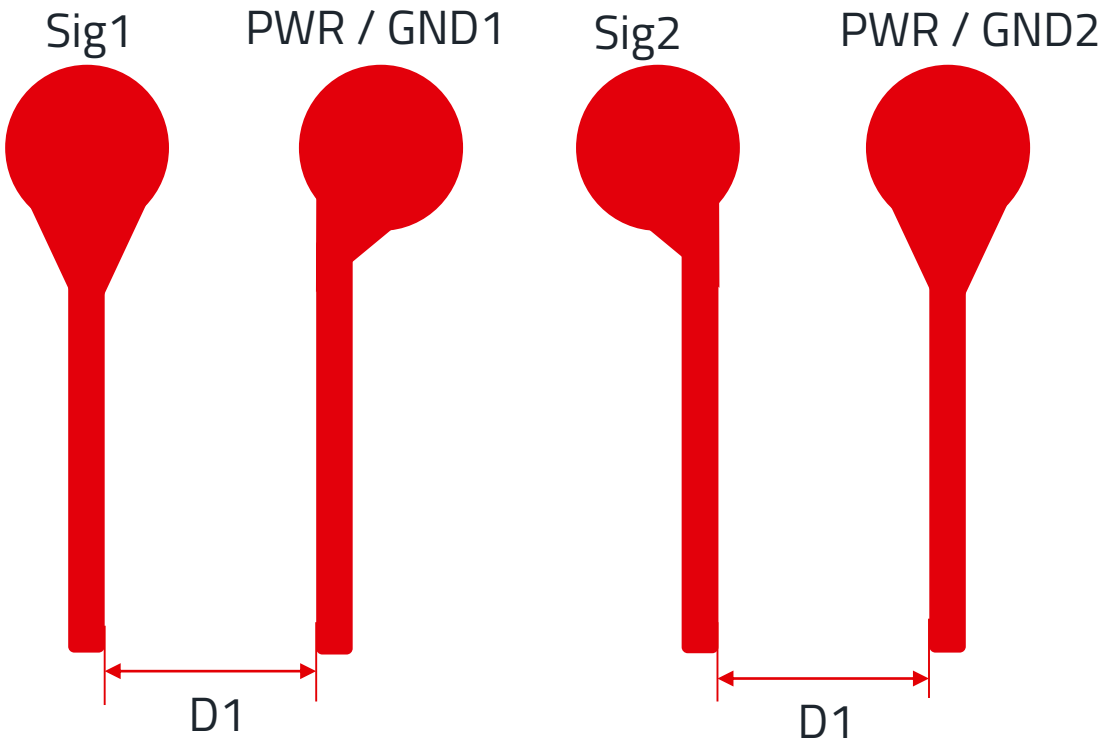
	Line/Space
Not	100/100 µm
but	80/120 µm

PITCH DEPENDENCY - PRACTICAL EXAMPLE

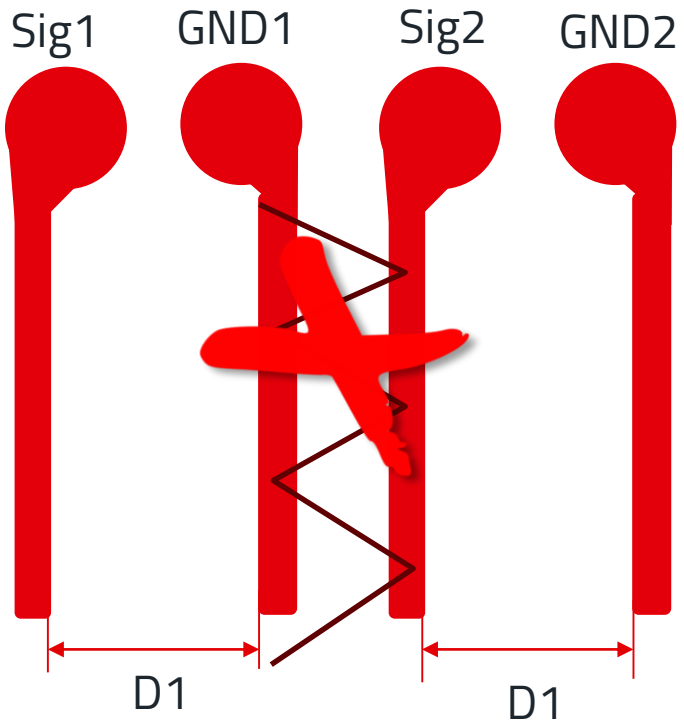


PITCH DEPENDENCY - PRACTICAL EXAMPLE

Pitch 0,80 mm



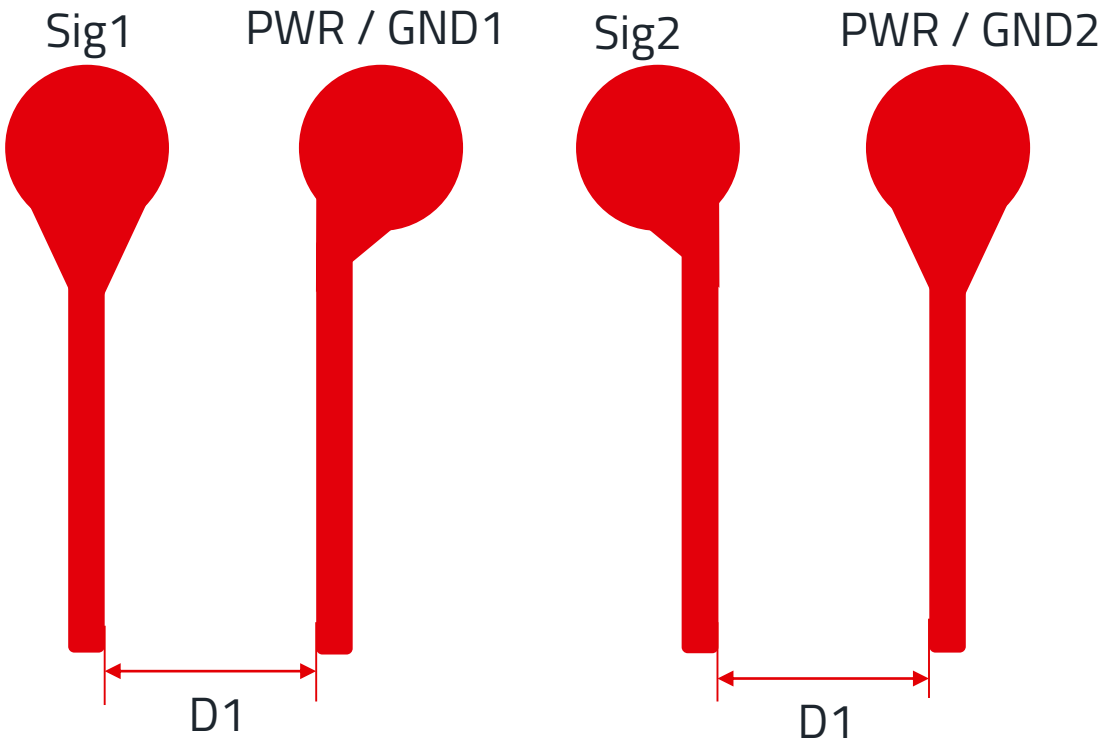
Pitch 0,50mm



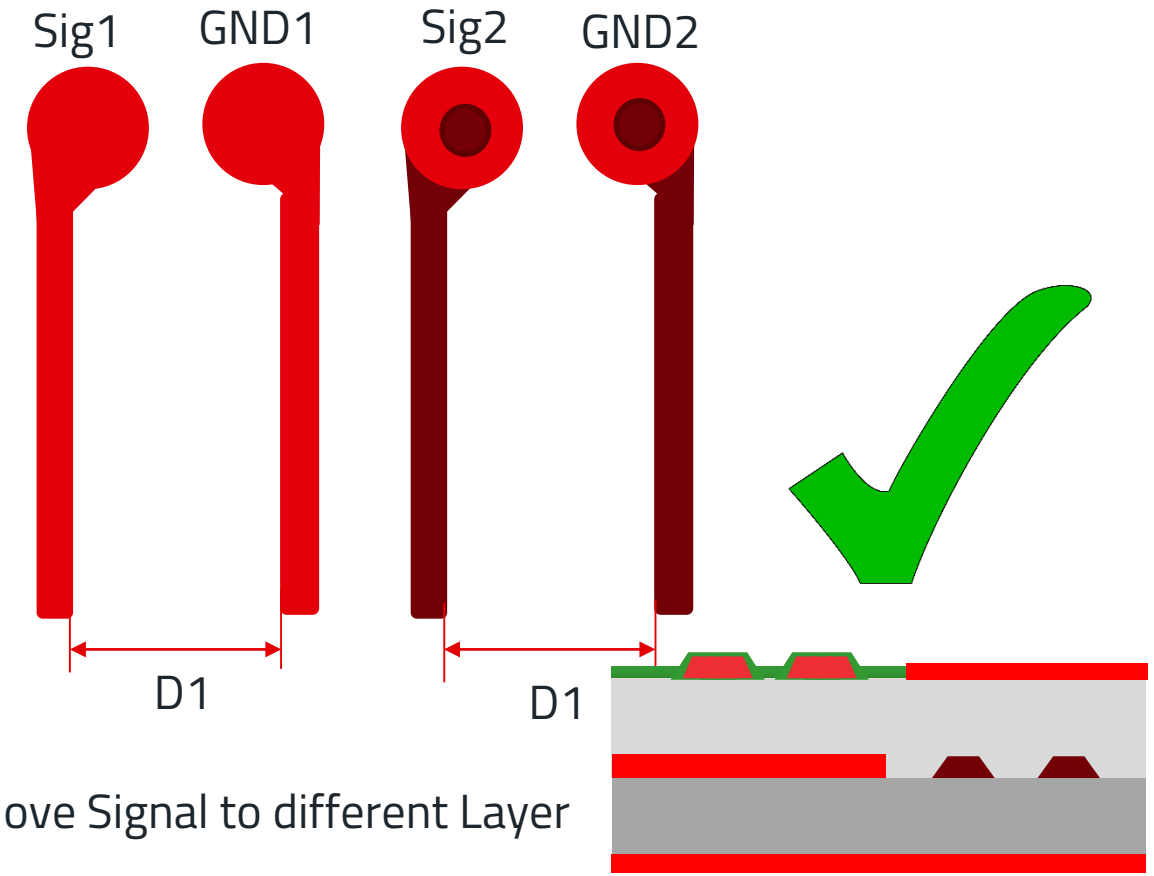
„Crosstalk Effekt“

PITCH DEPENDENCY - PRACTICAL EXAMPLE

Pitch 0,80 mm



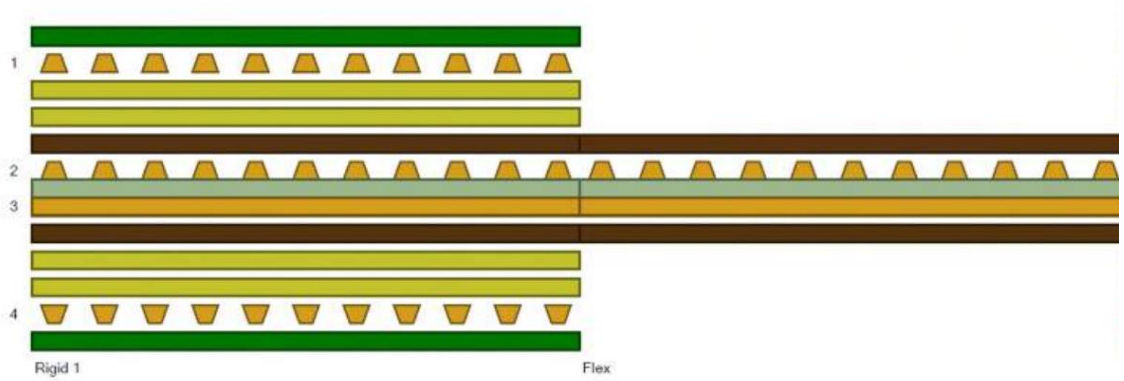
Pitch 0,50mm



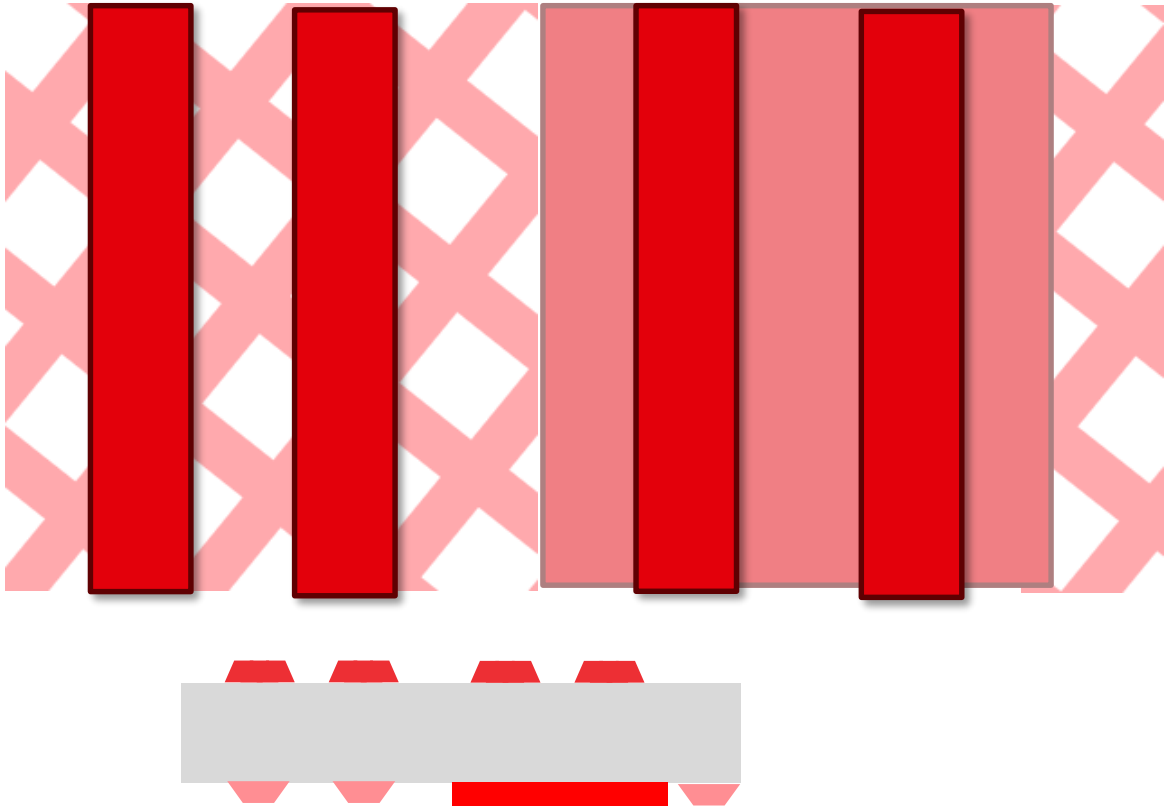
Move Signal to different Layer

FLEXIBLE STACKUP

Seperate Berechnung für jeden Bereich notwendig !



Lokale Geschlossene Massefläche hilfreich ?

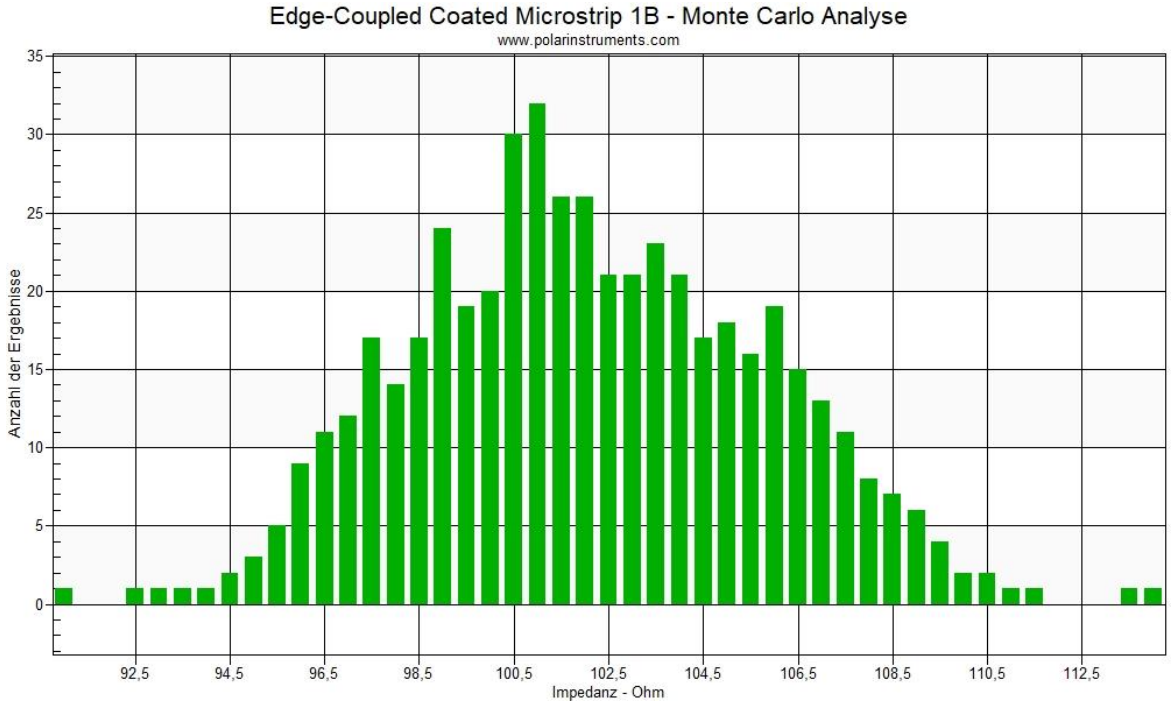


WENN SICH TOLERANZEN EINMISCHEN

Monte Carlo Simulation

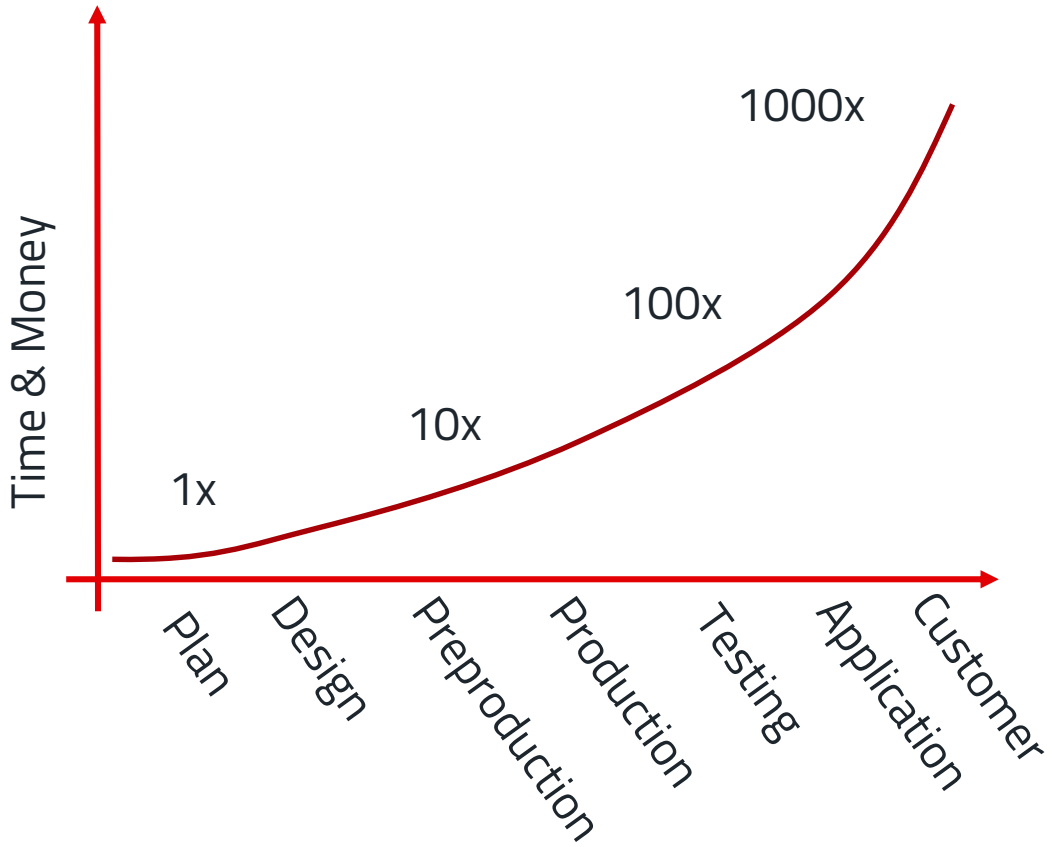
Substrat 1 Dicke	H1	118,00	±	20,00	98,00	138,00	118,00	6,67
Substrat 1 Dielektrikum	Er1	3,6000	±	0,2000	3,4000	3,8000	3,6000	0,0667
Untere Leiterbreite	W1	150,00	±	30,00	120,00	180,00	150,00	10,00
Obere Leiterbreite	W2	135,00	±	30,00	105,00	165,00	135,00	10,00
Leiterbahn Separation	S1	120,00	±	20,00	100,00	140,00	120,00	6,67
Leiterbahndicke	T1	40,00	±	5,00	35,00	45,00	40,00	1,67
Lackdicke auf Substrat	C1	25,40	±	10,00	15,40	35,40	25,40	3,33
Lackdicke auf Leiterbahn	C2	25,40	±	10,00	15,40	35,40	25,40	3,33
Lackdicke zw. Leiterbahnen	C3	25,40	±	10,00	15,40	35,40	25,40	3,33
Lack Dielektrikum	CEr	4,5000	±	0,2000	4,3000	4,7000	4,5000	0,0667

100 Ω



Innerhalb der IPC Toleranzen kann es im ungünstigsten Fall zu Impedanzabweichungen außerhalb der Spezifikation kommen –
daher ist eine sorgfältige und zuverlässige Parameterermittlung erforderlich.

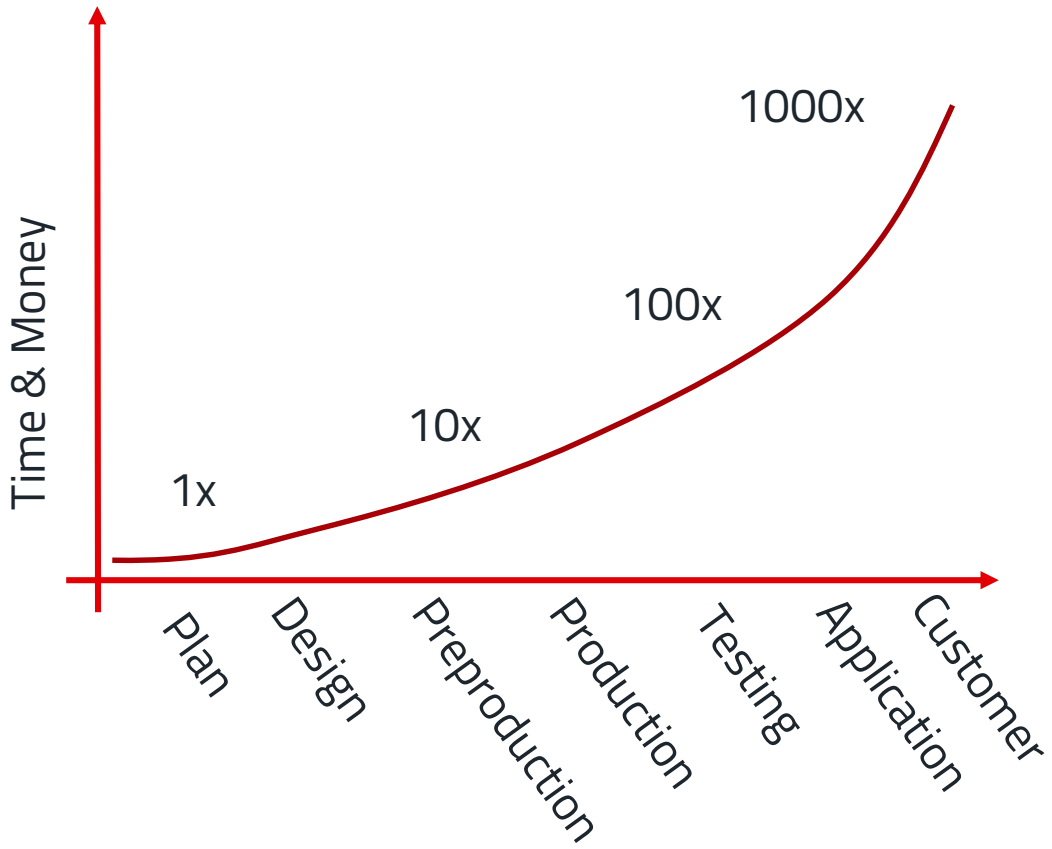
ZUSAMMENFASSUNG



Approach to a new High Speed Design :

- Experience?
- Competence?
- Trial & Error?
- Simulate before Fabricate?

ZUSAMMENFASSUNG



Approach to a new High Speed Design:

- **Plan**
  Impedance controlled Stack Up
- **Design**

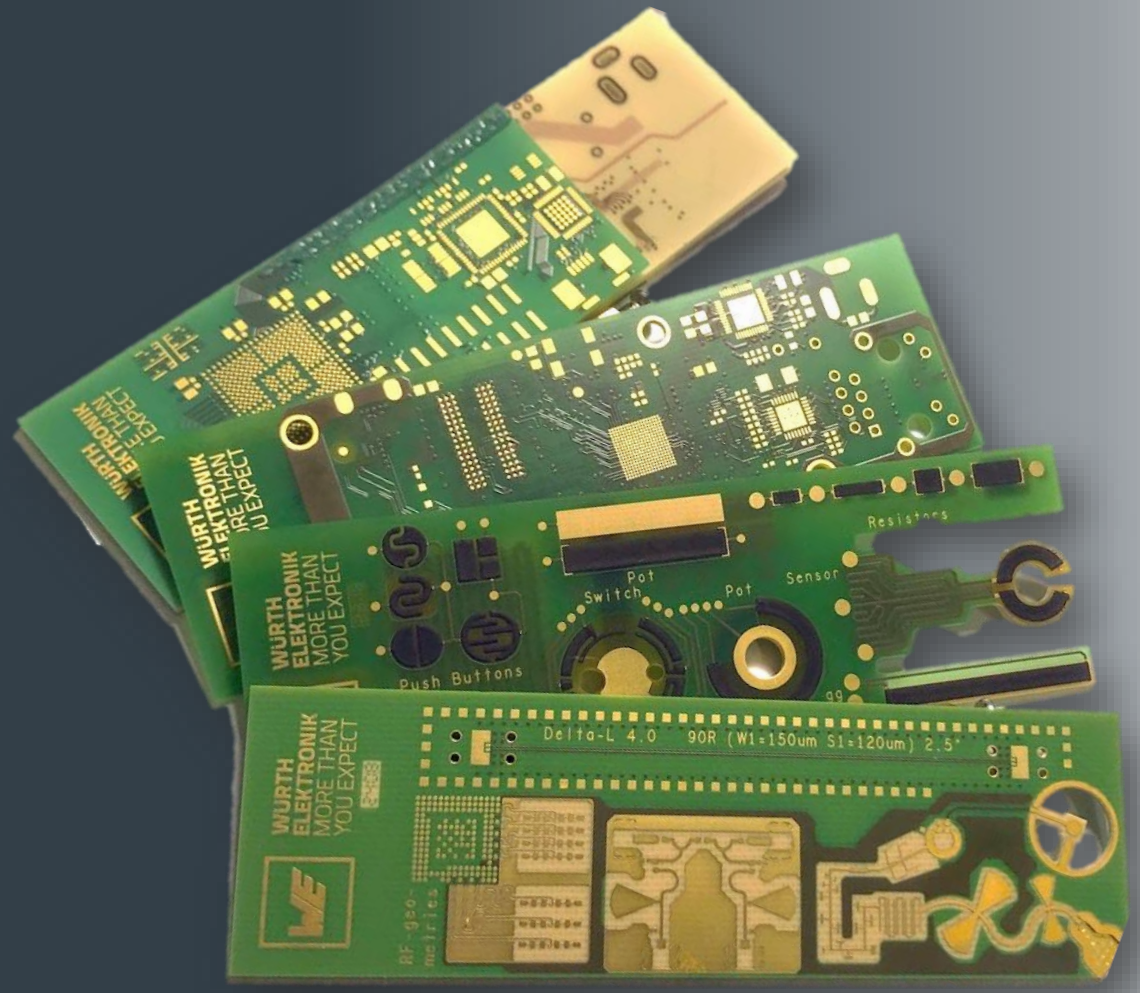
  Design Parameters & Guide Lines
  Design as Service by **WE**design Team
- **Preproduction**

  Feasibility & DRC Check
  EQ-Process with Documentation
- **Production**

  Quality Control

  „Design In“ if necessary
- **Testing**
  Impedance Control on every production panel

ZUSAMMENFASSUNG



- Würth Elektronik has High Speed Material qualified
  - Panasonic Megtron 6
  - Many others are available with WE-Asia
- **WE** can measure Material- and Layout parameters
  - Polar CITS880s Impedance Meter
  - Polar Atlas Delta L4.0 VNA Meter
- **WE** offers custom impedance controlled Stackups
  - More than 20 years of experience
- High Speed Designs can be complex -
  an early discussion about the Topic will lead to an optimal Solution


WÜRTH ELEKTRONIK
CIRCUIT BOARD TECHNOLOGY
We are your reliable partner – today and in the future