MASTERING CONDUCTED EMISSIONS TESTING: PROVEN TIPS AND TRICKS TO DEBUG YOUR BOARD

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Clark Kinnaird – Texas Instruments Automotive Systems

EMC STANDARDS

- What are EMC standards?
- Why EMC standards are so important and must be complied with?
- What types of EMC tests are being conducted?

WHY IS EMC IMPORTANT?

EMC TERMS AND DEFINITIONS

Radiated Emissions and Immunity

Emissions

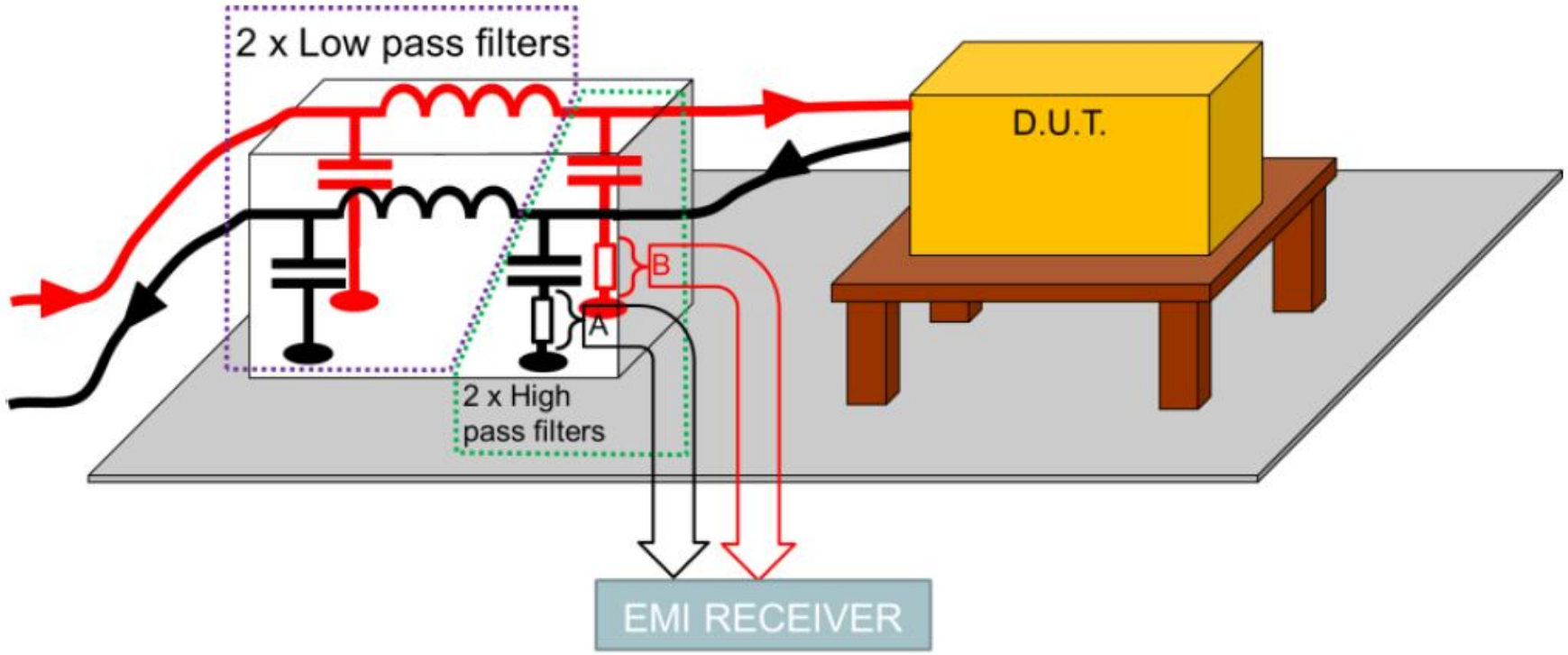
Immunity

EMC TERMS AND DEFINITIONS

Conducted Emissions and Immunity

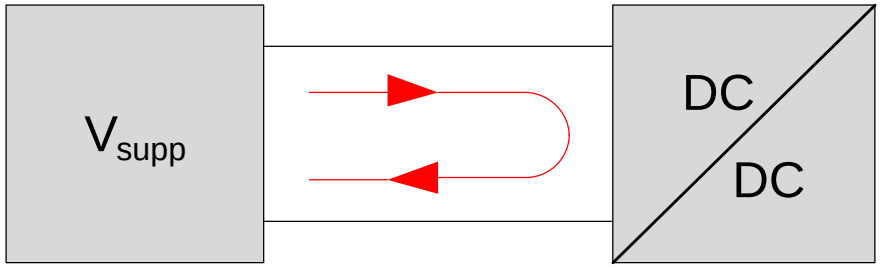
CONDUCTED EMISSION

Basic Set-up

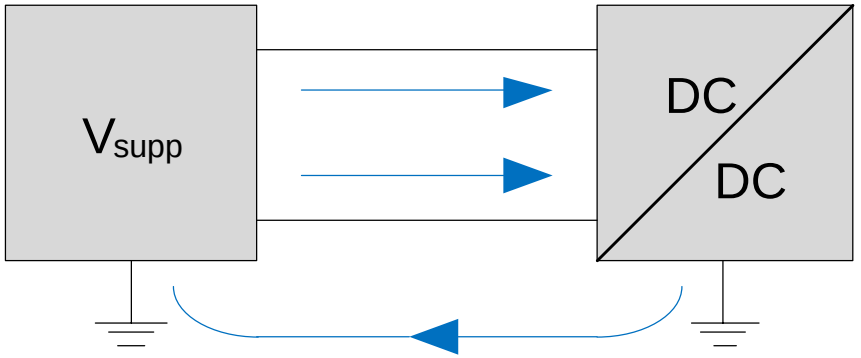


NOISE CATEGORIES

DM and CM noise path



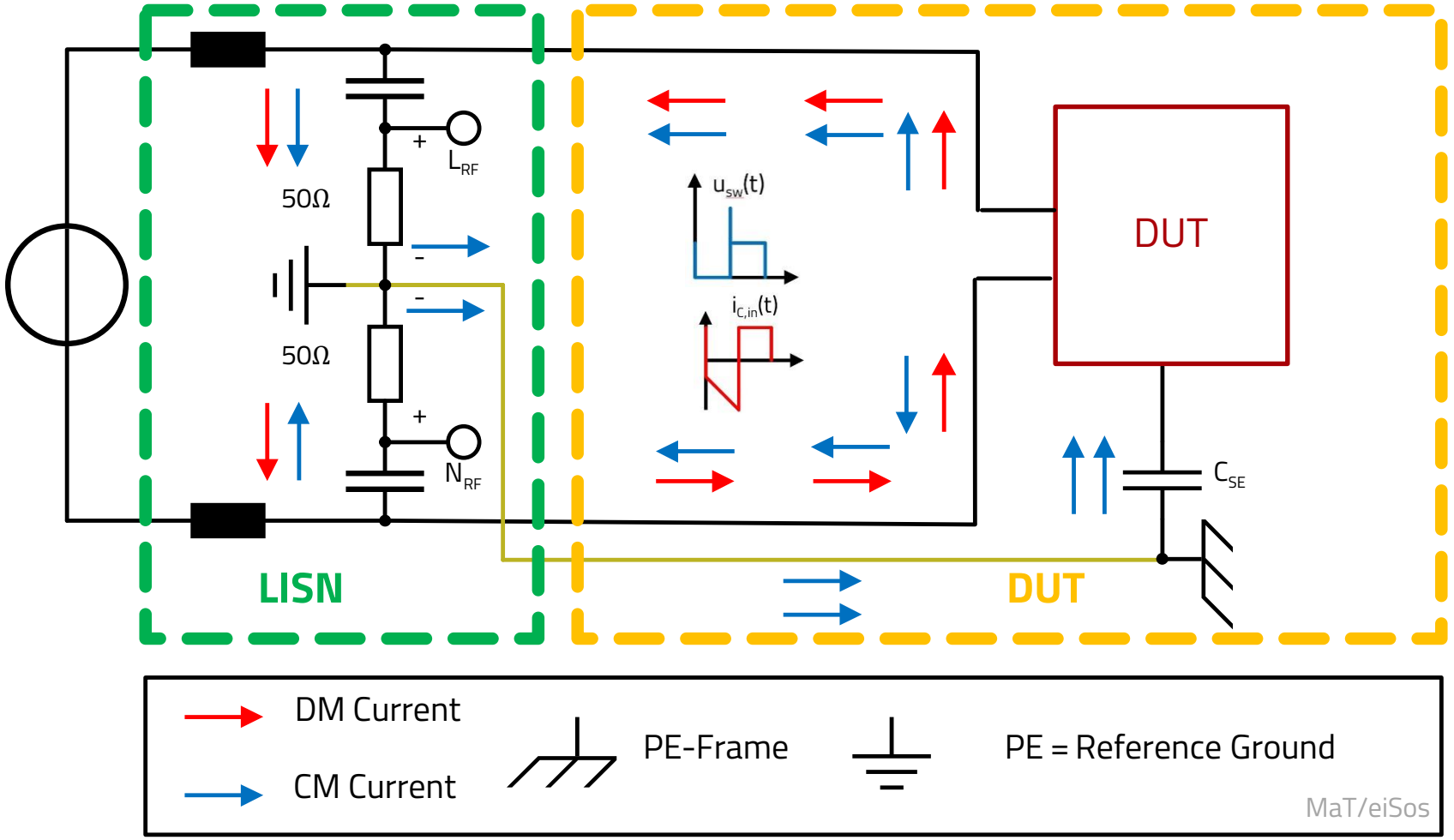
DIFFERENTIAL MODE



COMMON MODE

NOISE CATEGORIES

DM and CM noise path



$$U_{\mathrm{L,RF}} = U_{\mathrm{CM}} + U_{\mathrm{DM}}$$

$$U_{\mathrm{N,RF}} = U_{\mathrm{CM}} - U_{\mathrm{DM}}$$

$$U_{\mathrm{DM}} = \frac{U_{\mathrm{L,RF}} - U_{\mathrm{N,RF}}}{2}$$

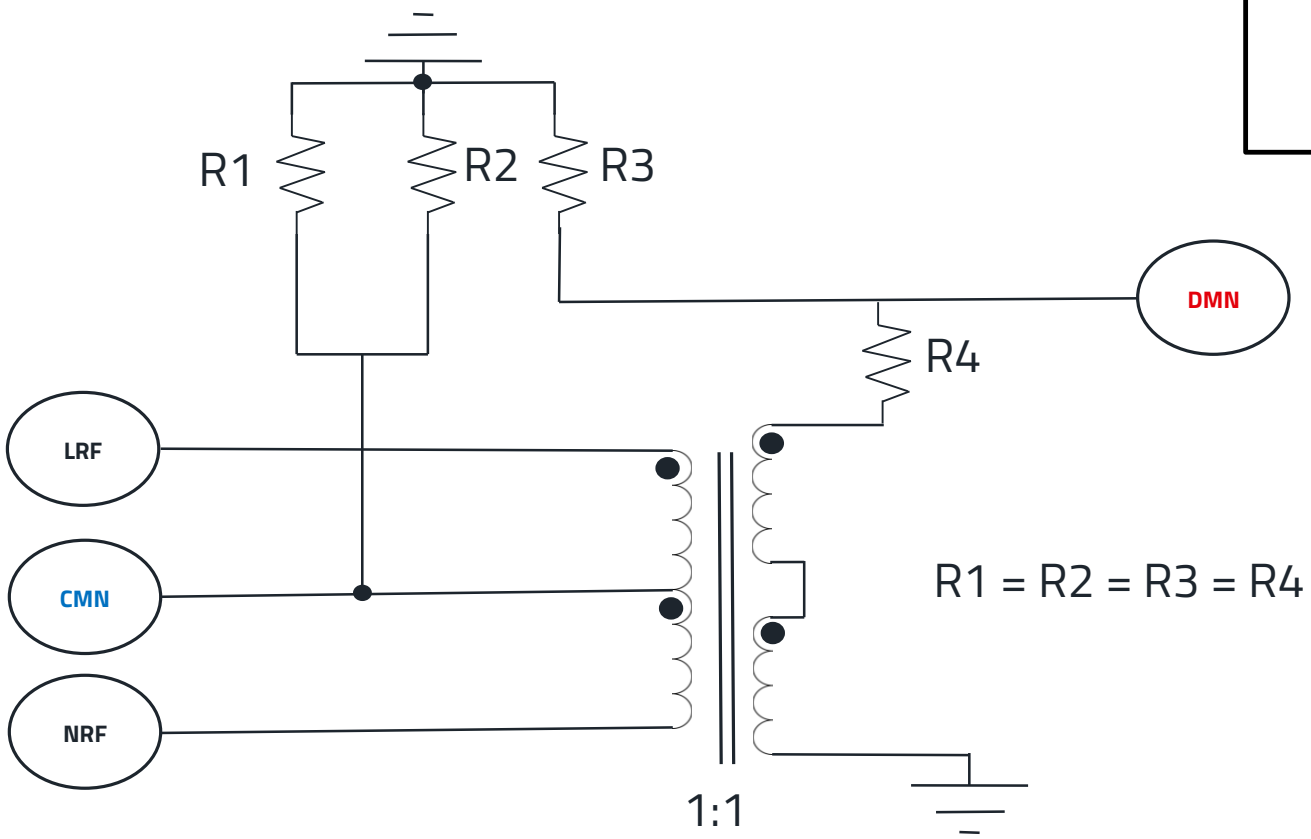
$$U_{\mathrm{CM}} = \frac{U_{\mathrm{L,RF}} + U_{\mathrm{N,RF}}}{2}$$

MEASURING THE NOISE

DMB and CMN Splitter

$$U_{\mathrm{DM}} = \frac{U_{\mathrm{L,RF}} - U_{\mathrm{N,RF}}}{2}$$

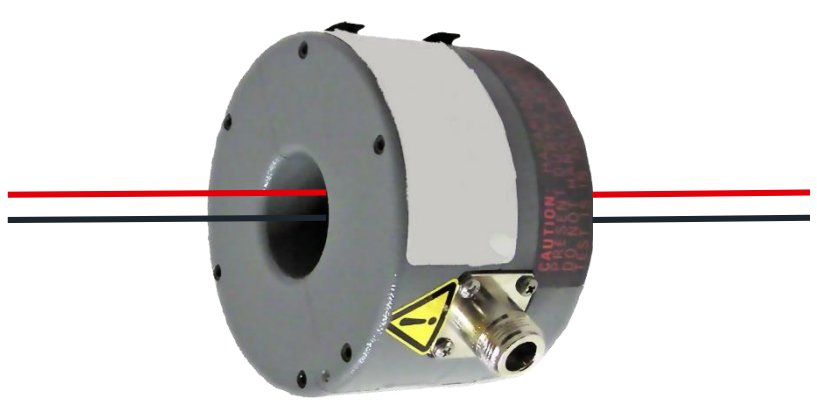
$$U_{\mathrm{CM}} = \frac{U_{\mathrm{L,RF}} + U_{\mathrm{N,RF}}}{2}$$

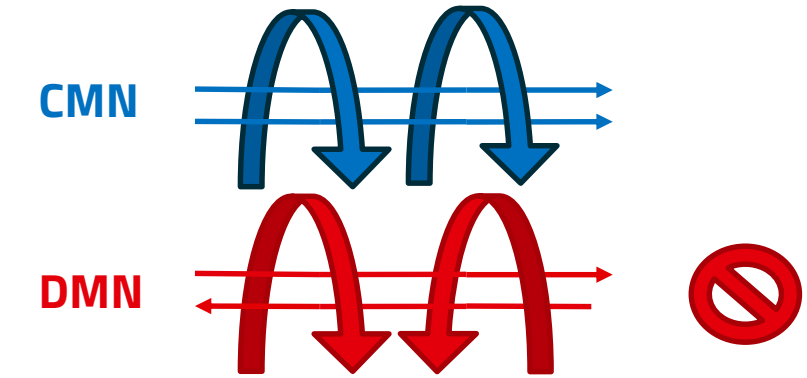


MEASURING THE NOISE

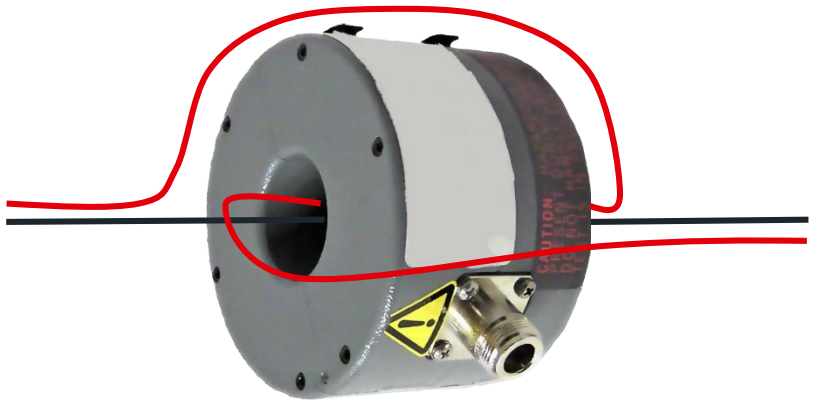
Current Clamp

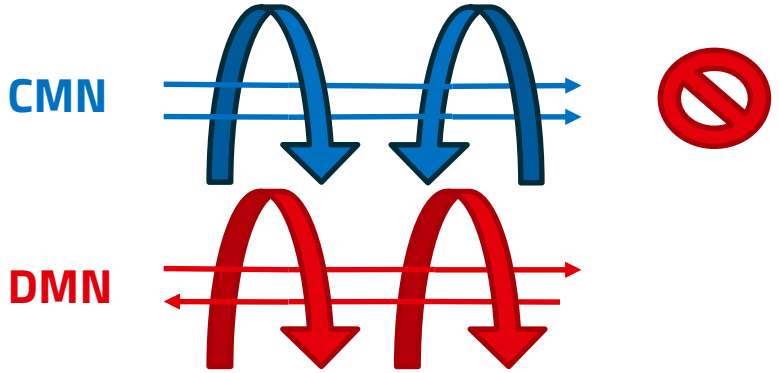
Common Mode Noise



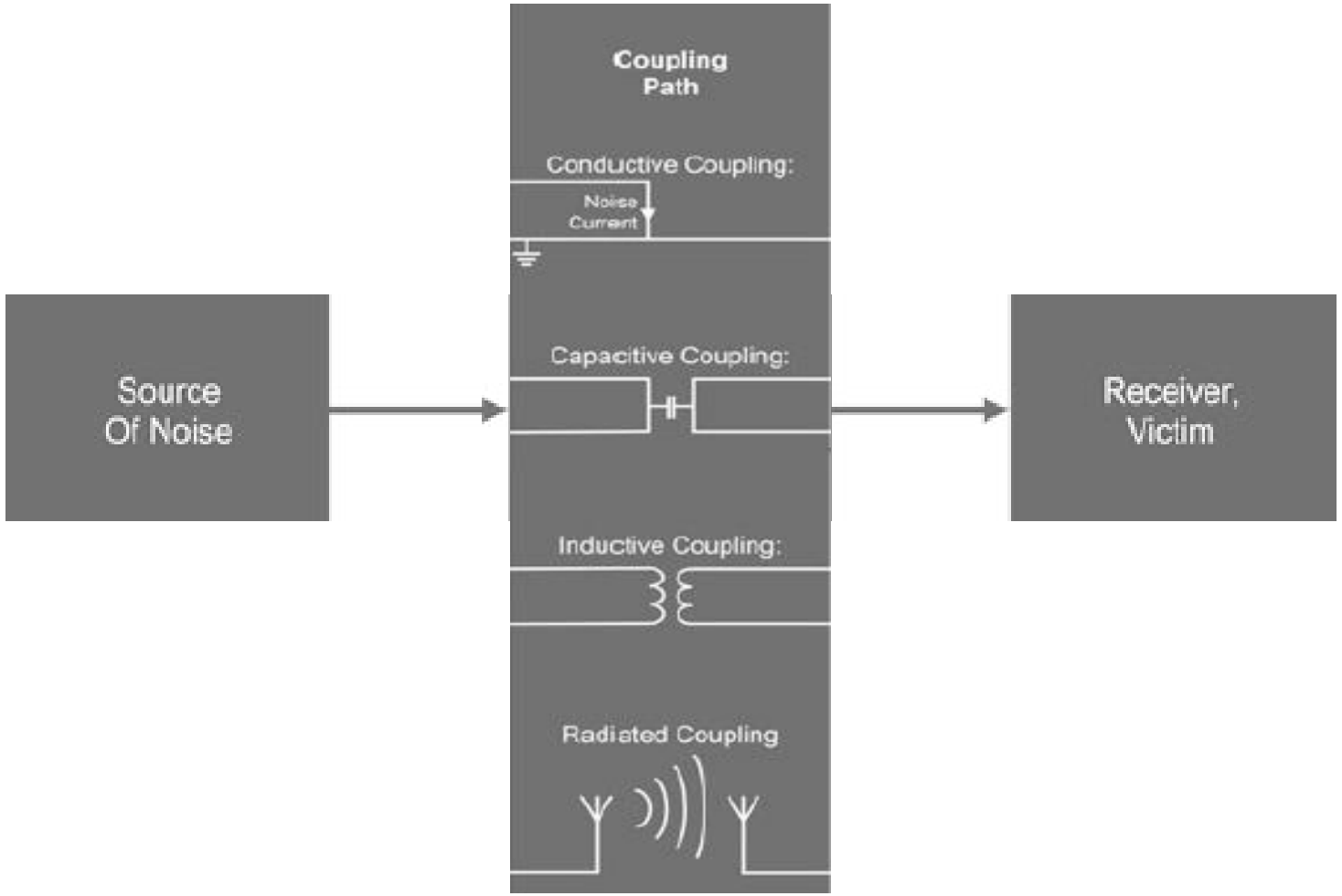


Differential Mode Noise

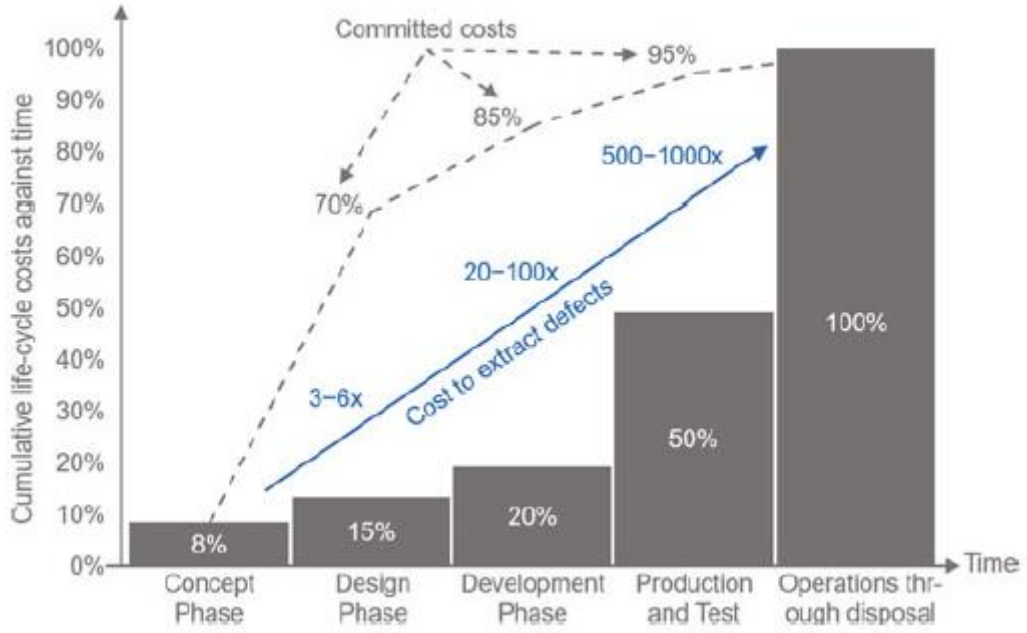




COUPLING PATHS



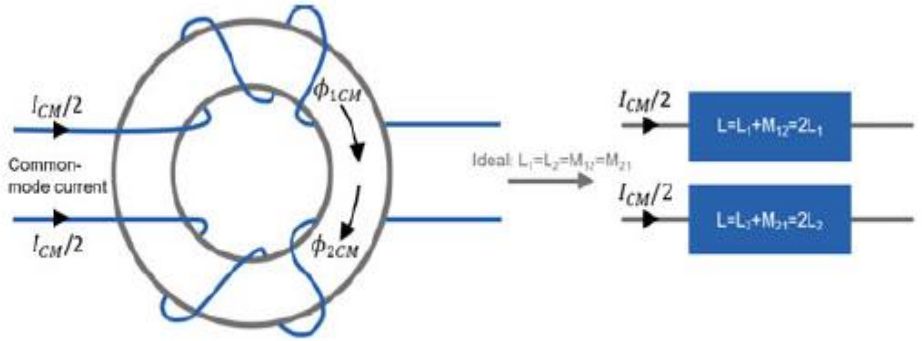
DESIGN FOR EMC



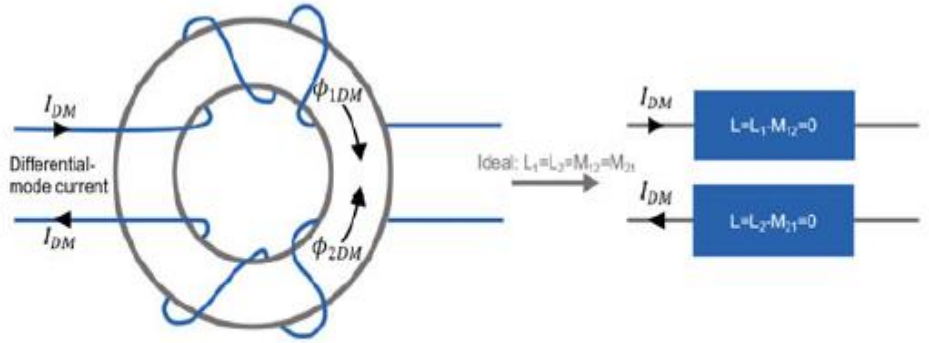
(DAU). 1993. Committed life cycle costs against time. Fort Belvoir, VA. Defense Acquisition University

CMC

CM & DM Insertion Loss



(a)



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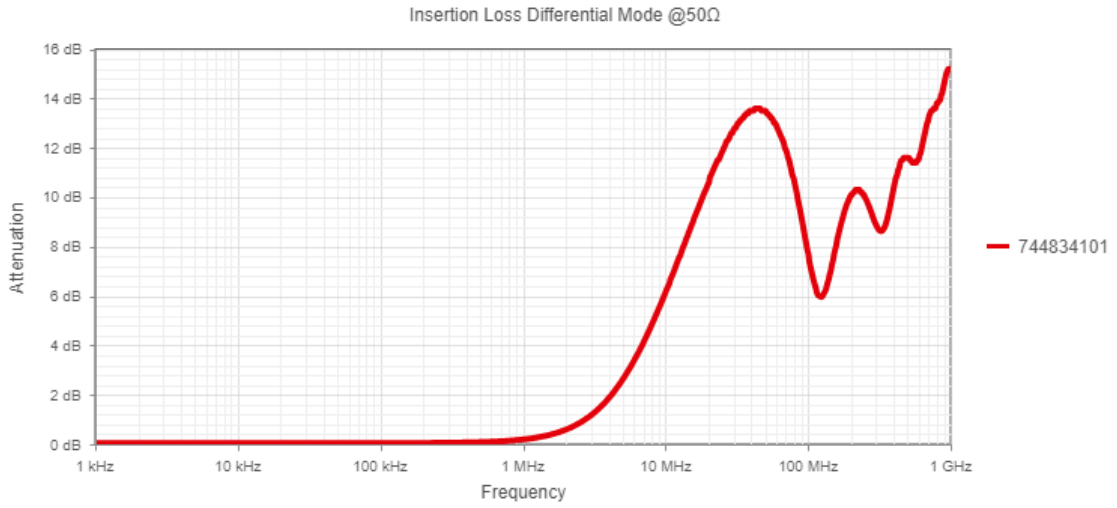
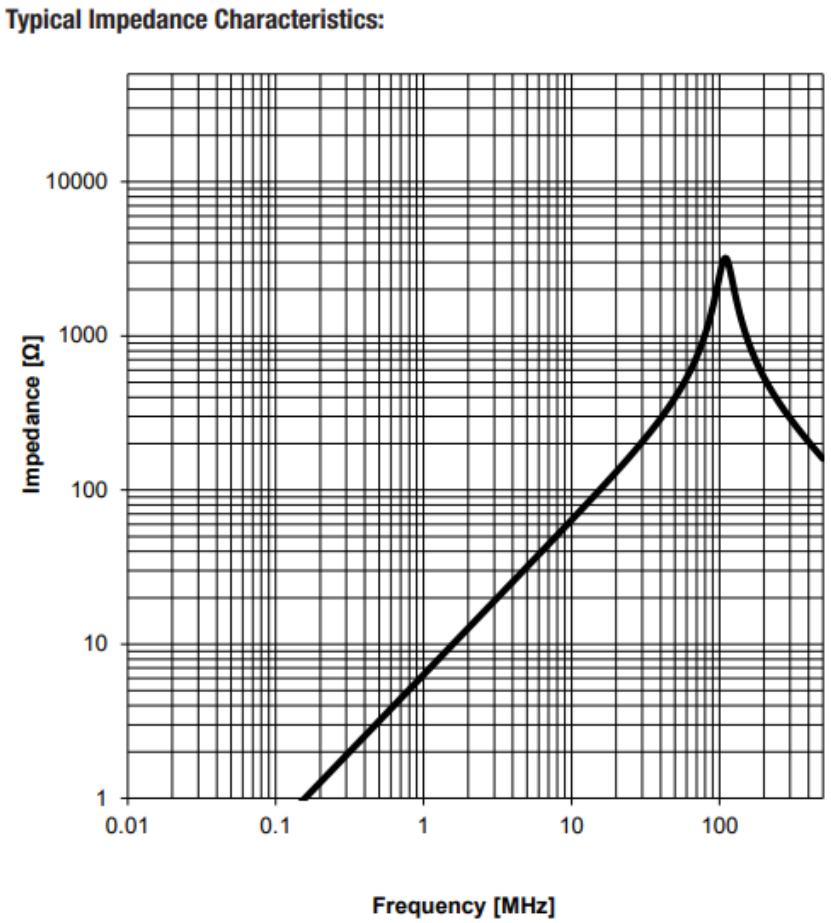


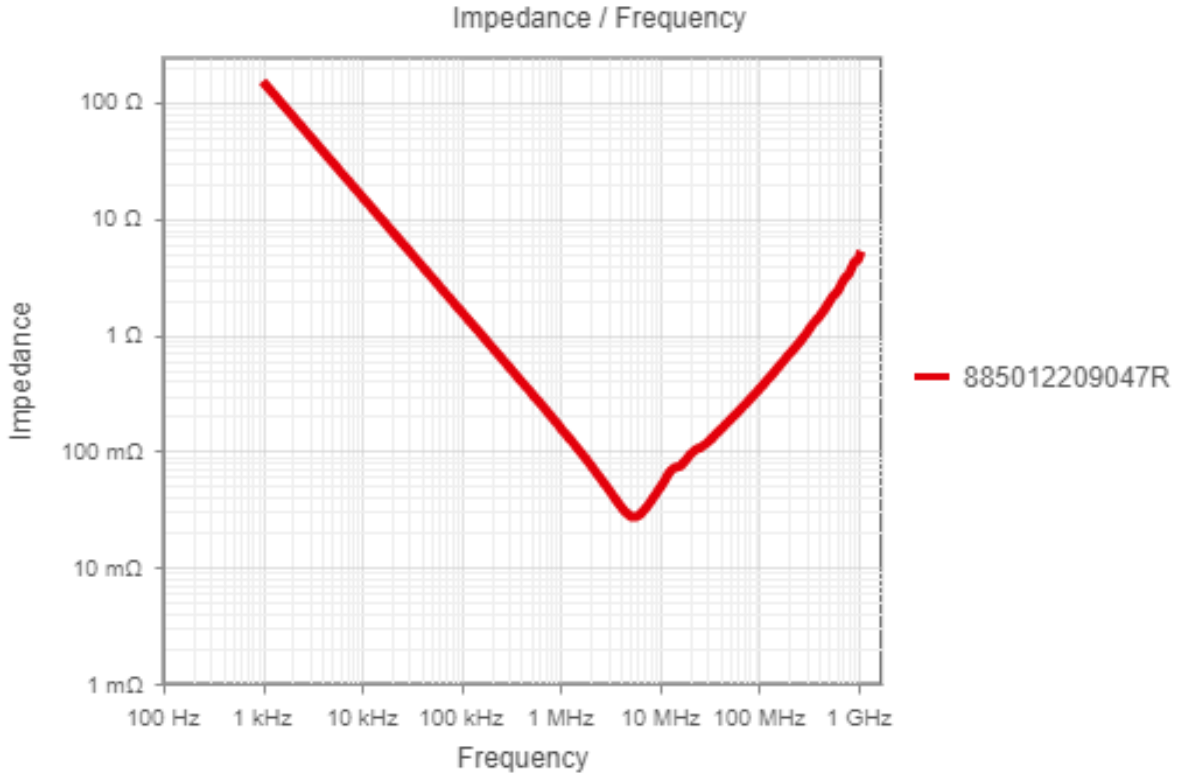
INDUCTOR

Impedance Response

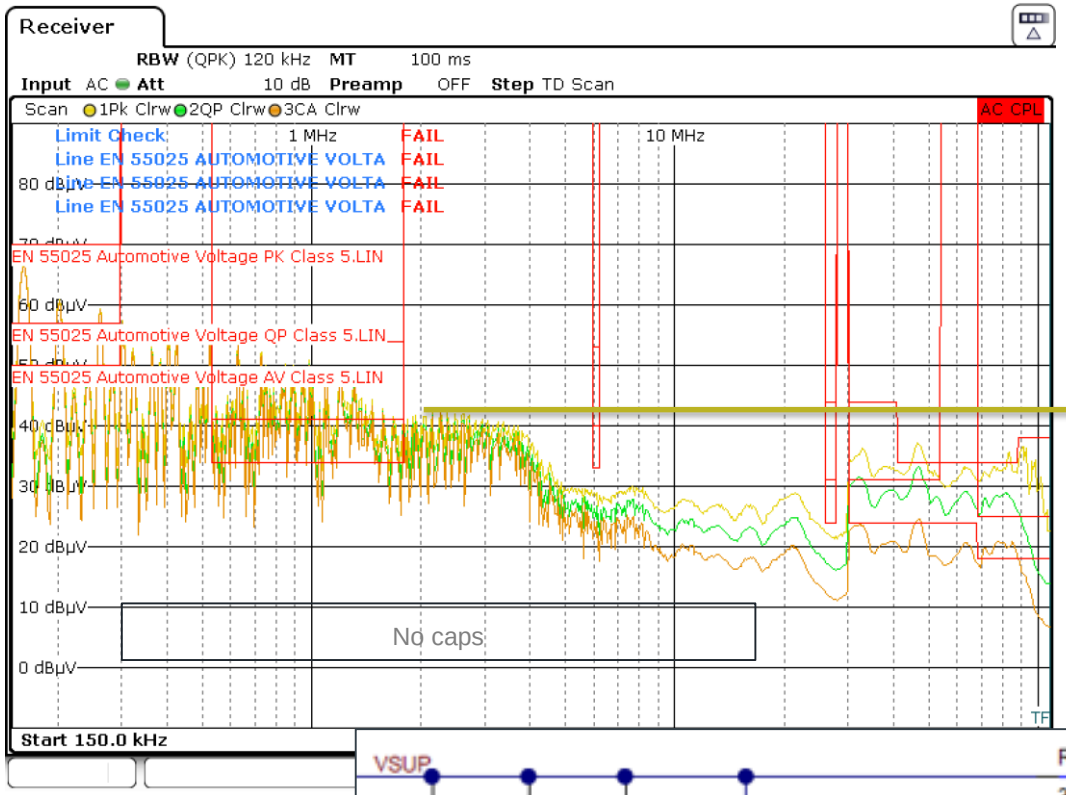


CAPACITOR

Impedance Response



EMC RESULTS – CERAMIC BYPASS CAPS



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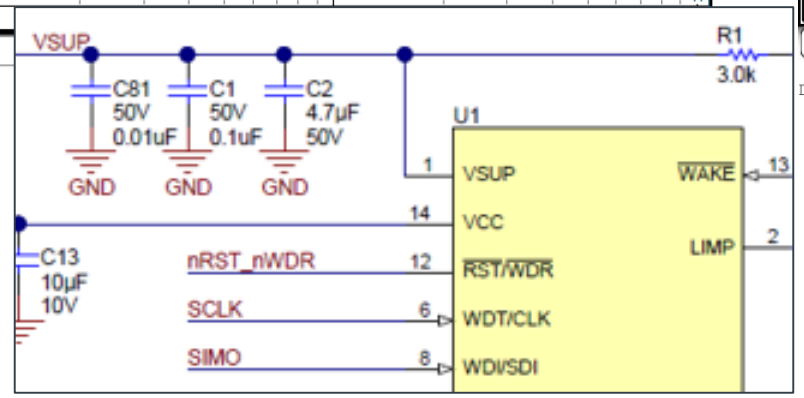

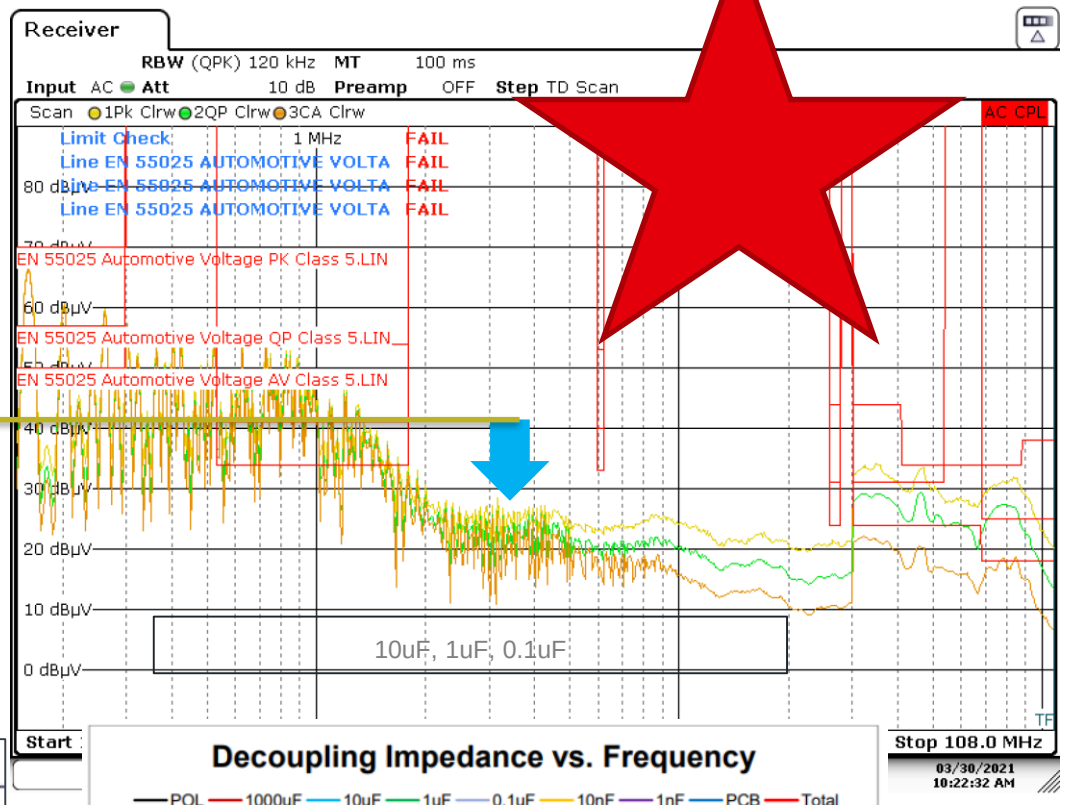

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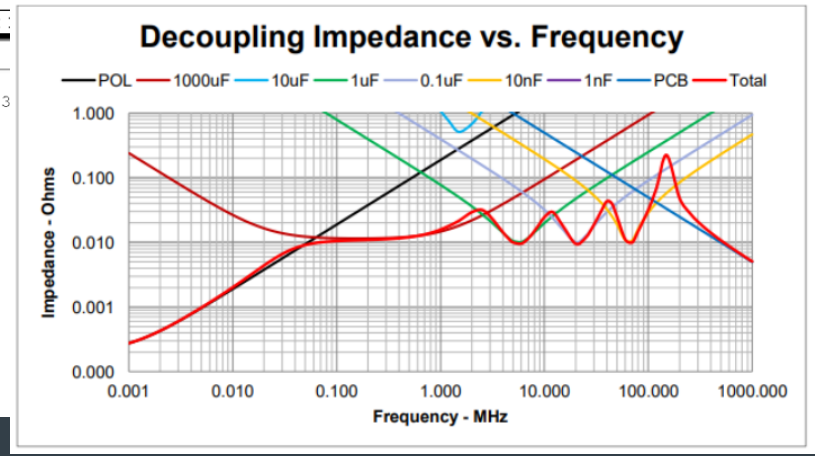
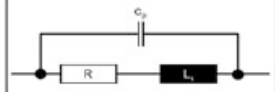
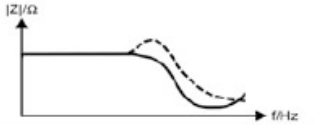
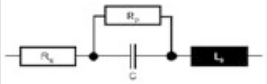
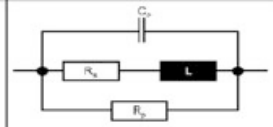
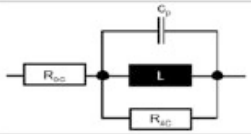
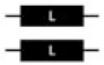
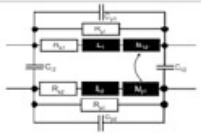
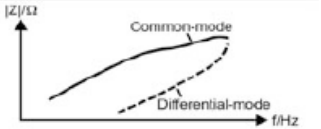


SUMMARY OF THE HIGH-FREQUENCY RESPONSE

Devices	Low-Frequency (e.g. <10kHz)	High-Frequency (e.g. >10MHz)	Frequency response
Single Conductor, Single Wire			
Resistor			
Capacitor			
Inductor			
Chip Ferrite Beads			
Cable Mount Ferrite Beads			
Common-Mode Chokes			

FILTERS

Filter Summary

Common Mode Filters

Common Mode Chokes

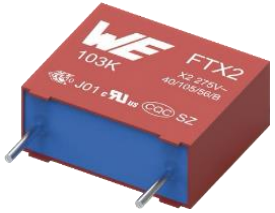
Y-Capacitors

Cable Ferrites

Differential Filters

Inductors

PCB Ferrites



X-Capacitors

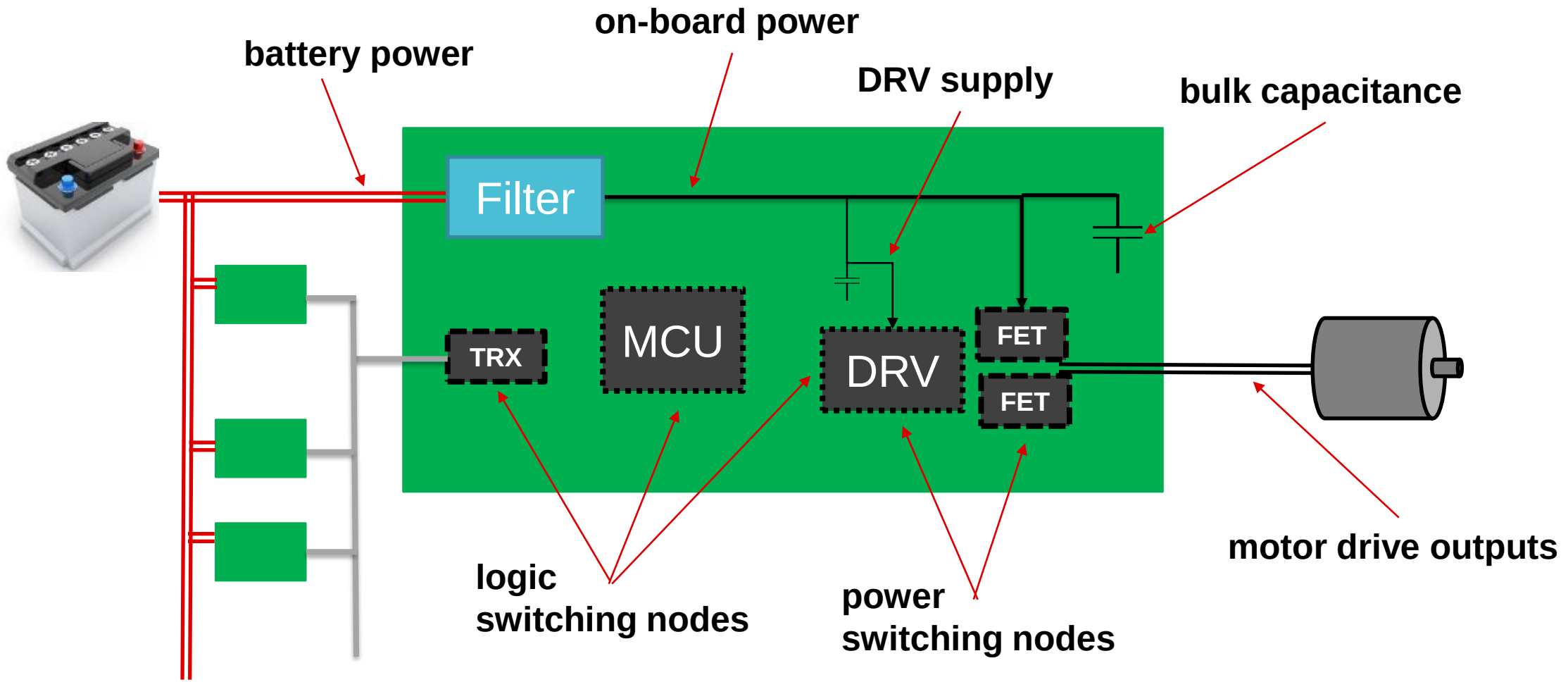
Guidelines for improving conducted emissions

Würth Electronics Conducted Emissions webinar Oct. 24, 2023

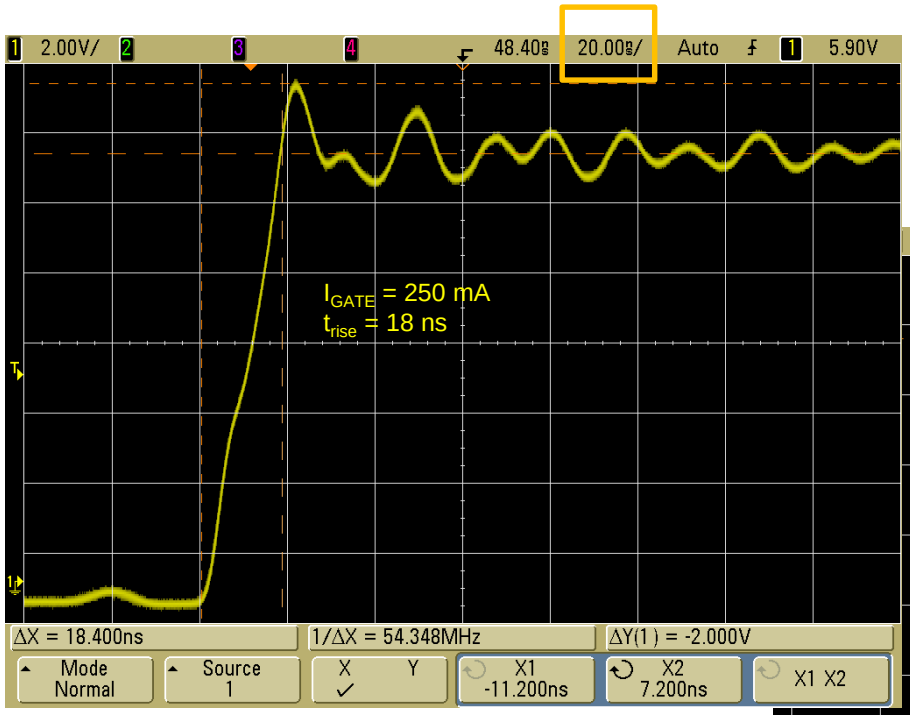
Clark Kinnaird

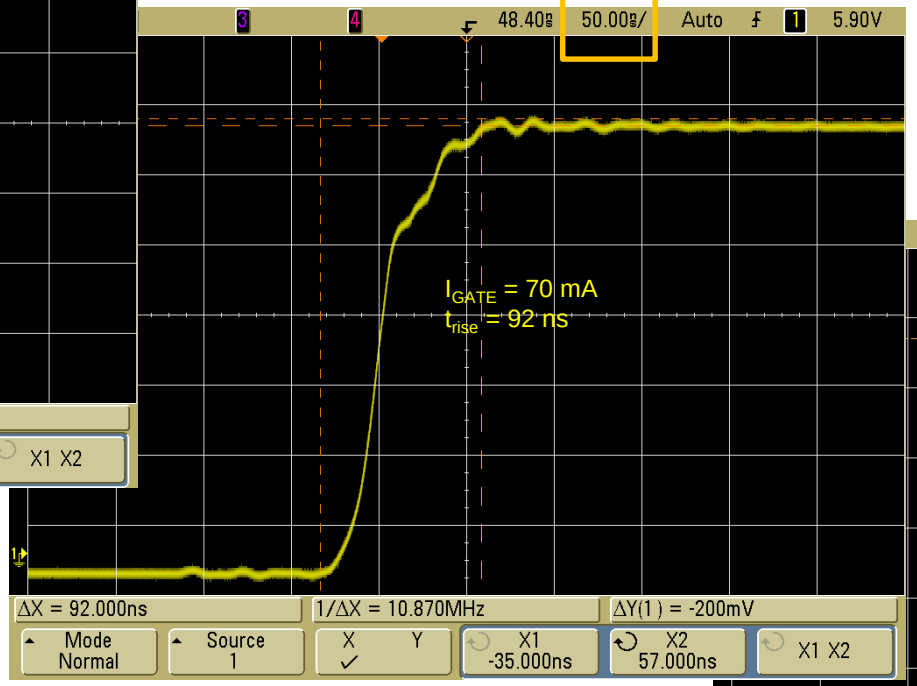
Texas Instruments

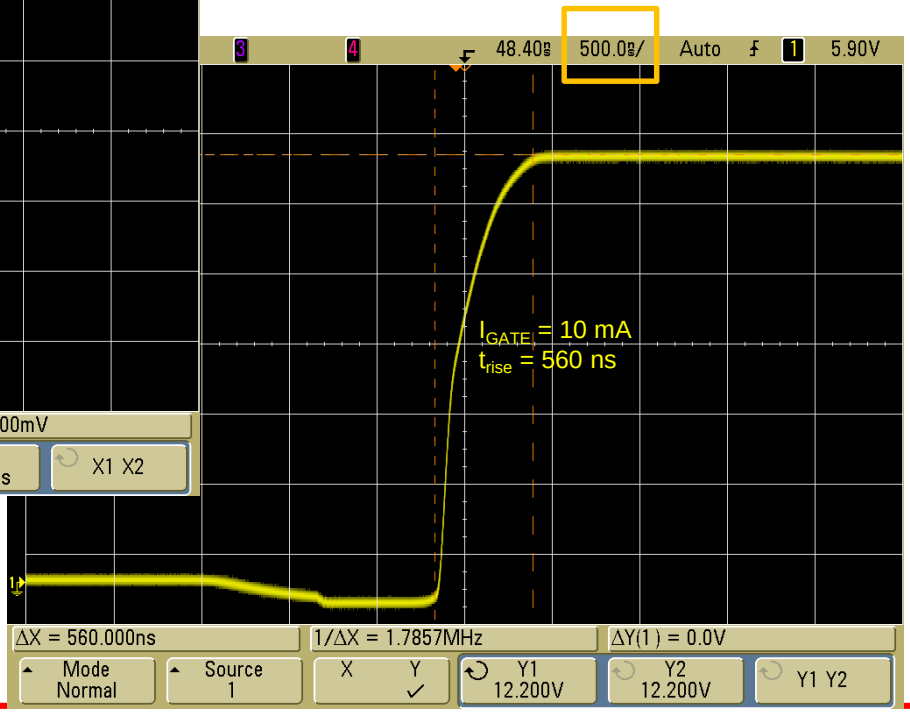
Emissions opportunity points

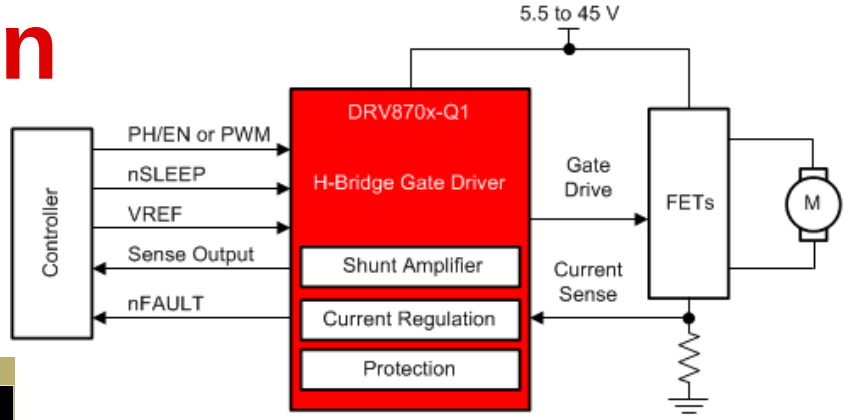


Effect of gate current in time domain



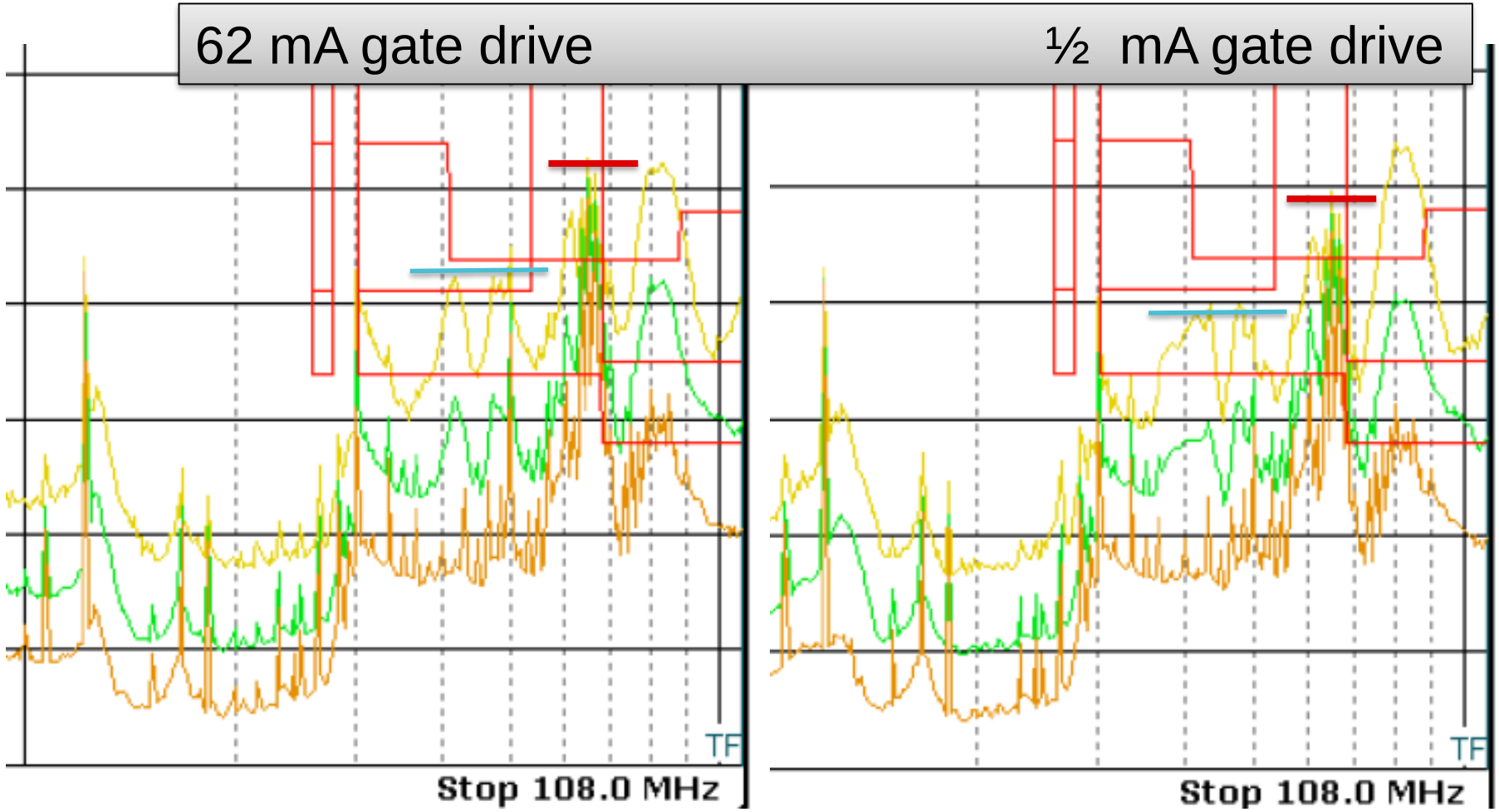






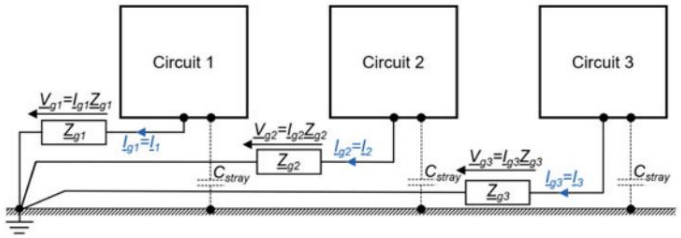
Effect of gate current in frequency domain

- Change the rise time of PWM edges at 20 kHz
- Reduced emissions at > 10 MHz frequencies

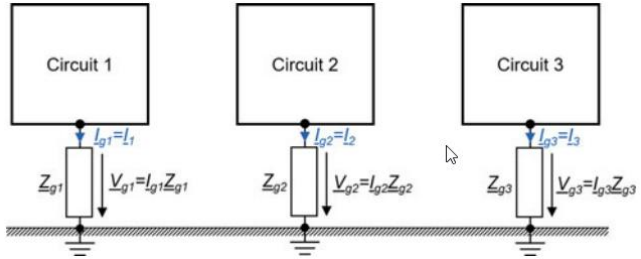


Grounding techniques

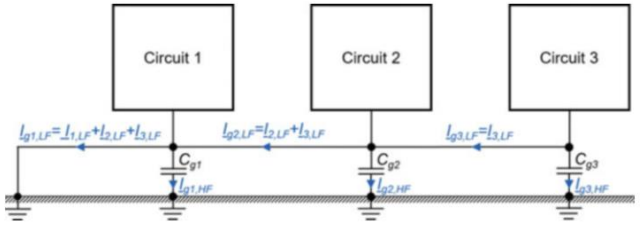
- Single Point (Star ground): Effective for low frequencies ($f < 100\ kHz$)

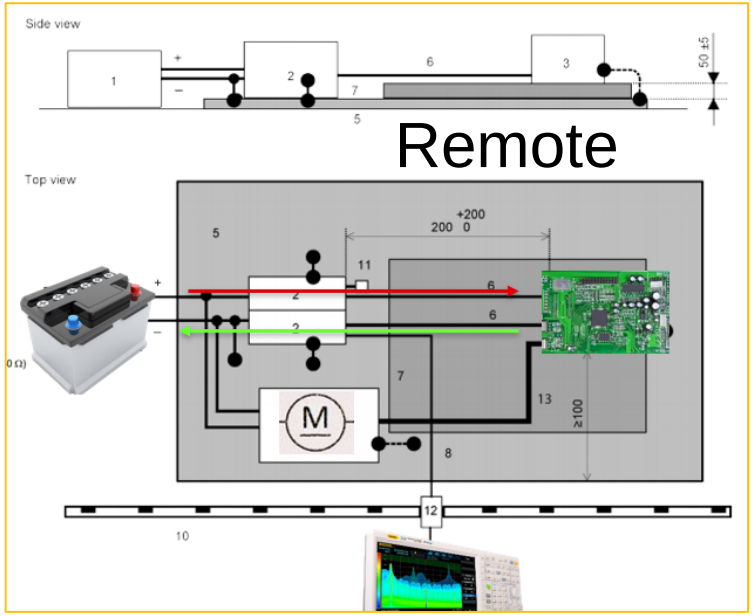


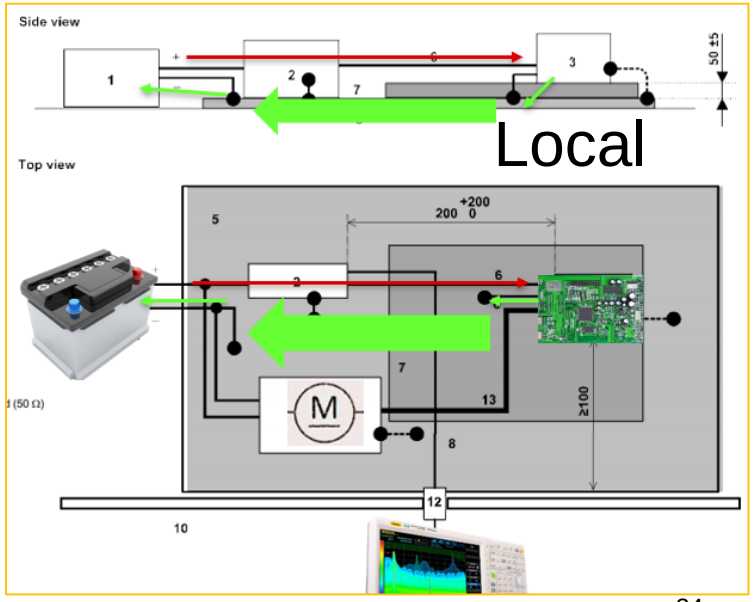
- Multipoint ground: Effective for high frequencies ($f > 1\ MHz$)



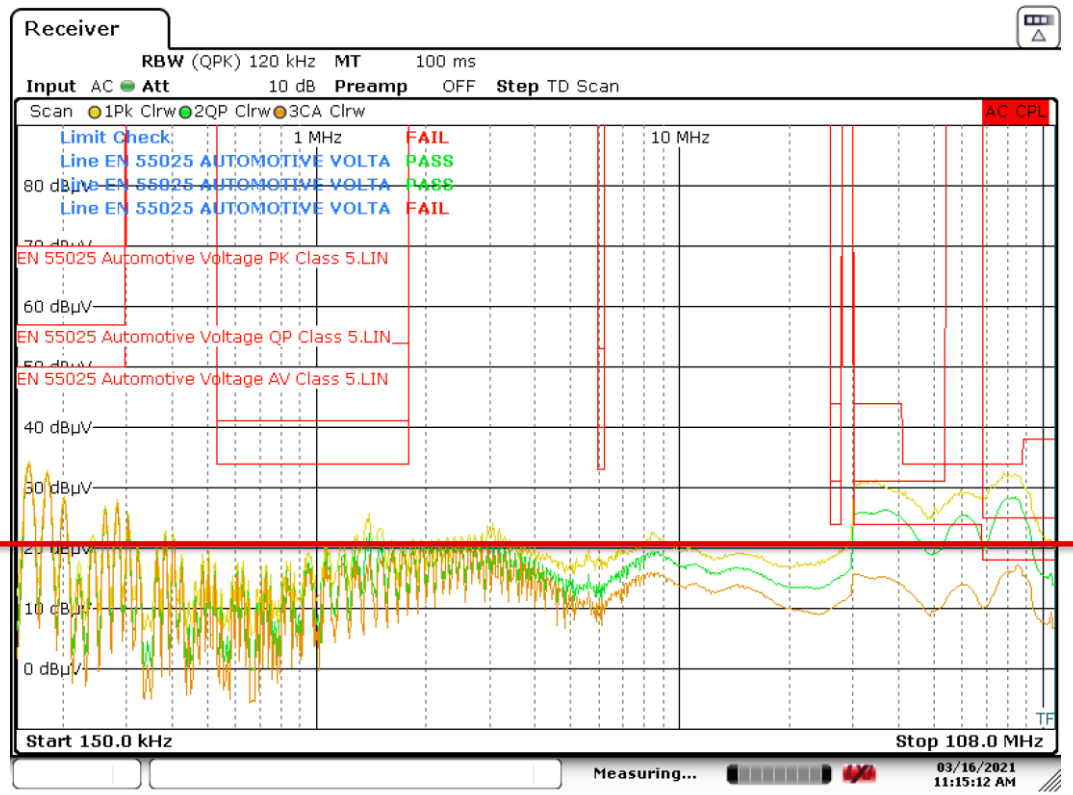
- Hybrid ground: Effective for both low and high frequencies







Local GND vs Remote GND results



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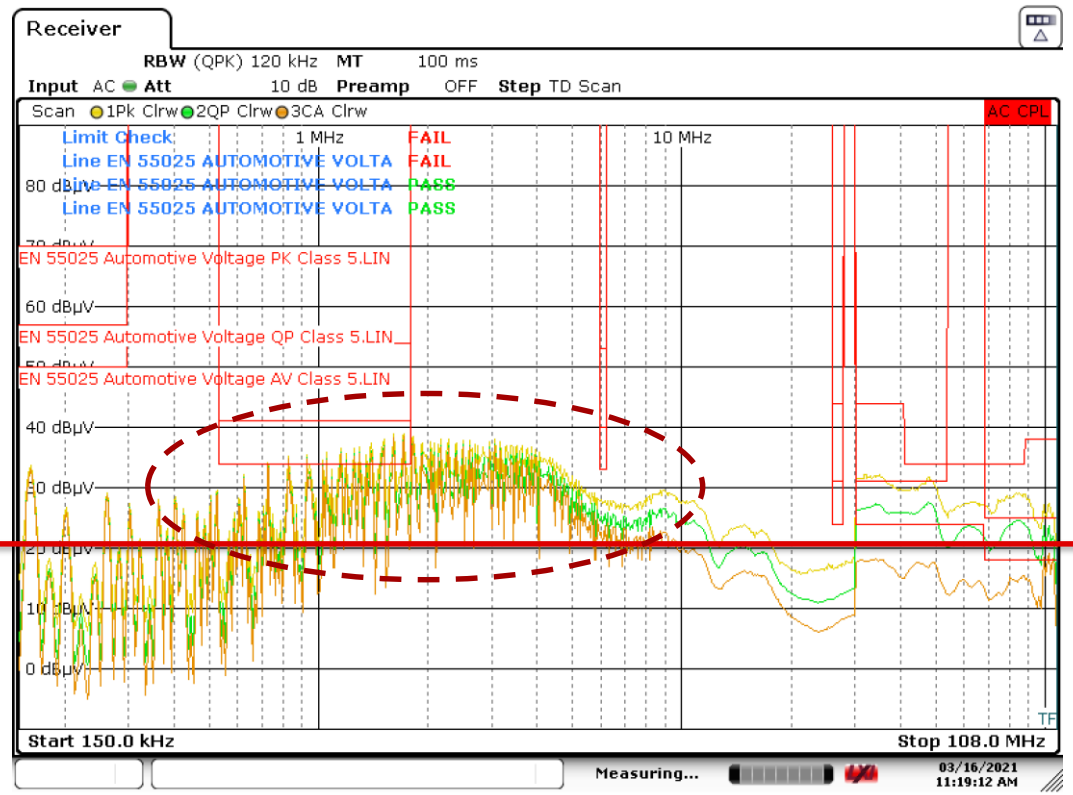
Local GND



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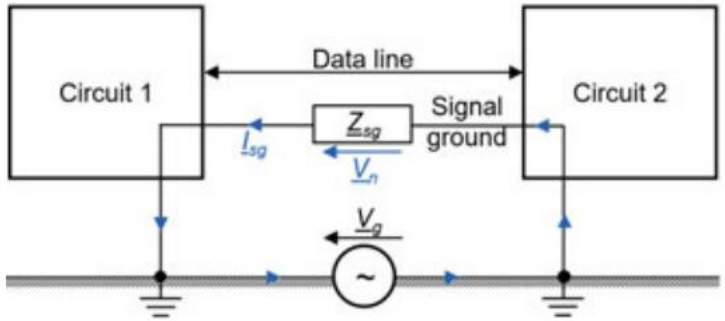
Remote GND

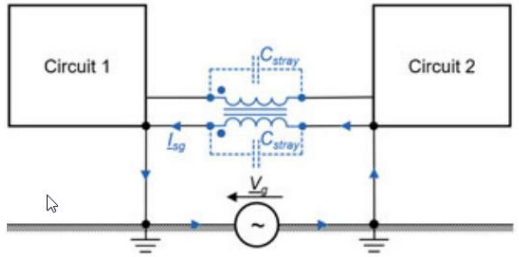
Minimizing ground loops

- Ground loops can be a problem in lower frequency ($f < 100\ kHz$)



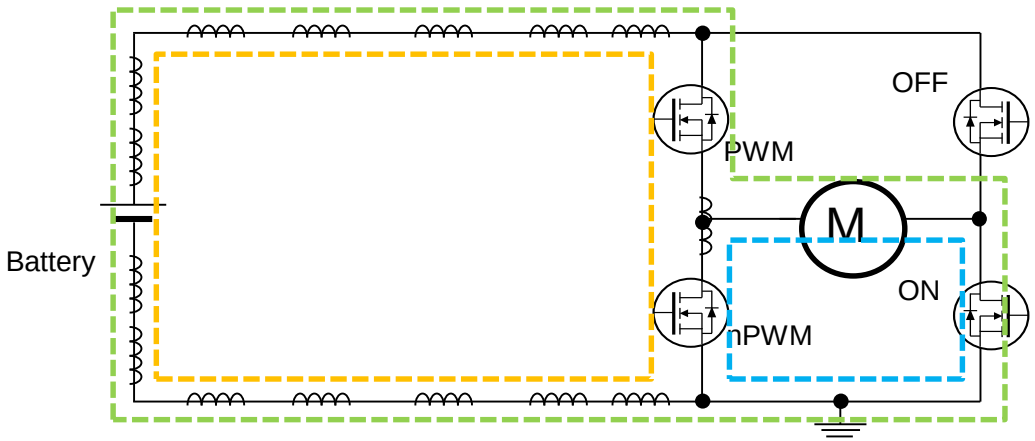
V_g is caused by voltage potential difference between two circuits or induced by external magnetic field.
V_n is noise voltage that can interfere with the useful signal

- Methods for minimizing impact of ground loops:
  - Use single-ended or hybrid ground systems
  - Minimize ground impedance and loop area
  - Add inductance in the GND path with a common-mode choke to attenuate HF



Attenuation of LF ($f < 10\ kHz$) and very HF ($f > 1\ GHz$) due to the relative low inductance and stray capacitance

Minimize di/dt and dv/dt loops

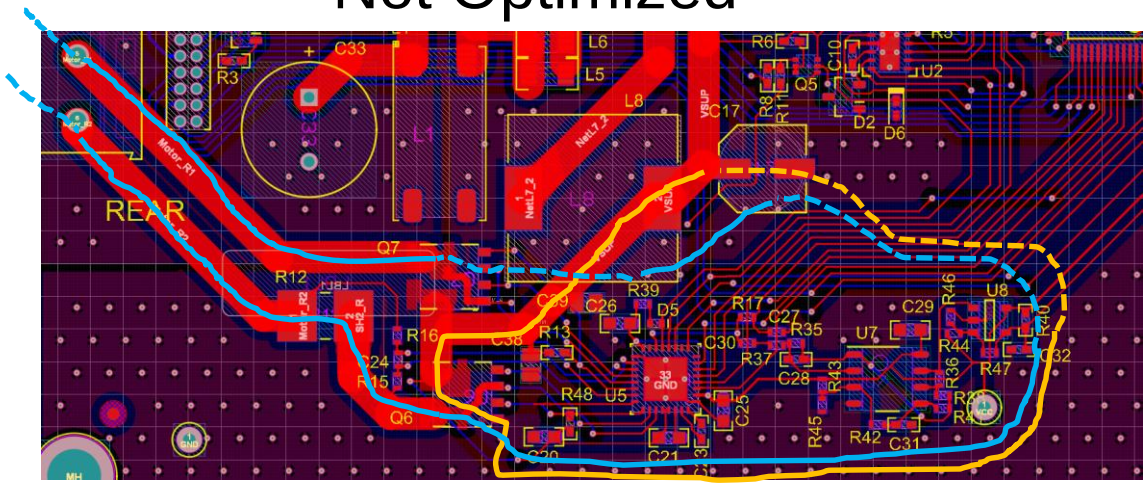


Green Loop: Current path at ON duty
Blue Loop: Current path at OFF duty
Orange Loop: The area where two loops don't overlap
= High di/dt loop

Inductance causes ringing, spikes, generation of EMI

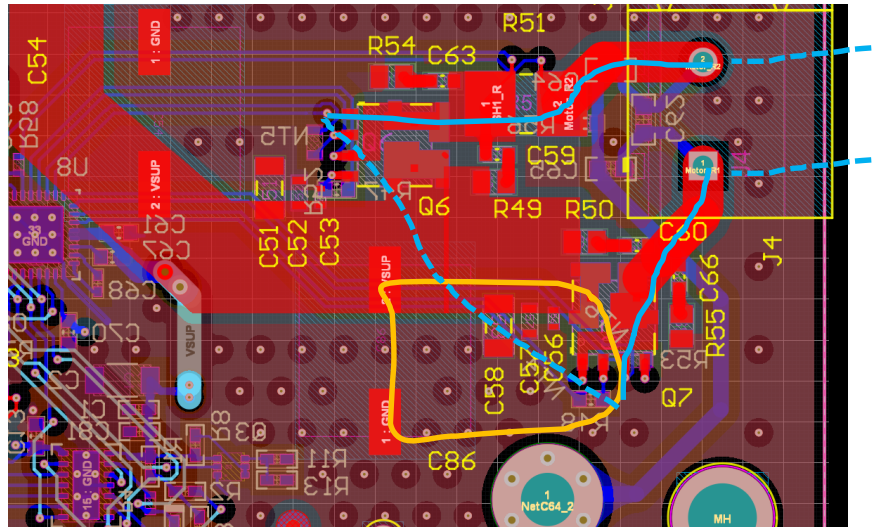
L ∝ Loop Area

Not Optimized



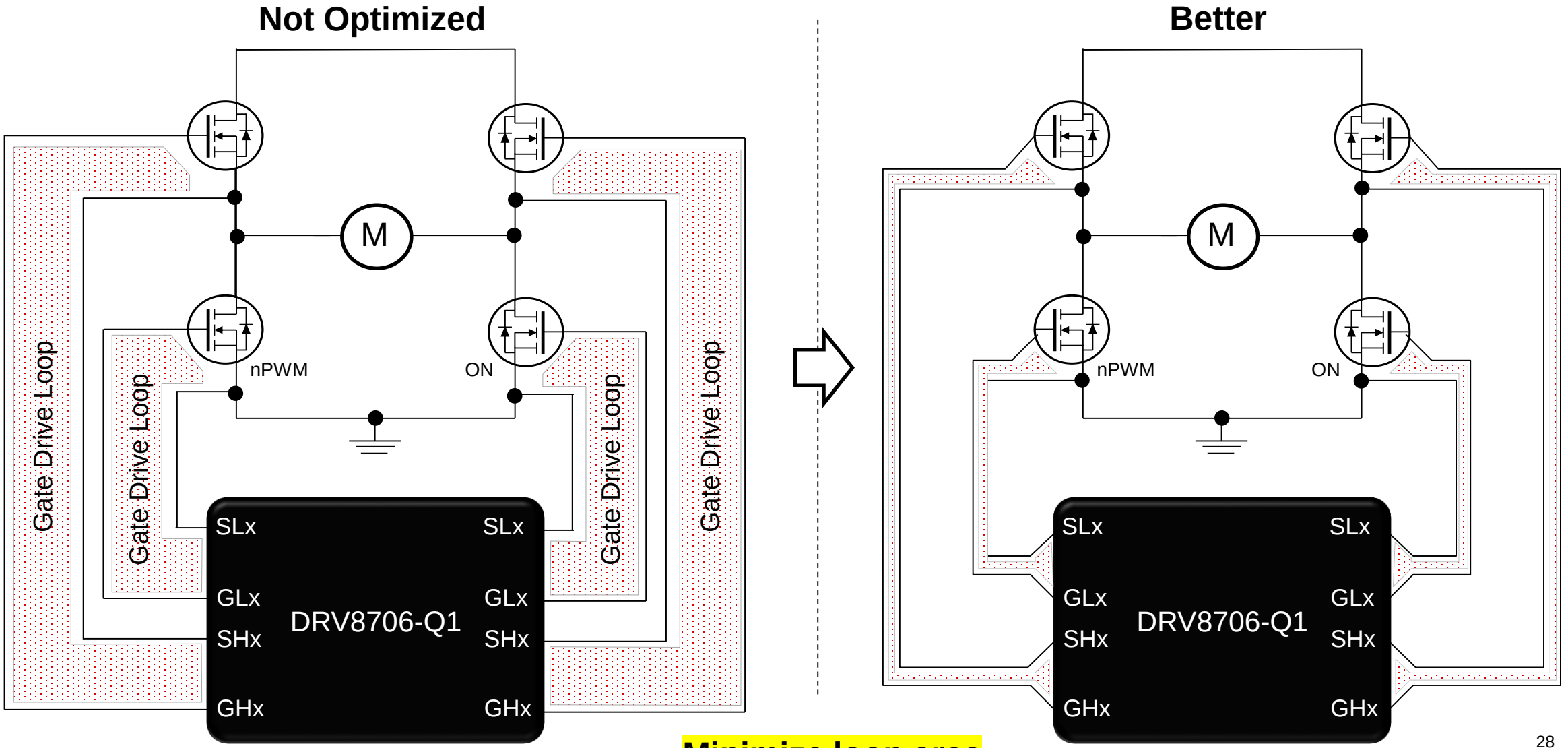
2 Layers; Stack: LY1: Signal; LY2: Signal

Better



4 Layers; Stack: LY1: Signal; LY2: GND; LY3: Power; LY4: Signal

Minimize Gate Drive Loop

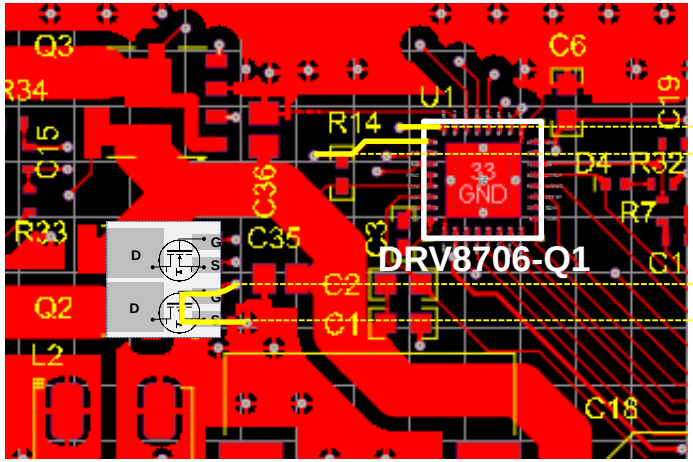


Minimize loop area to minimize parasitic inductance

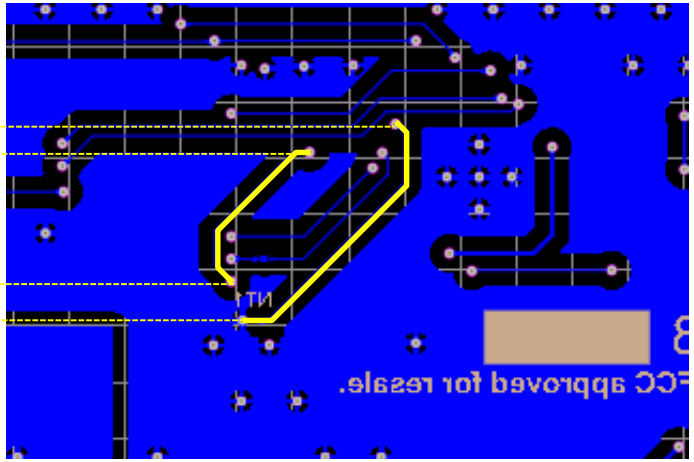
Minimize Gate Drive Loop

Not Optimized

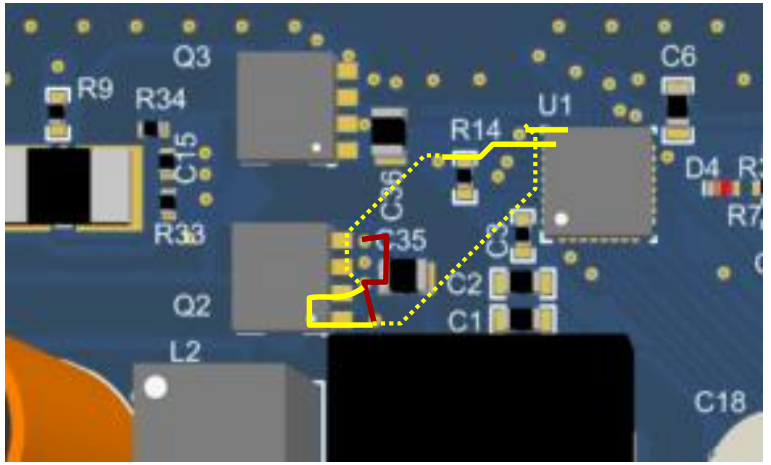
1st Layer



2nd Layer

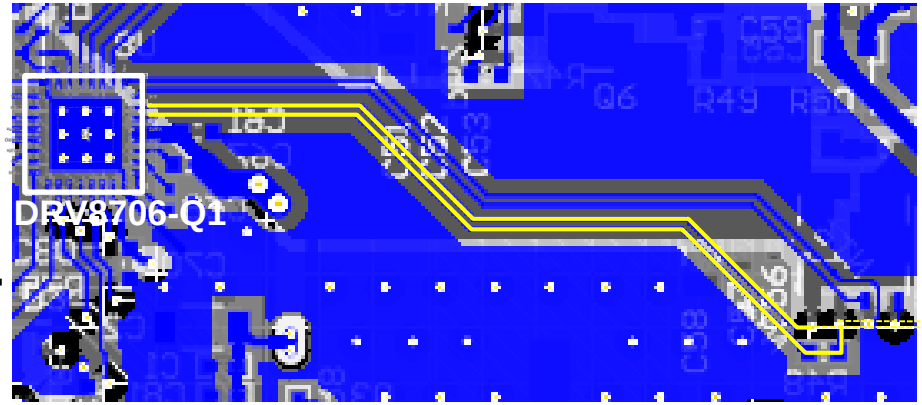


3D View

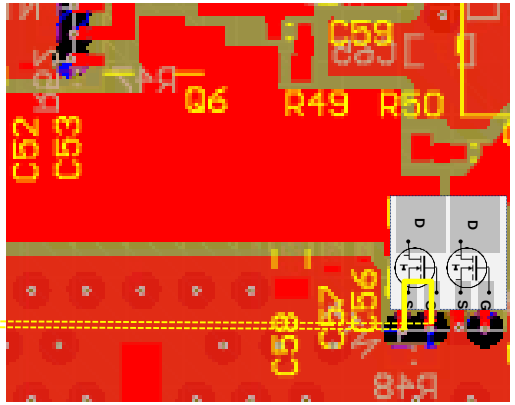


Optimized

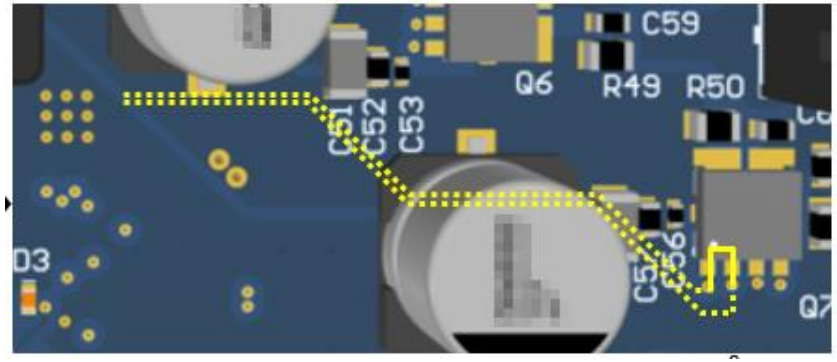
4th Layer



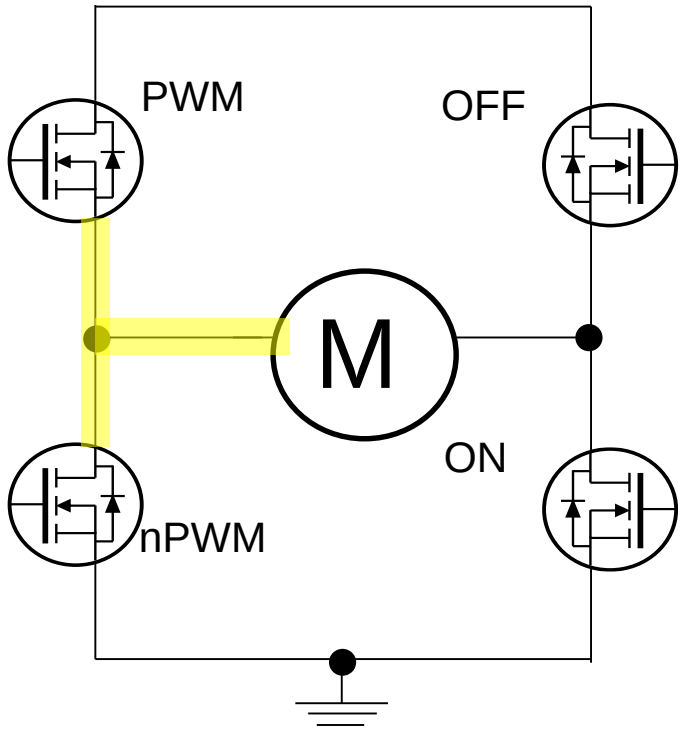
1st Layer

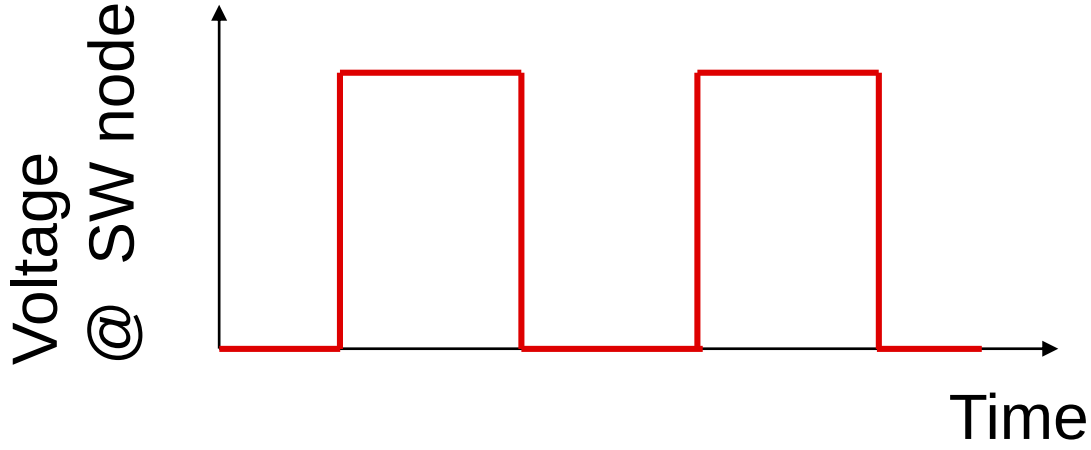


3D View



Minimize Switching Node Area





Switch node: dV from 0V to VBAT

→ Causing capacitive noise coupling

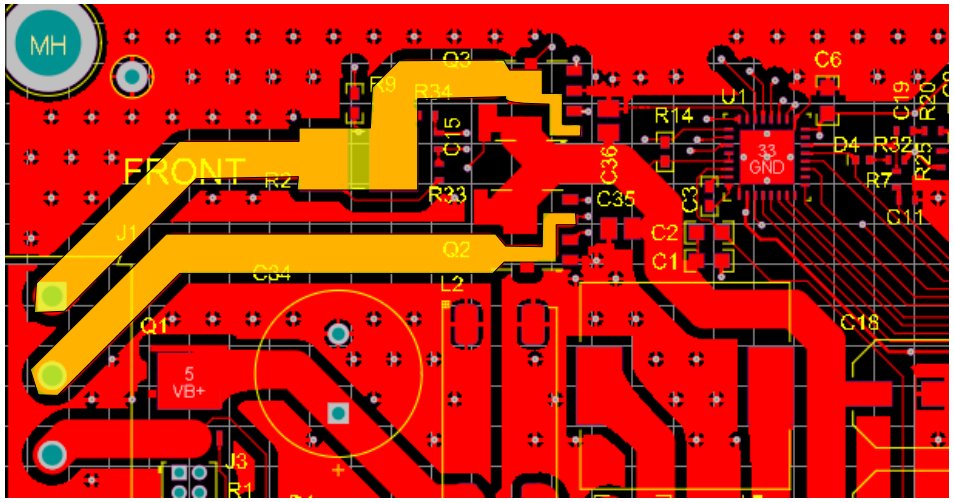
→ Generating EMC as an antenna

Minimize the switching node as much as possible

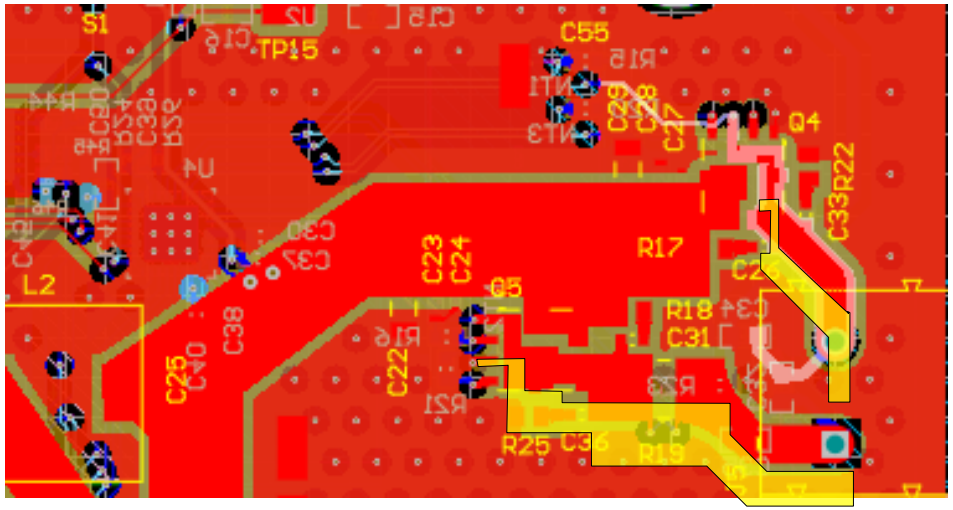
Minimize Switching Node Area

Top Layer

Not Optimized

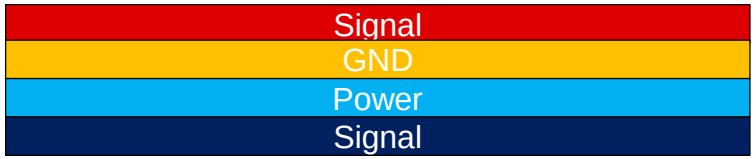


Better

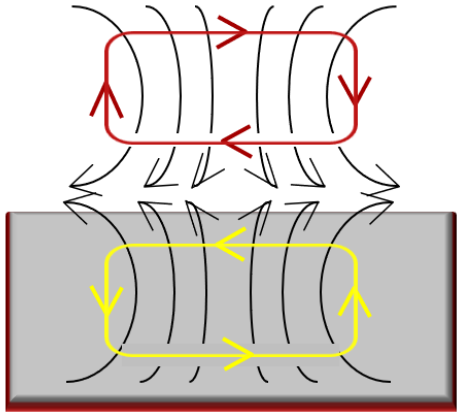


PCB Layer Stack

- PCB should have 4 layers with the following stack up:

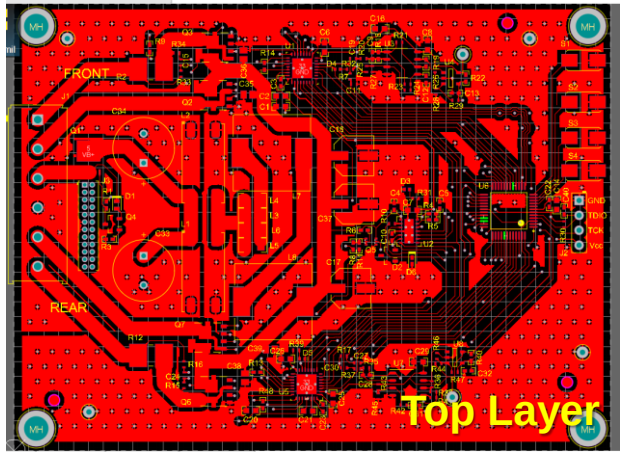


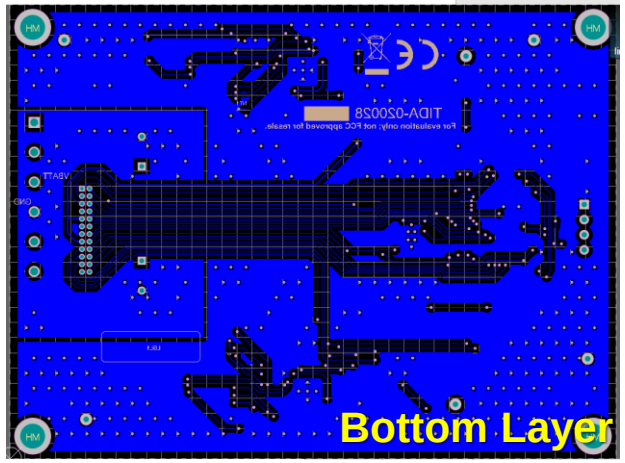
- The GND layer should be continuous without any gaps
- The GND layer minimizes the overall impedance of the GND return path as well as minimizing the ground return loops.
- Induced eddy currents in the GND layer helps to cancel out magnetic fields generated from the top layer



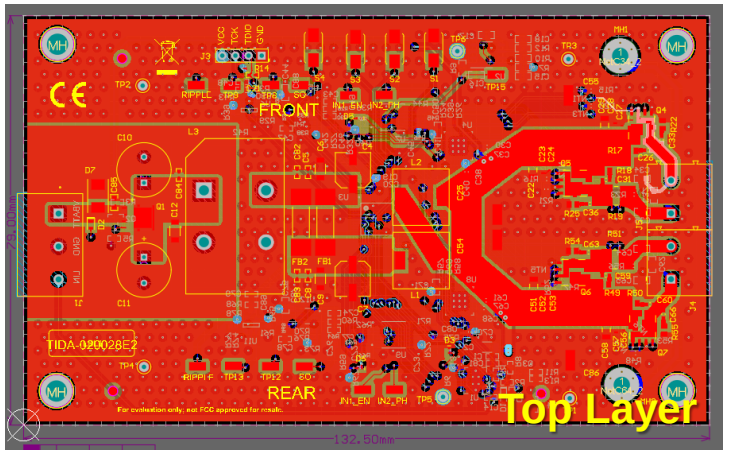
PCB Layer Stack

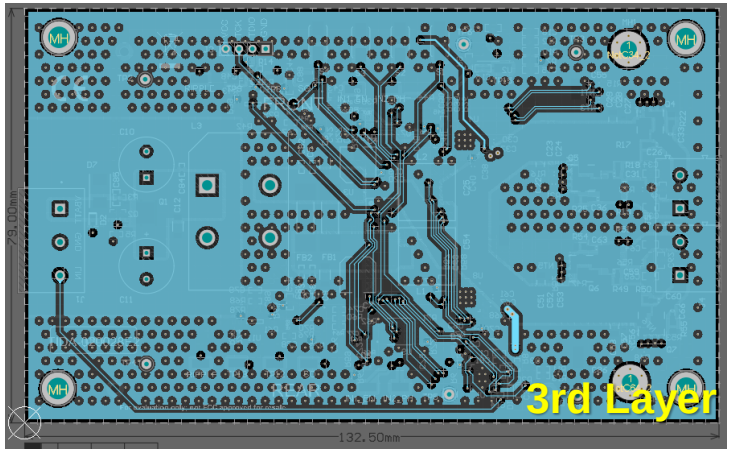
Not Optimized

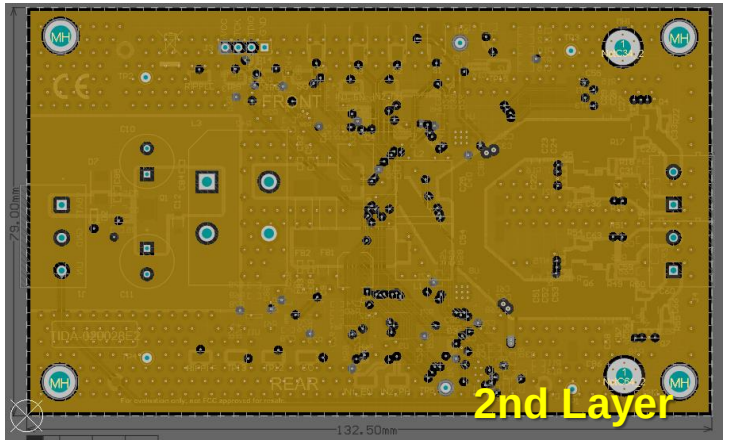


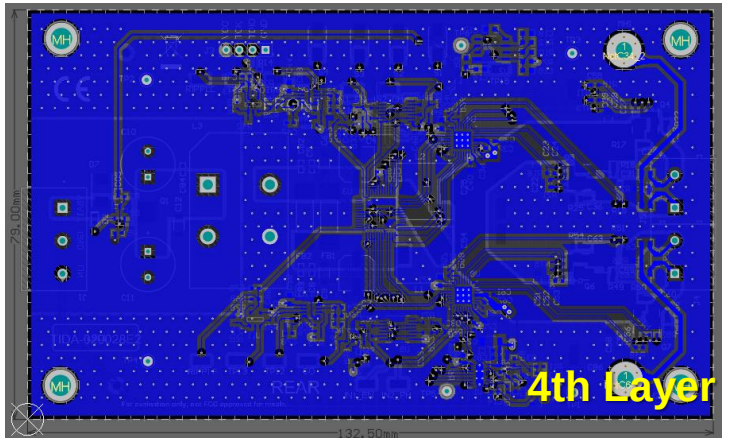


Better



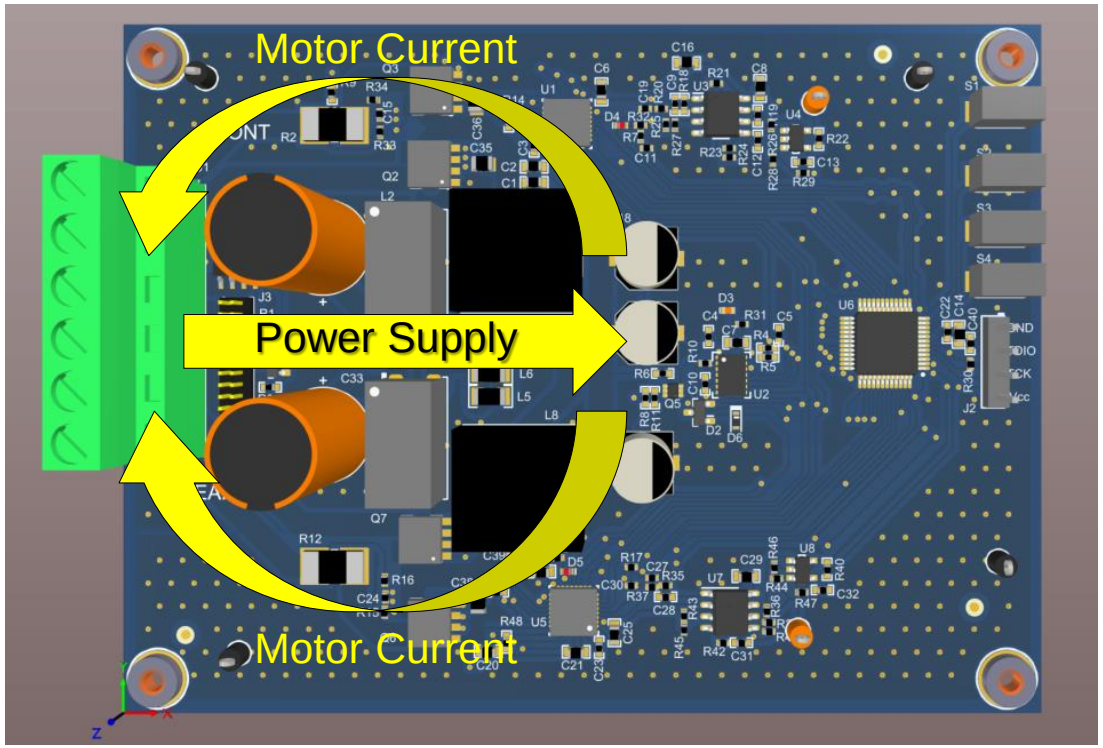




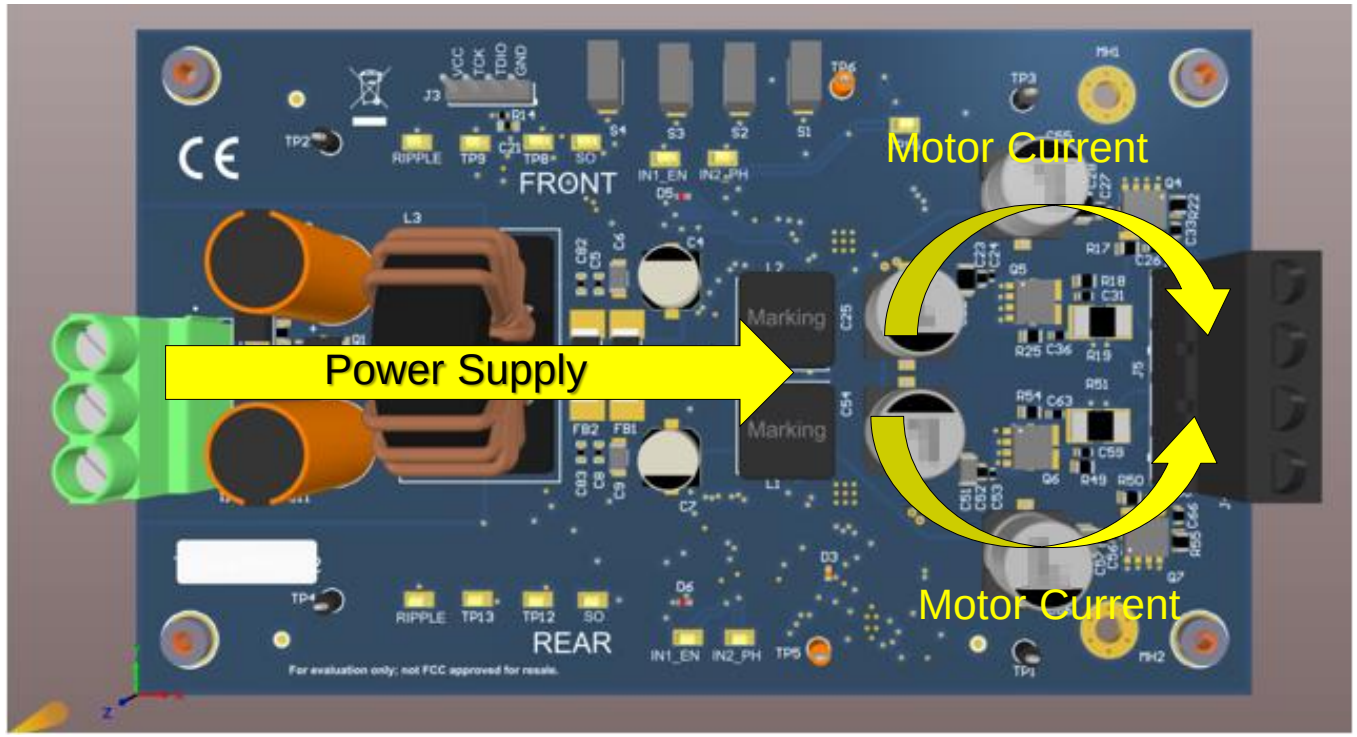


Separate Input & Output Connector

Not Optimized

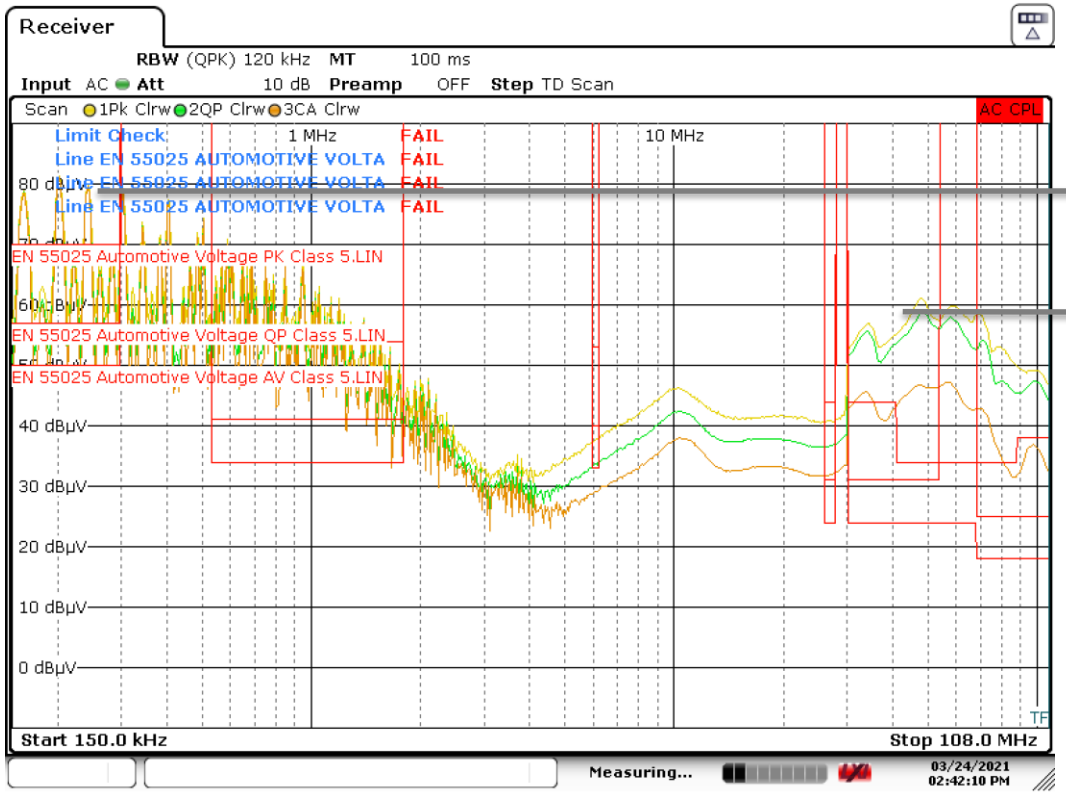


Better



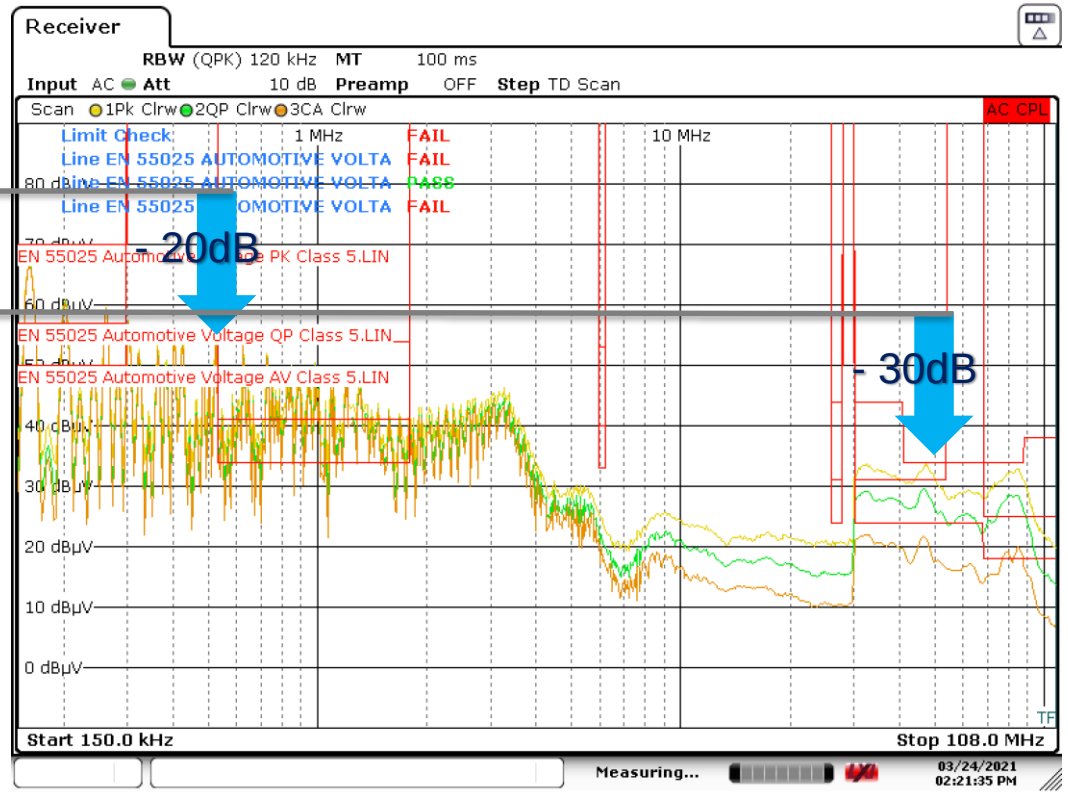
Separate the power supply input and output to motor to minimize the noise coupling

EMC results – Layout comparison



Date: 24.MAR.2021 14:42:09

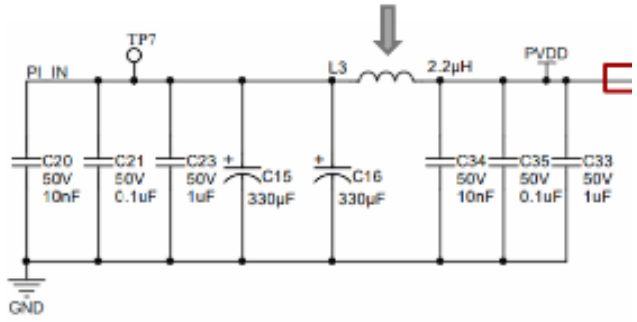
PCB Version 1

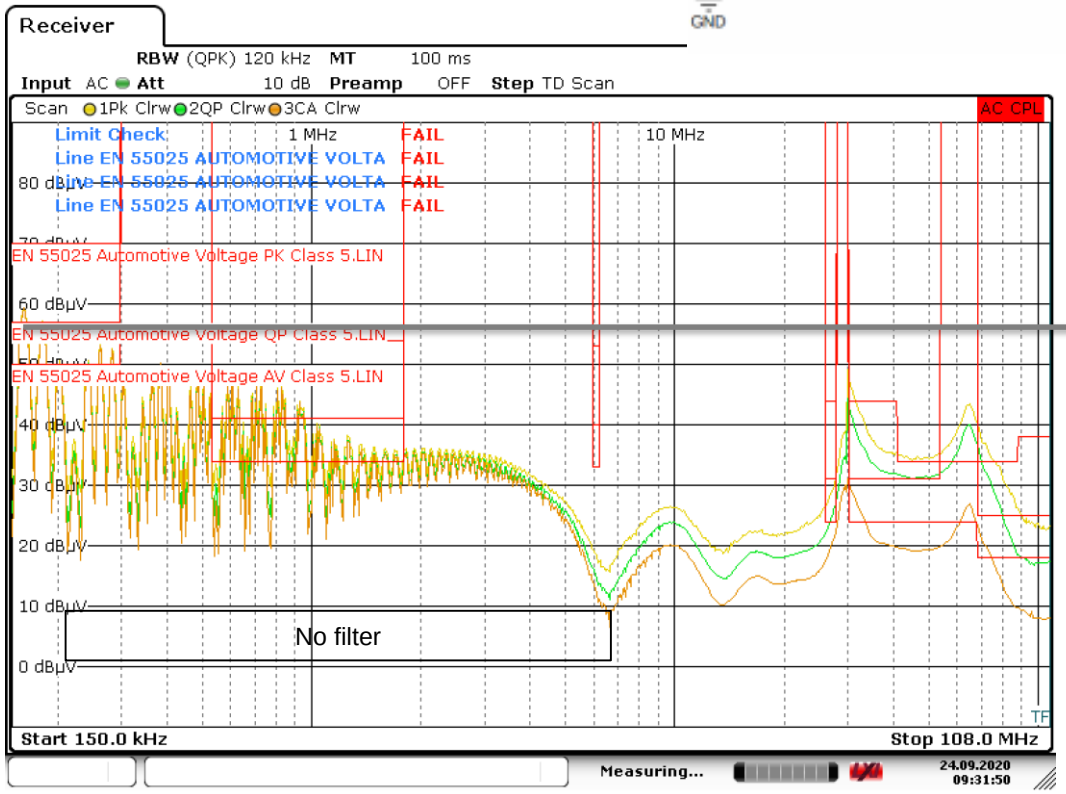


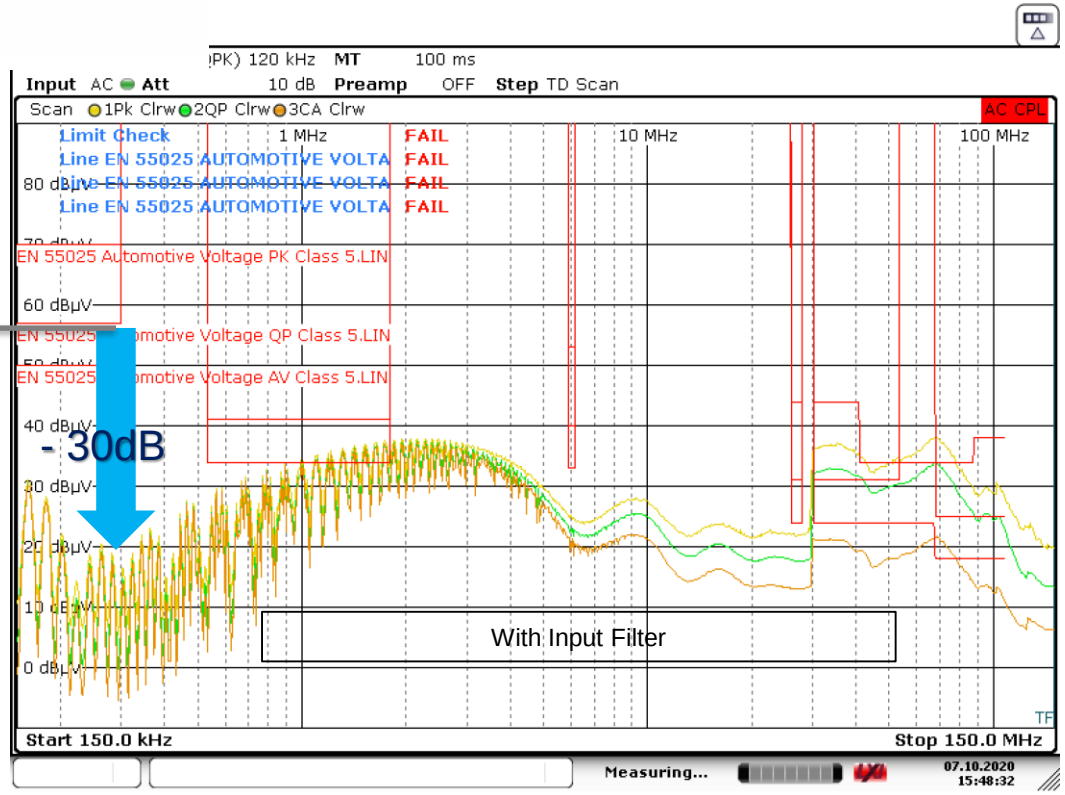
Date: 24.MAR.2021 14:21:35

PCB Version 2

EMC results – differential mode input filter





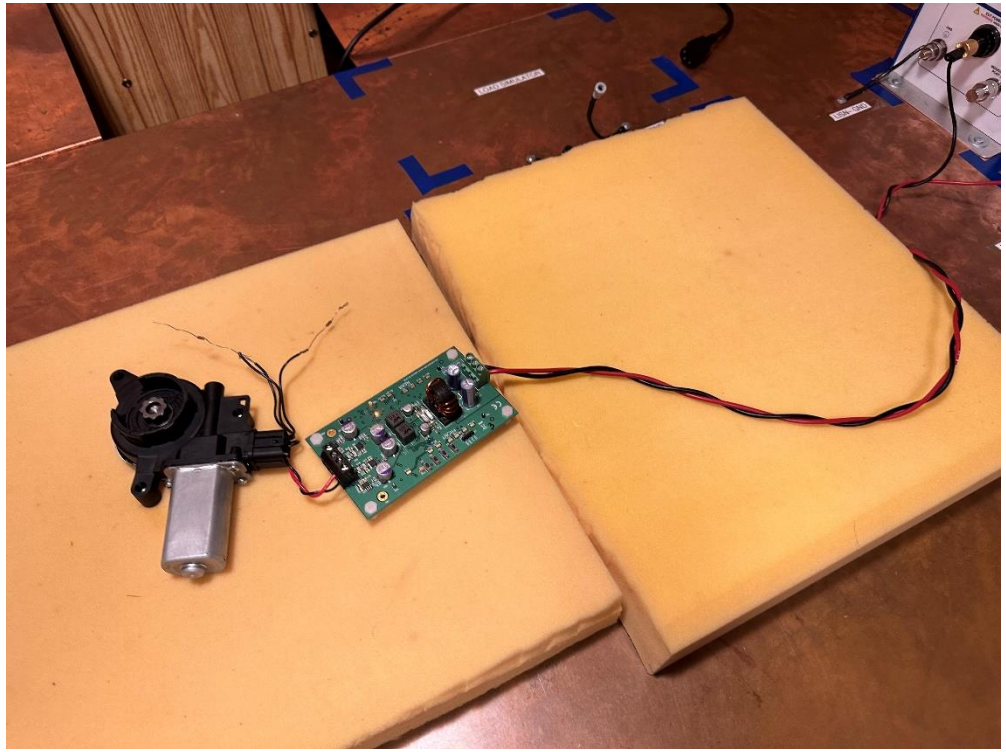


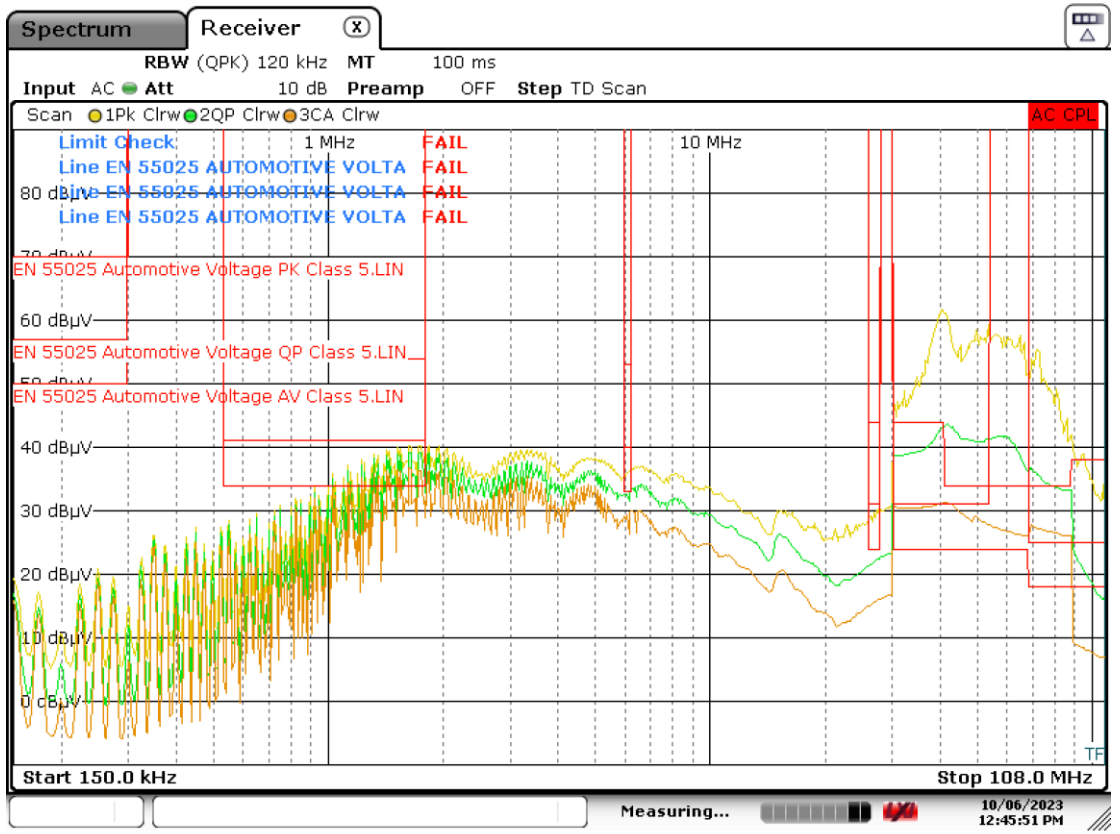
Date: 24.SEP.2020 09:31:50

Date: 7.OCT.2020 15:48:32

CONDUCTED EMISSIONS DEBUGGING TECHNIQUES

BOARD ALL FILTERS

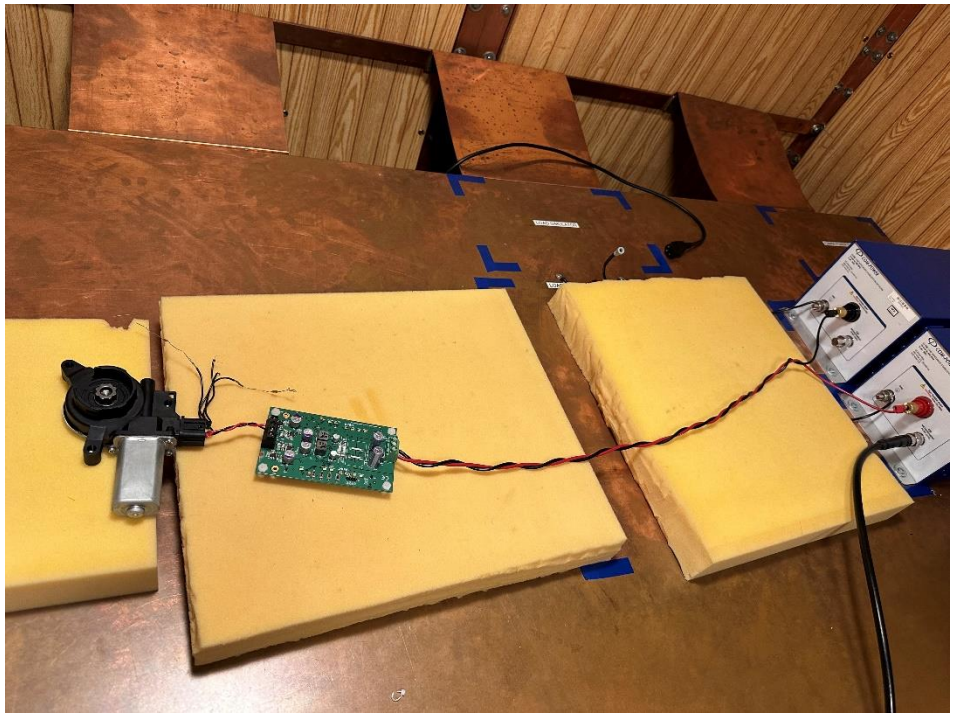


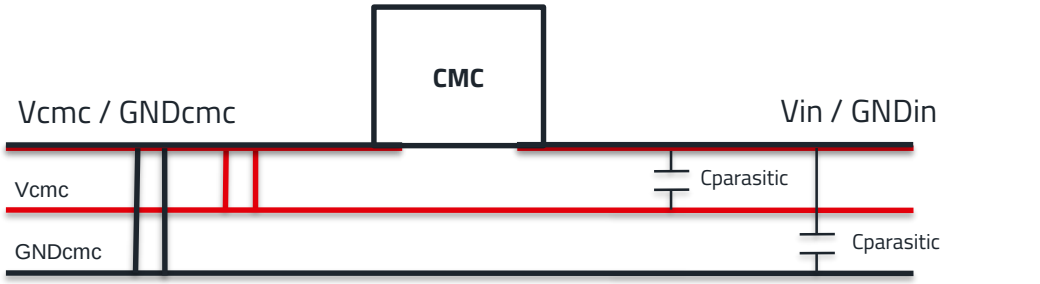


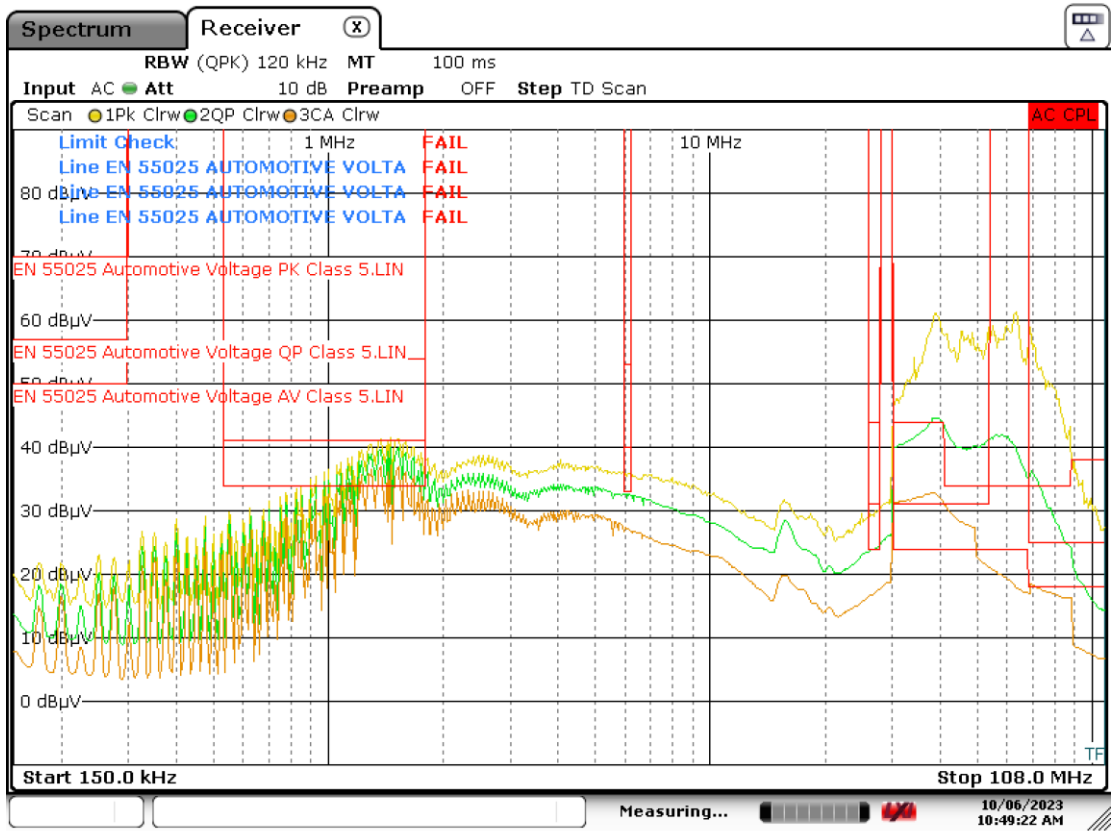
Date: 6.OCT.2023 12:45:51

NO COMMON MODE CHOKE

Twisted cables



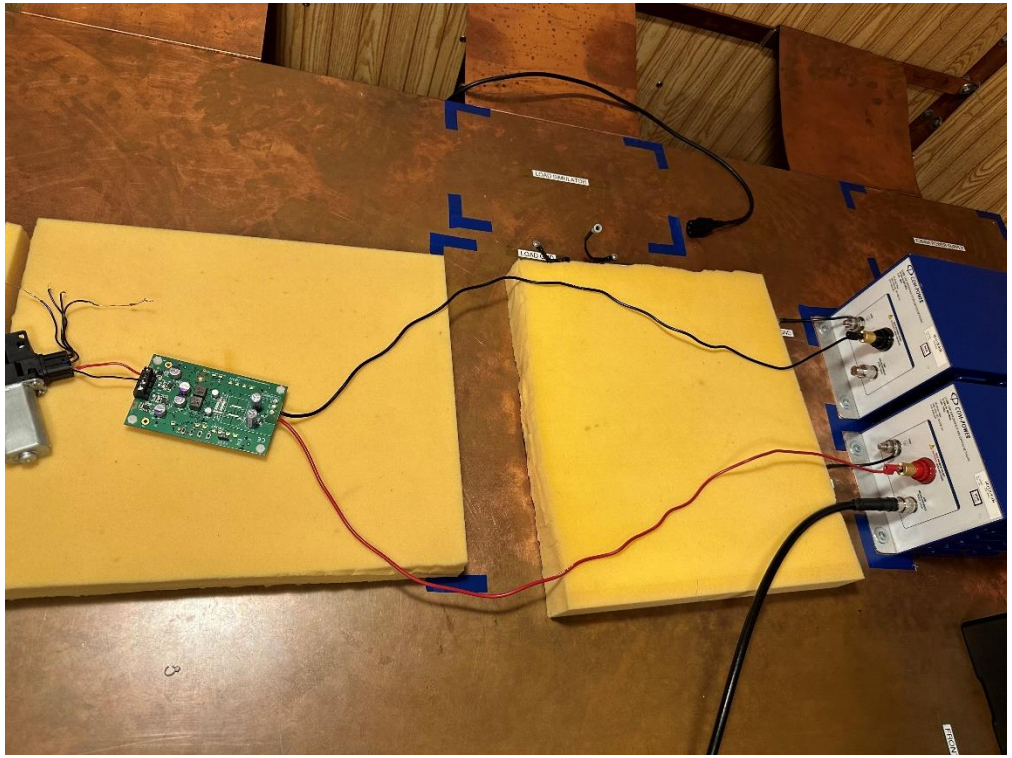


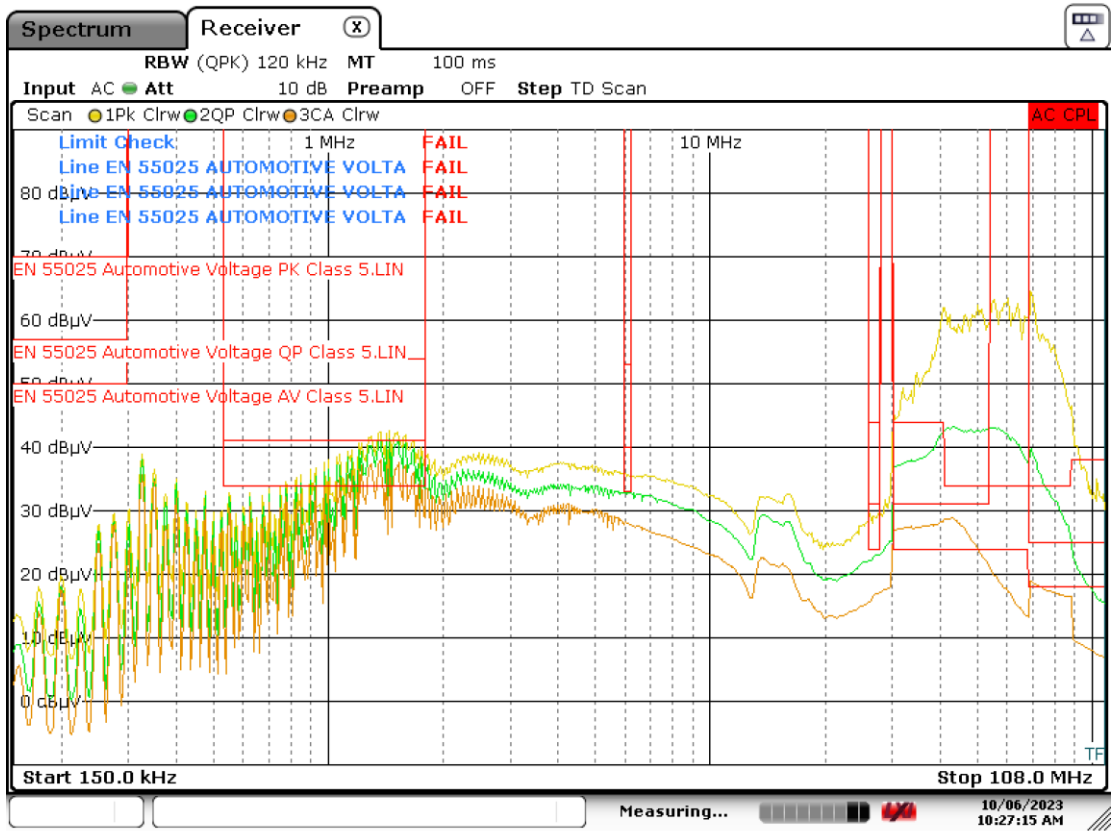


Date: 6.OCT.2023 10:49:22

NO COMMON MODE CHOKE

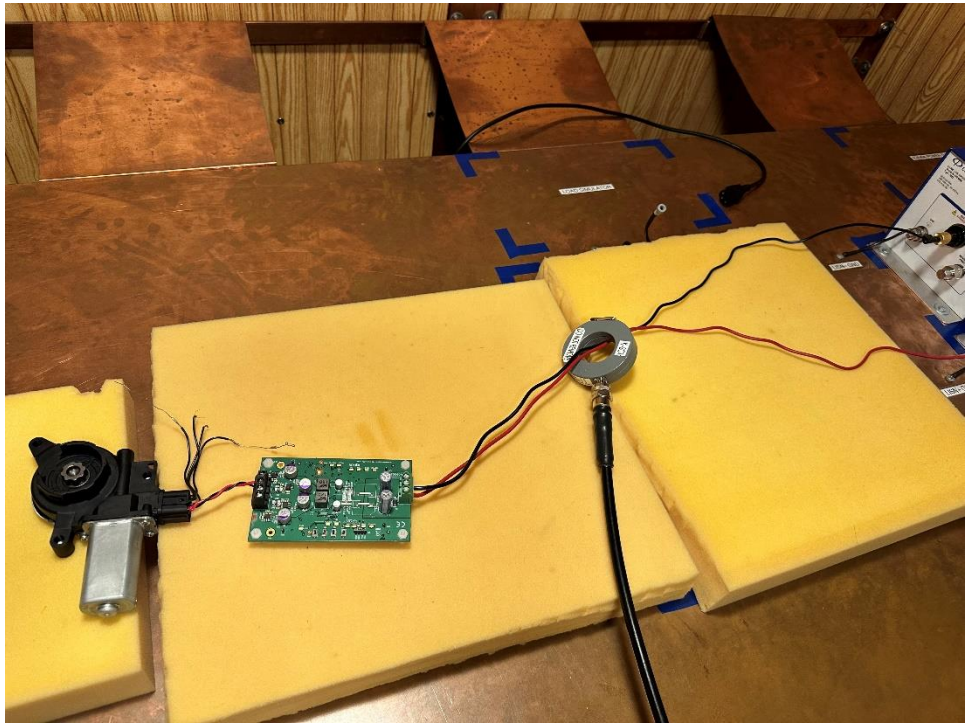
Untwisted cables

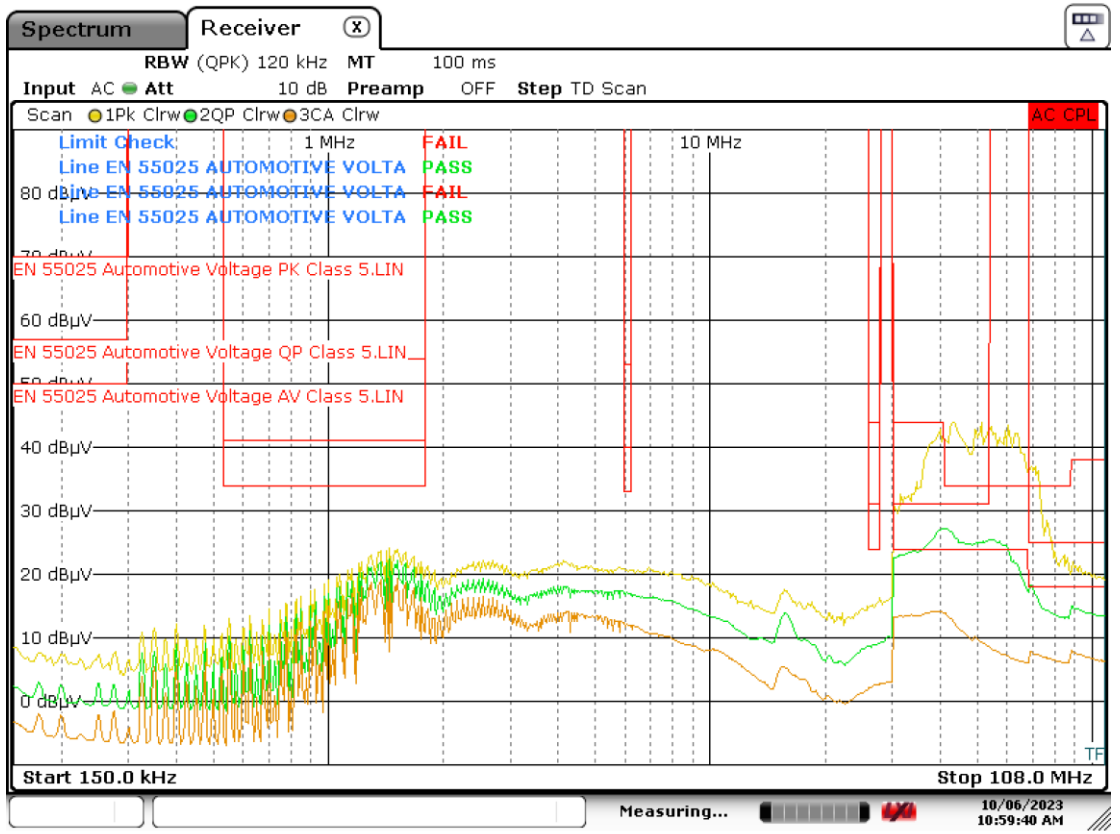




COMMON MODE NOISE MEASUREMT

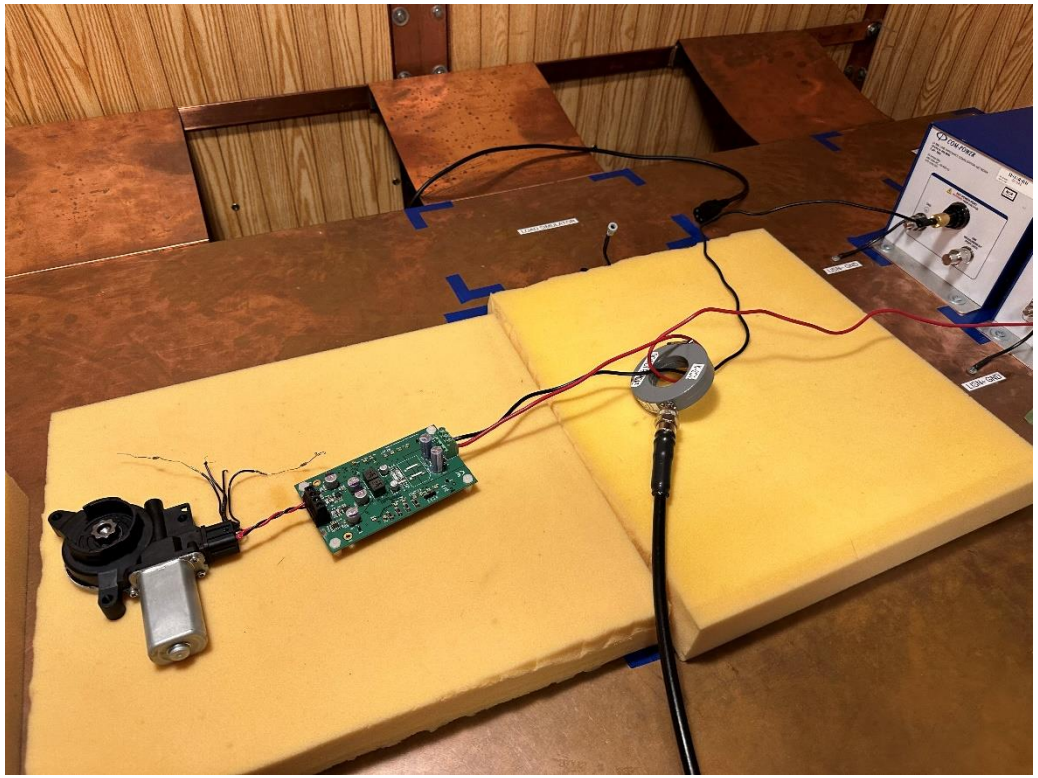
Current Clamp

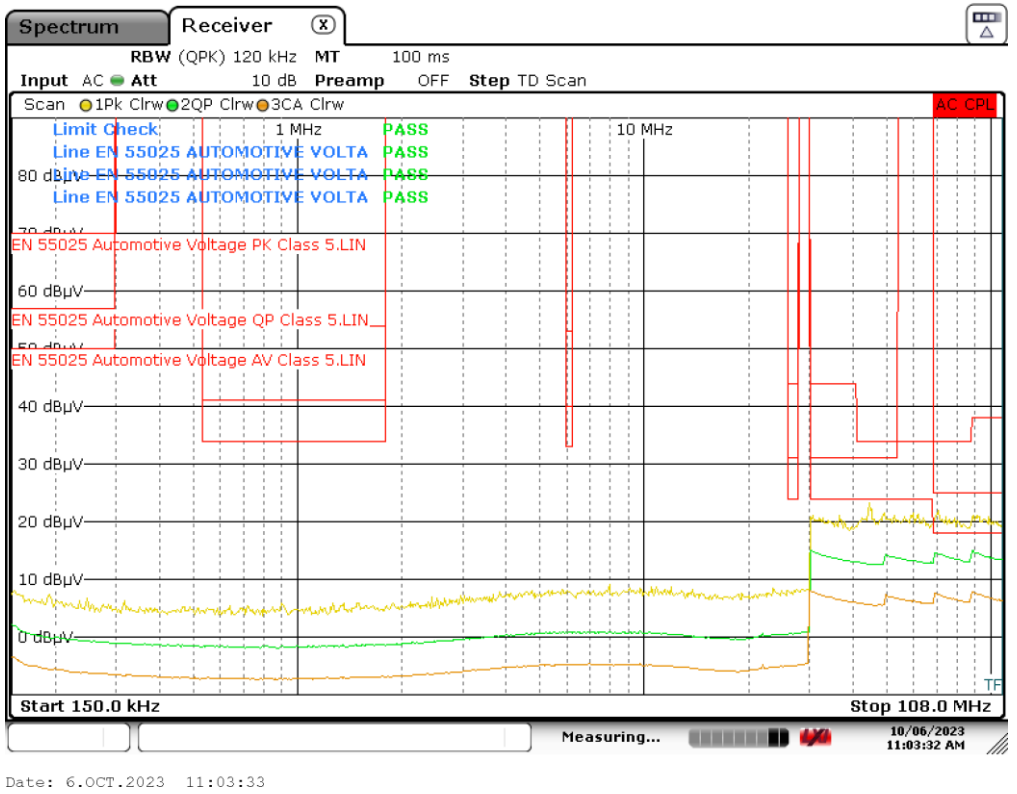




DIFFERENTIAL MODE NOISE MEASUREMENT

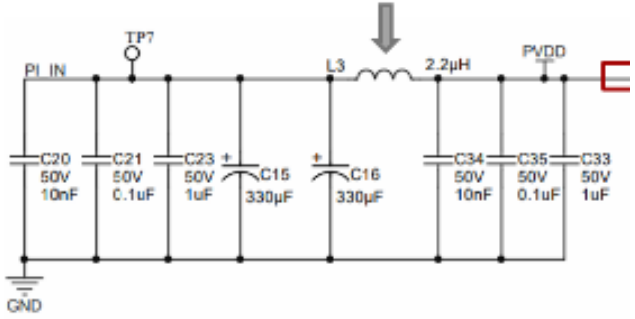
Current Clapm

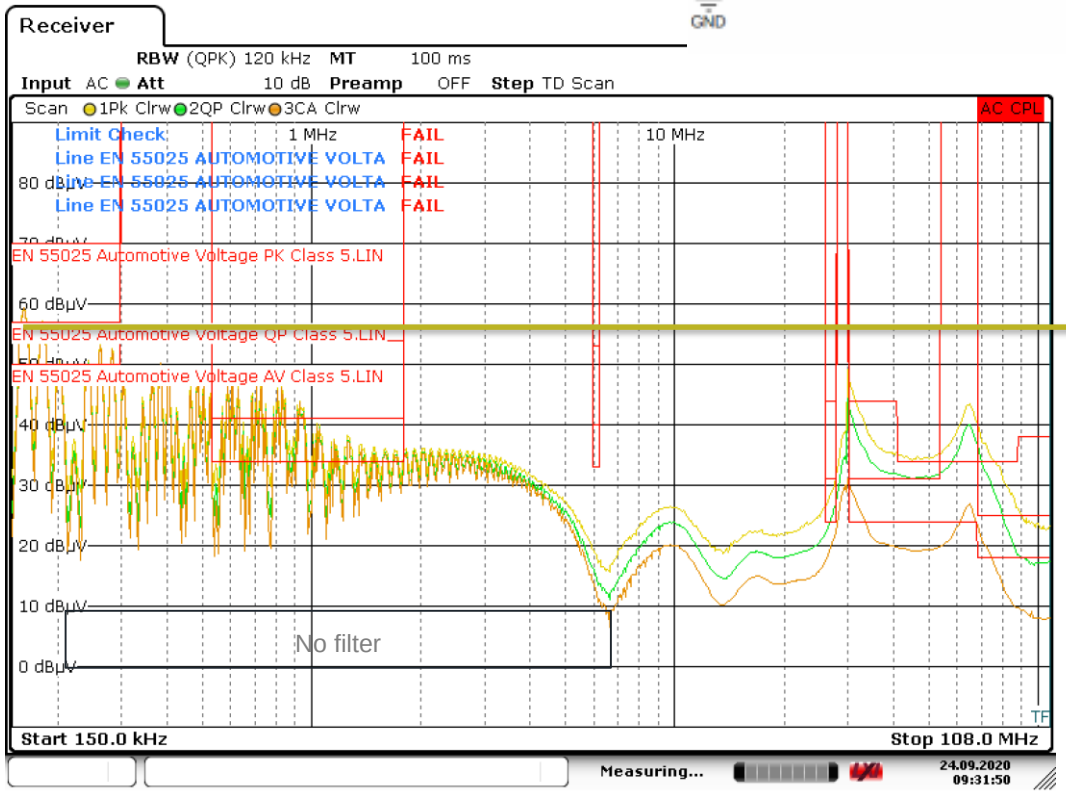




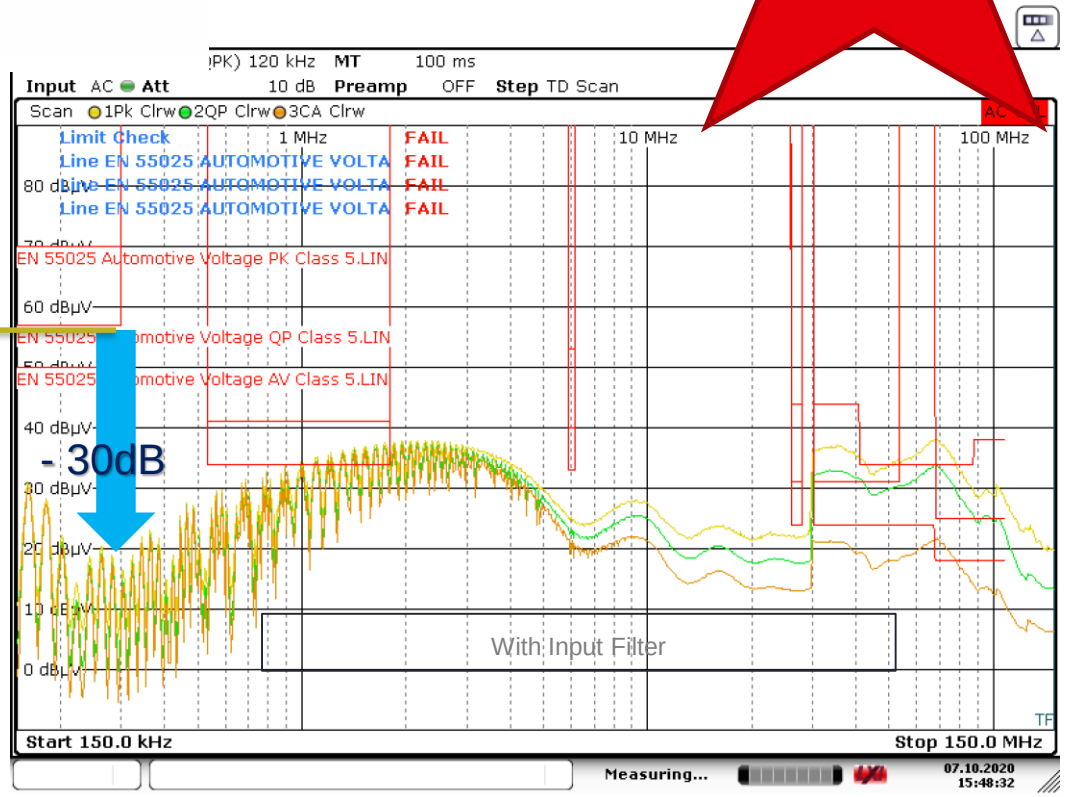
Date: 6.OCT.2023 11:03:33

EMC RESULTS – DIFFERENTIAL MODE INPUT FILTER



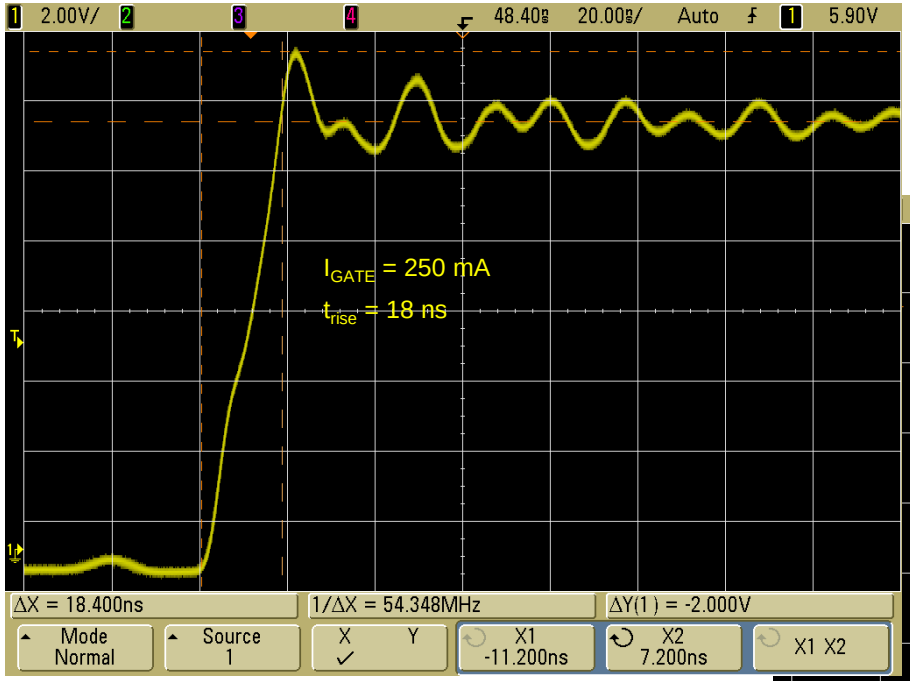


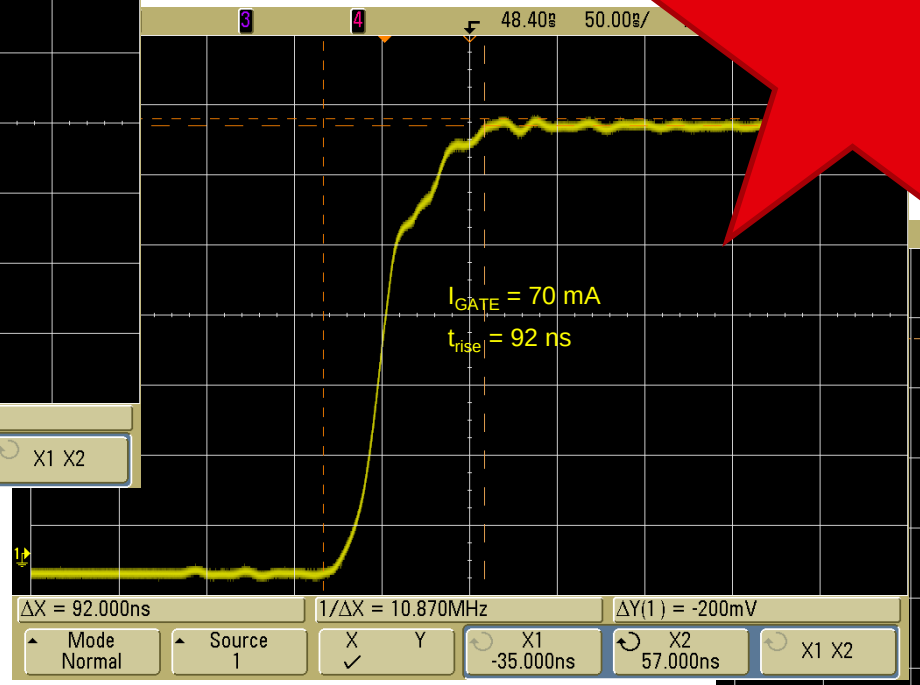
Date: 24.SEP.2020 09:31:50

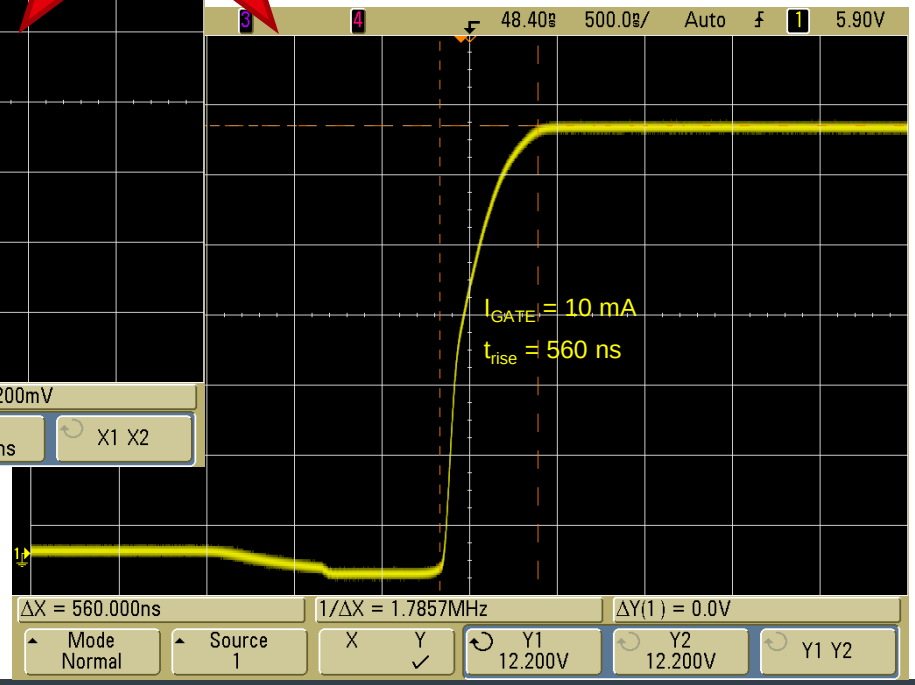


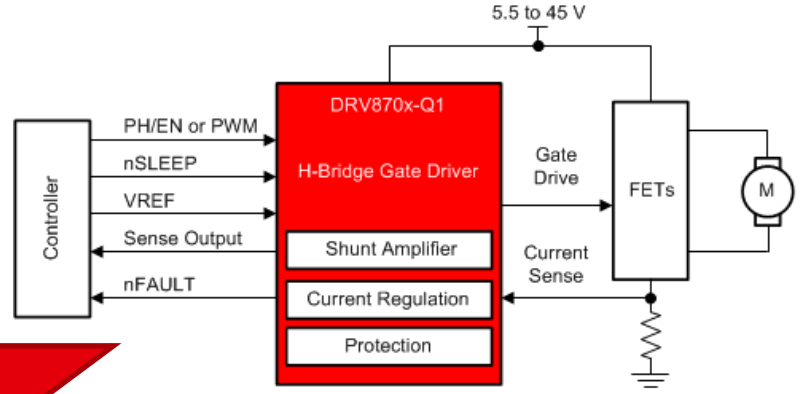
Date: 7.OCT.2020 15:48:32

EFFECT OF GATE CURRENT IN TIME DOMAIN



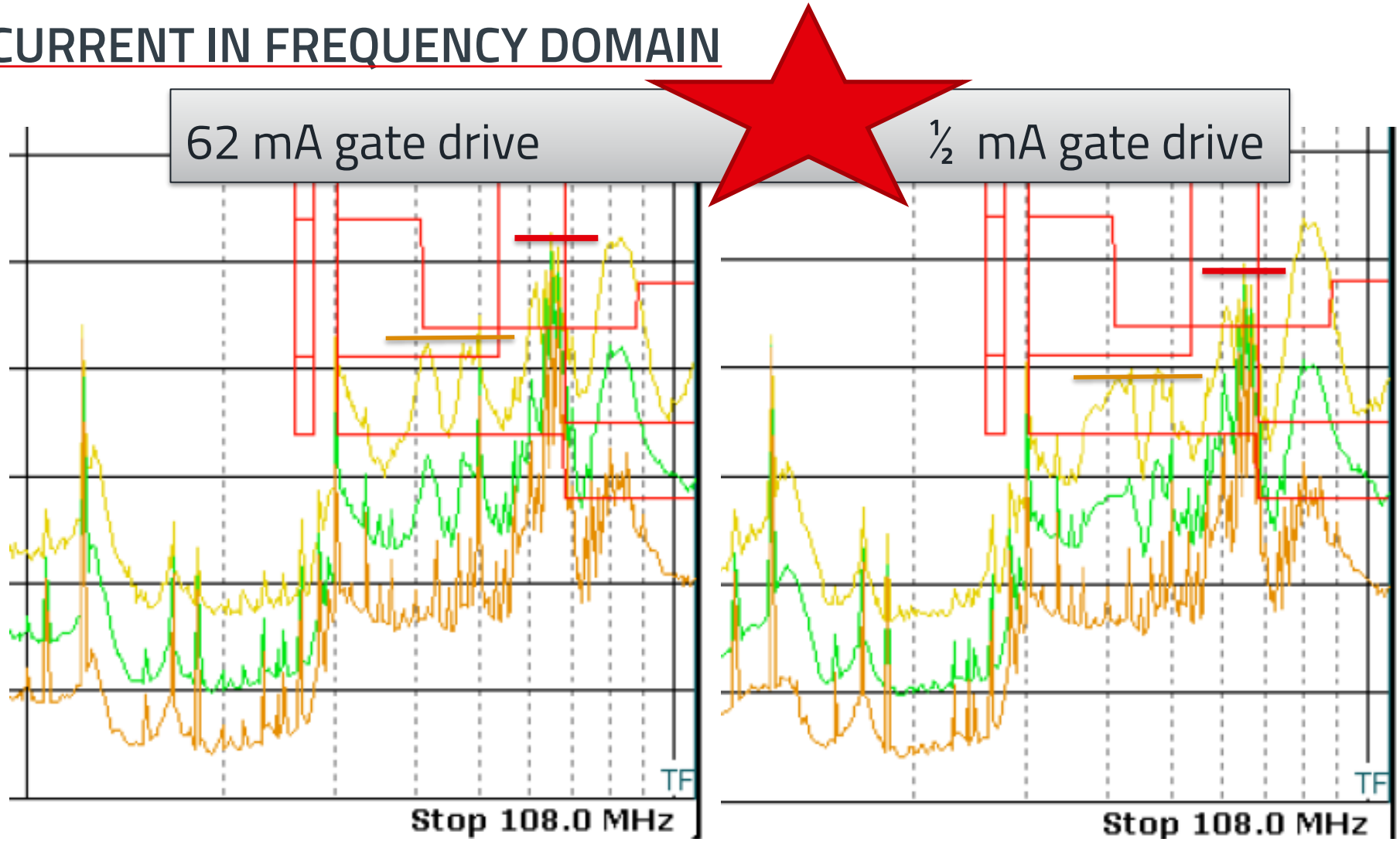






EFFECT OF GATE CURRENT IN FREQUENCY DOMAIN

- Change the rise time of PWM edges at 20 kHz
- Reduced emissions at > 10 MHz frequencies



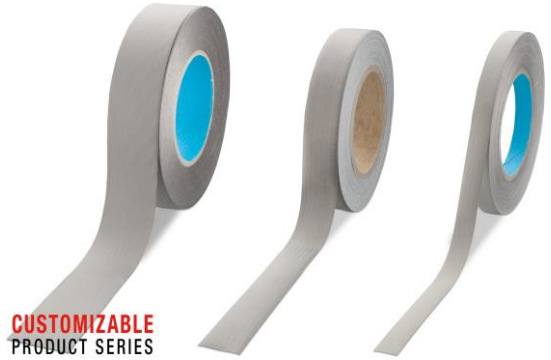
DEBUGGING

tools

Copper and Aluminum Tape

Copper Tape
3003310A
Aluminum Tape
3013310A

Shielding textiles Tape



Shielding textiles
33020

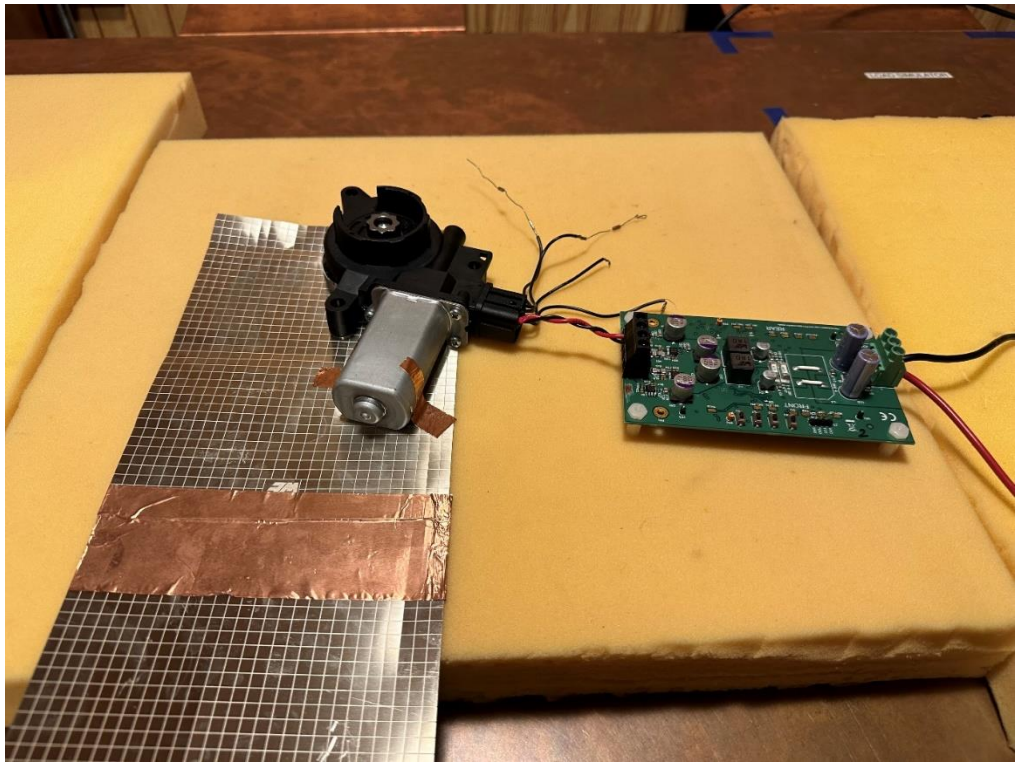
DIY Shielding Plate

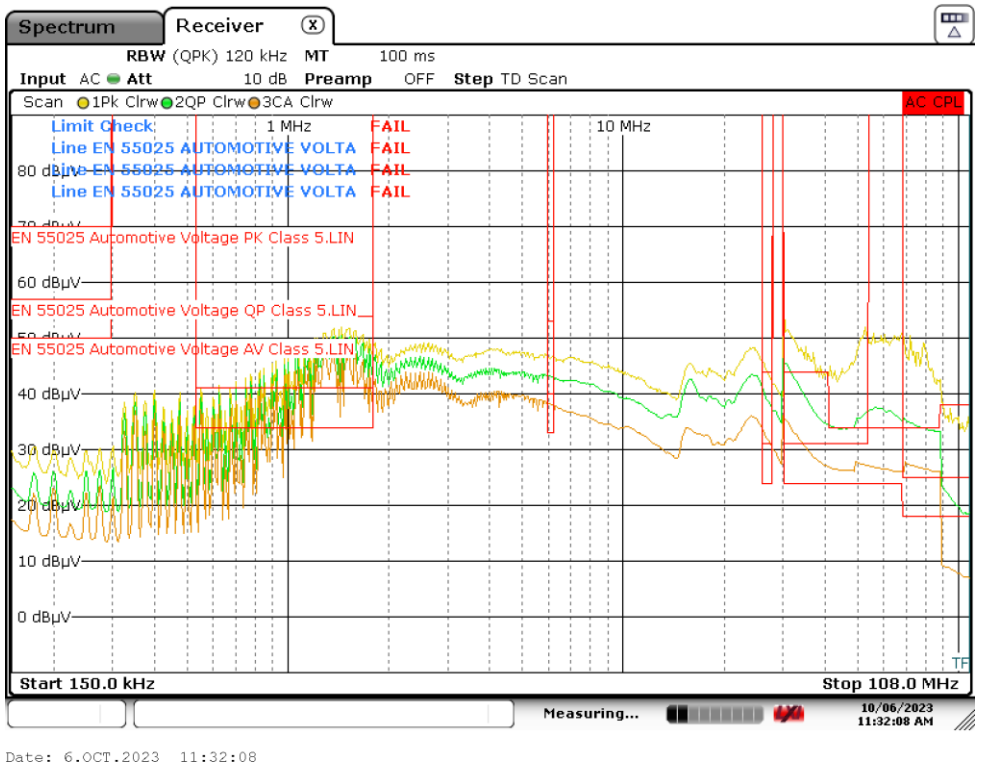
PN 360002

Clamp-on Ferrites

Start-tec

SHIELDING UNDER MOTOR

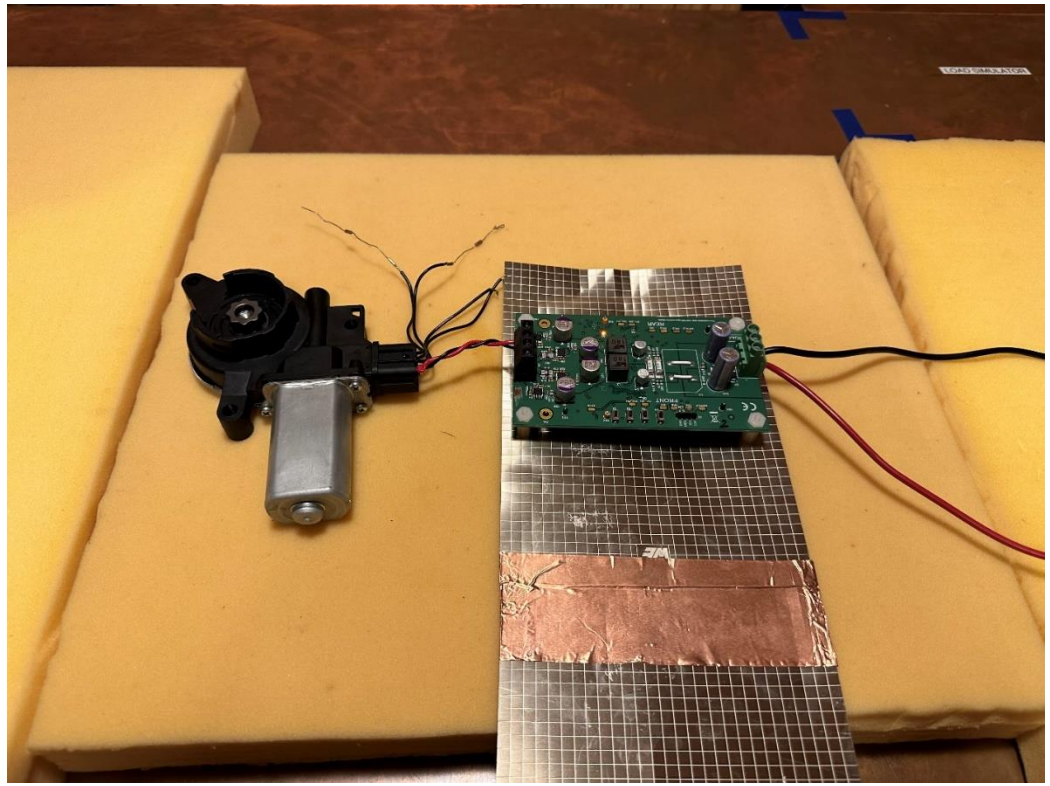


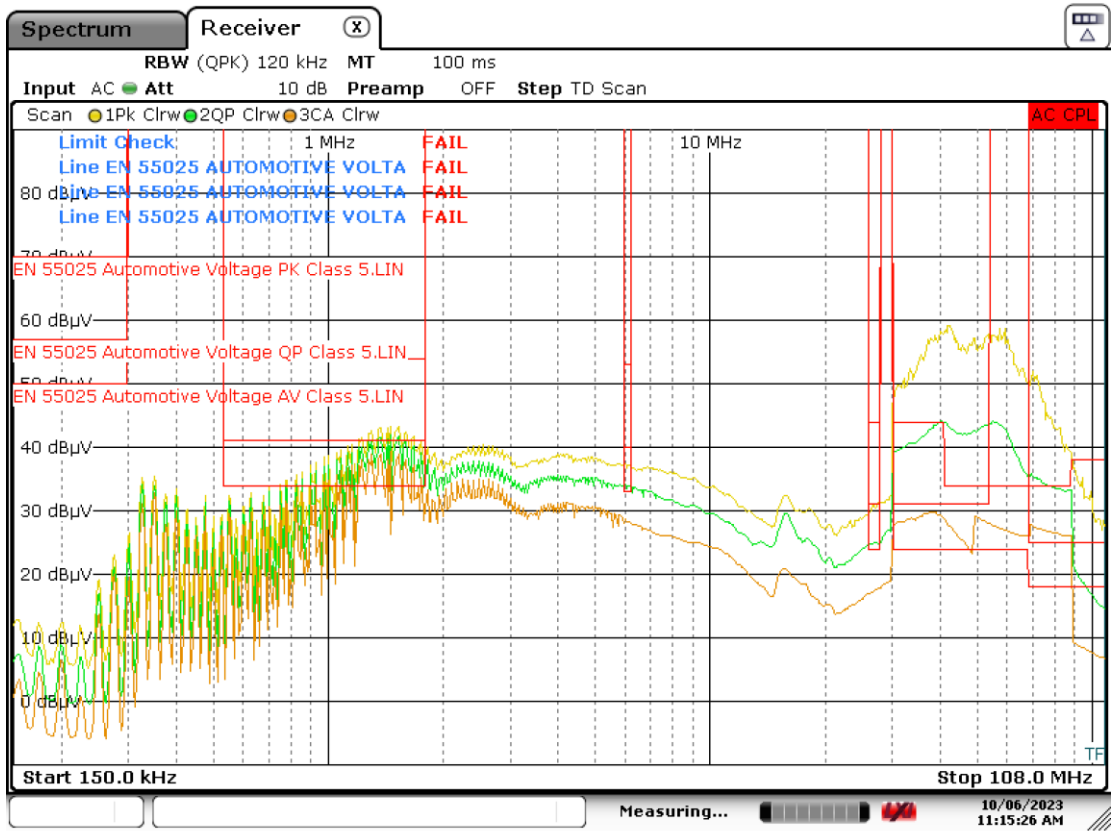


Date: 6.OCT.2023 11:32:08

SHIELDING UNDER BOARD

No Grounded

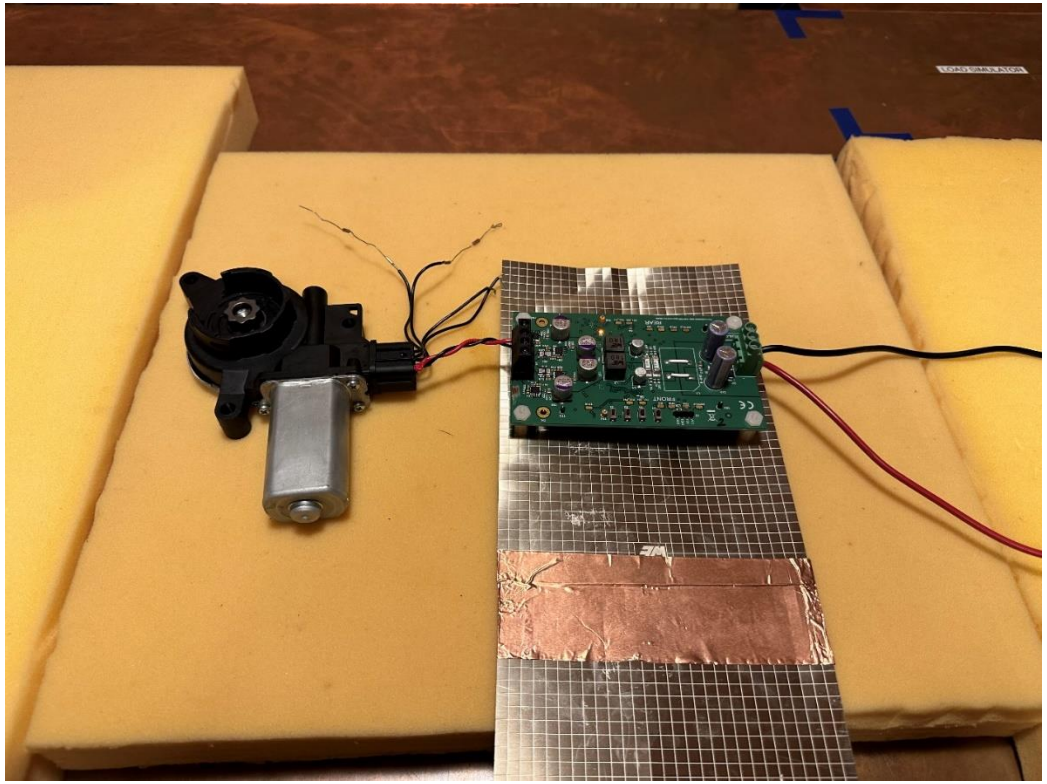


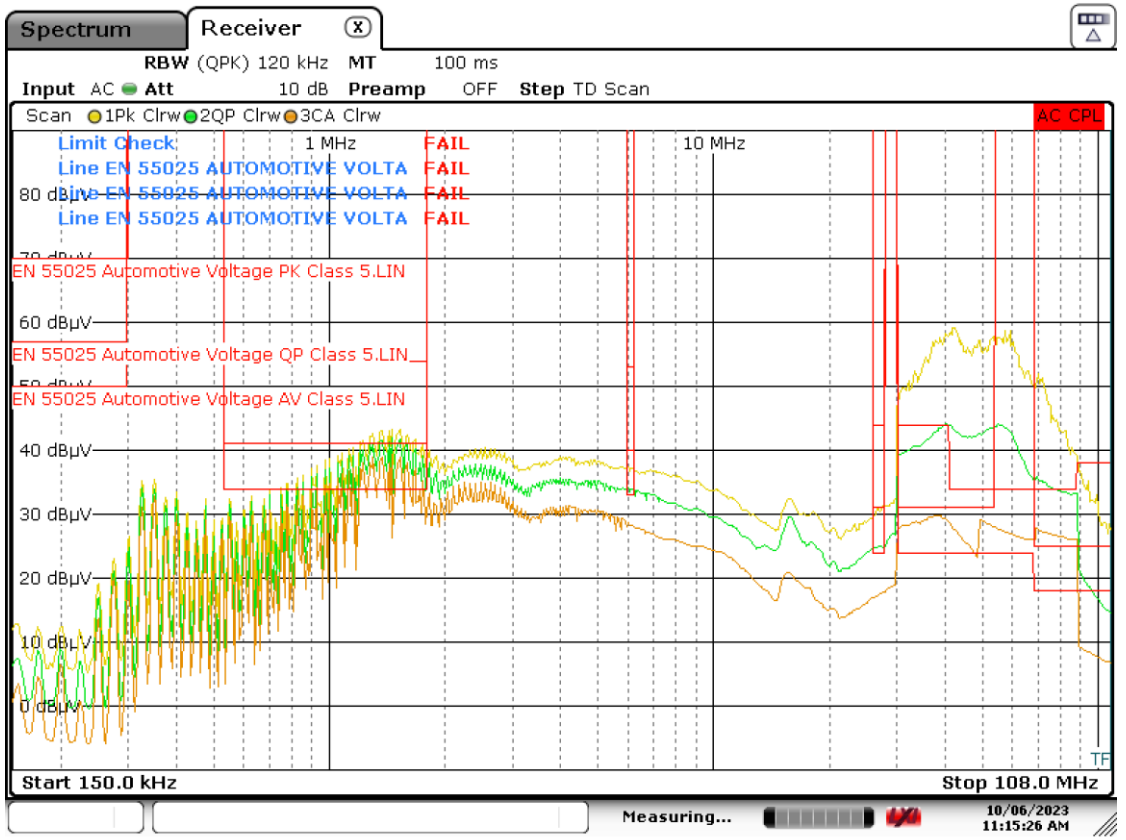


Date: 6.OCT.2023 11:15:26

SHIELDING UNDER BOARD

No Grounded

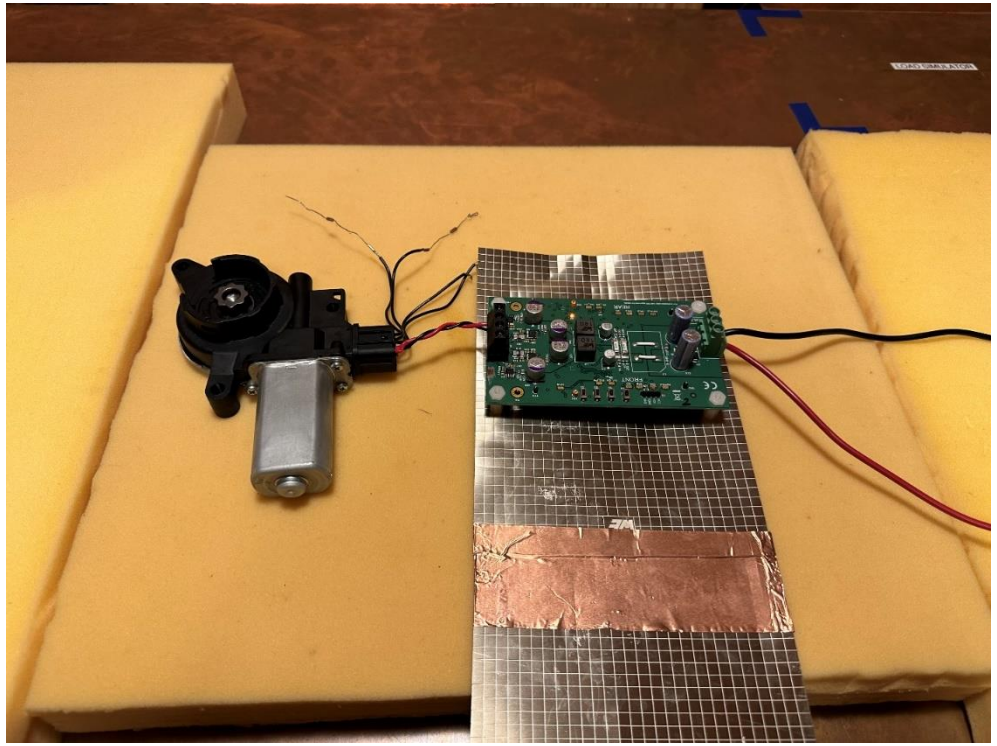


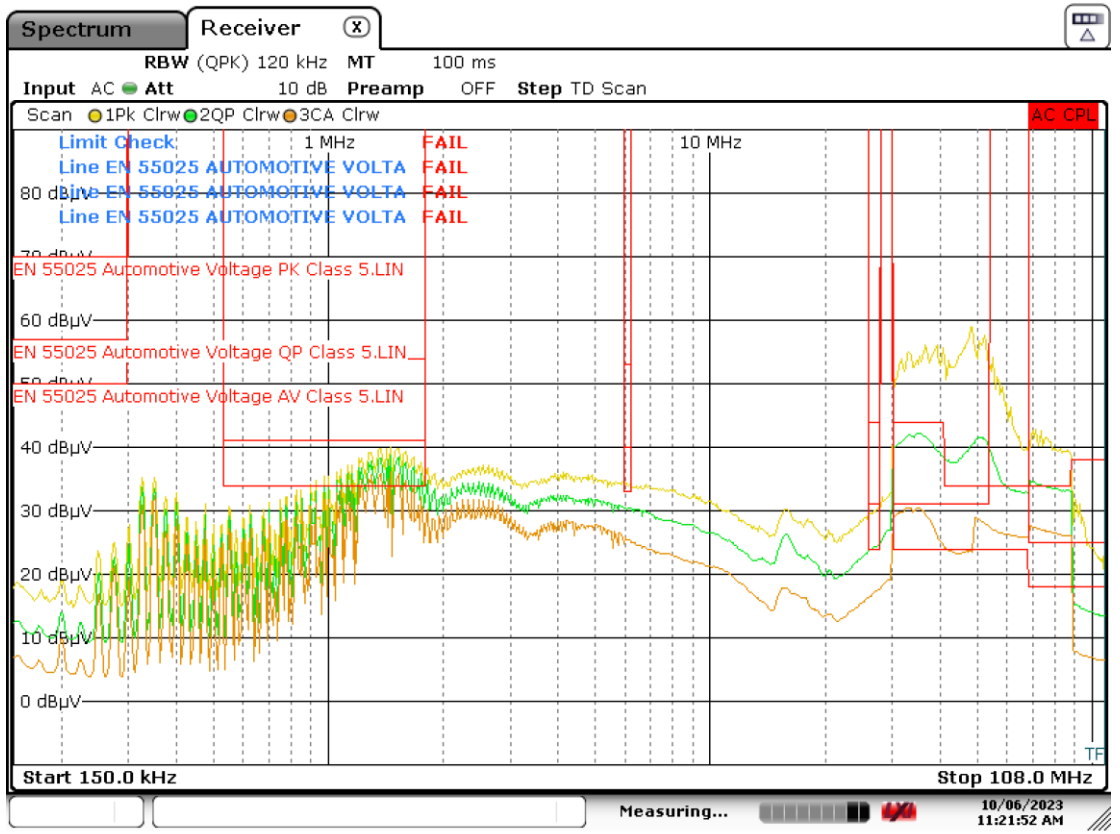


Date: 6.OCT.2023 11:15:26

SHIELDING UNDER BOARD

Ground

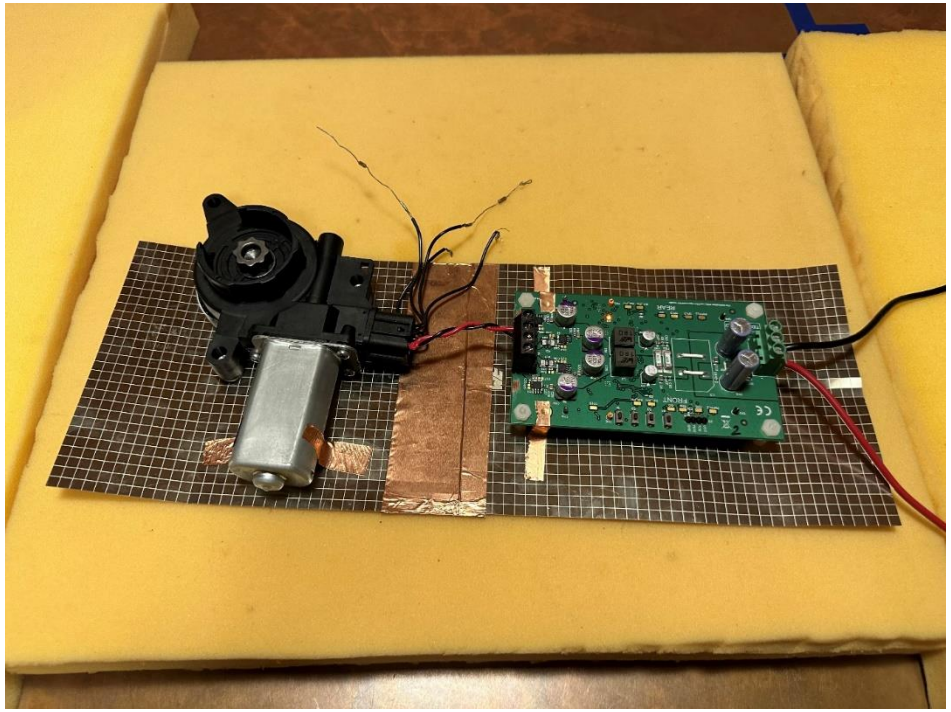


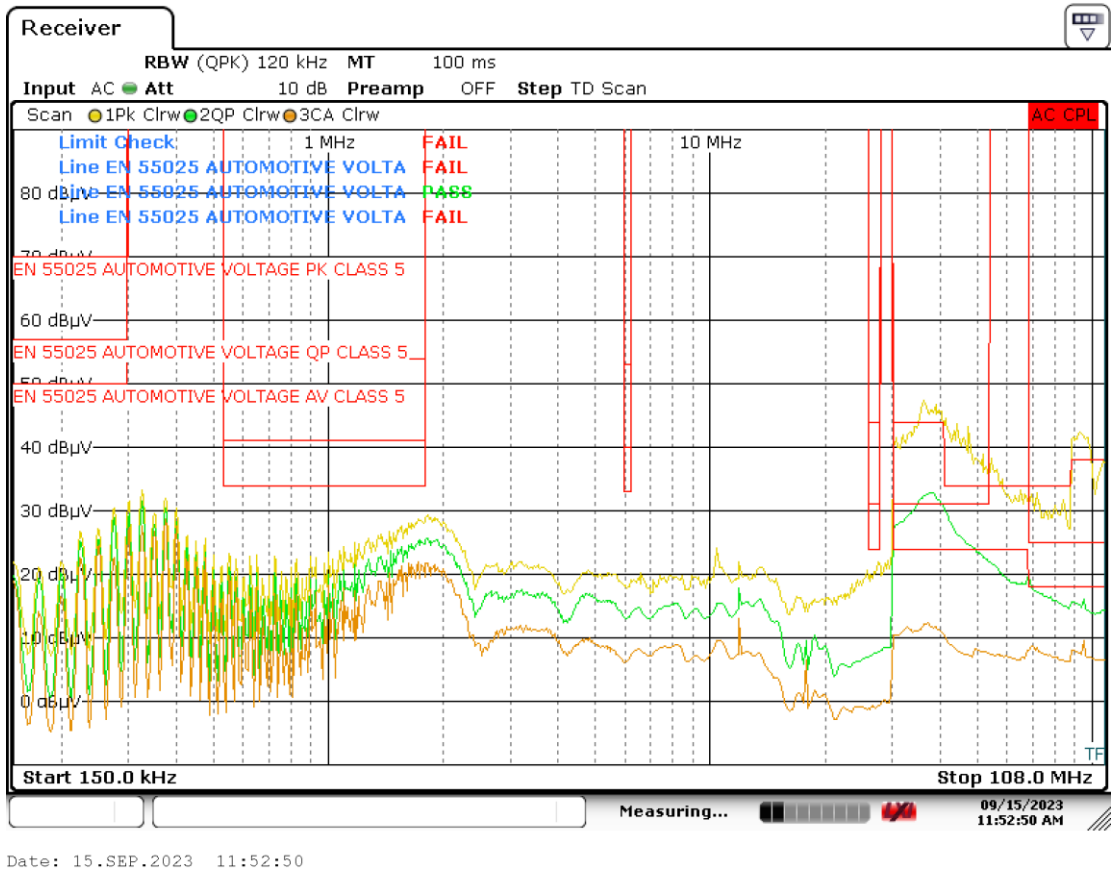


Date: 6.OCT.2023 11:21:52

SHIELDING UNDER MOTOR AND BOARD

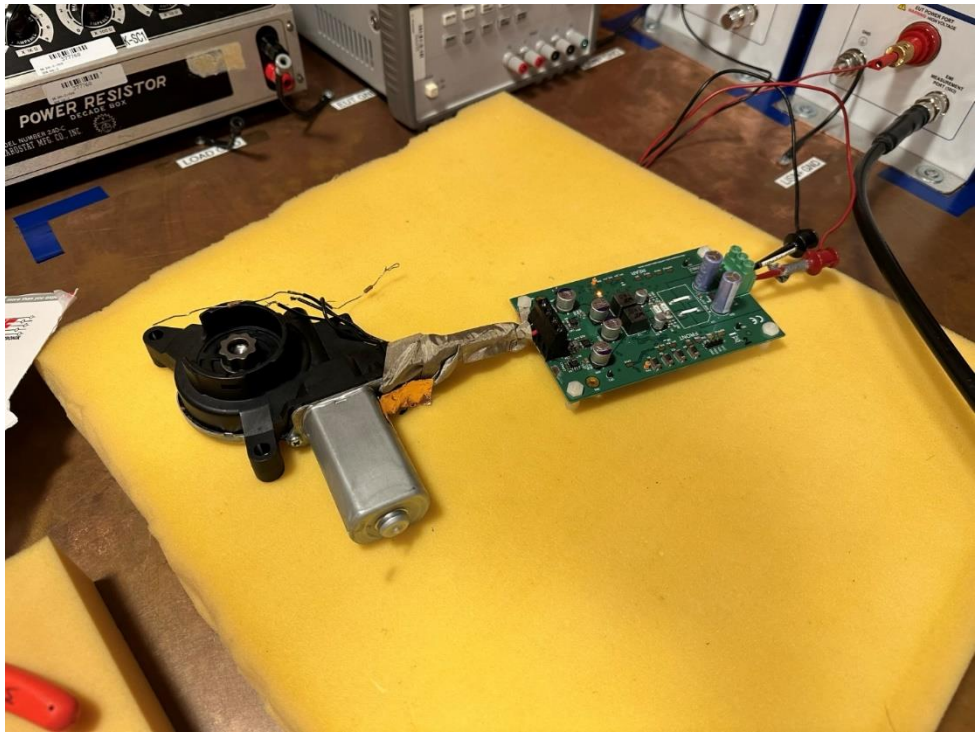
Shielding under both

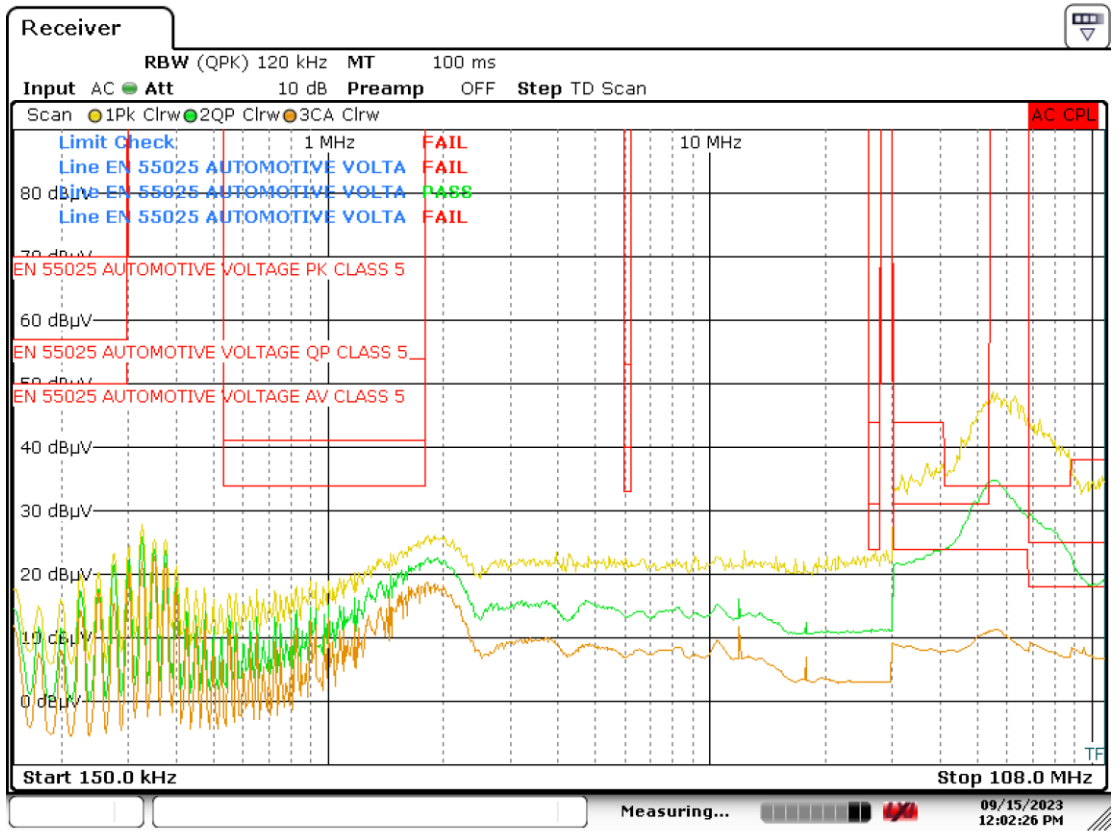




Date: 15.SEP.2023 11:52:50

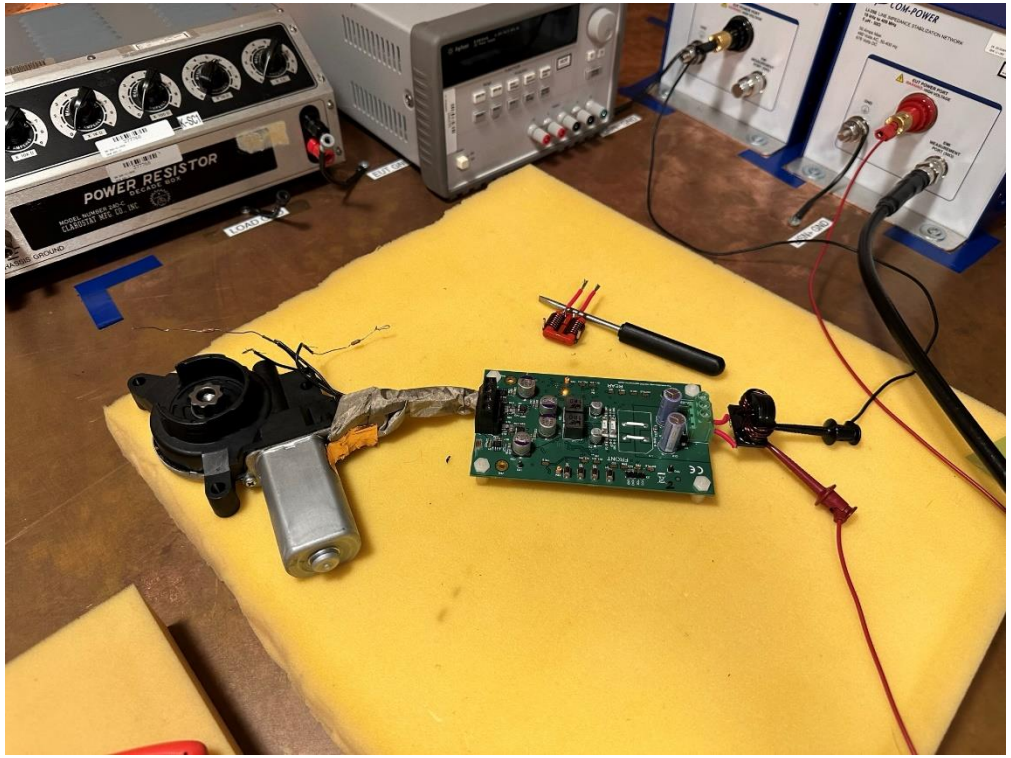
CABLE SHIELDED AND GROUNDED

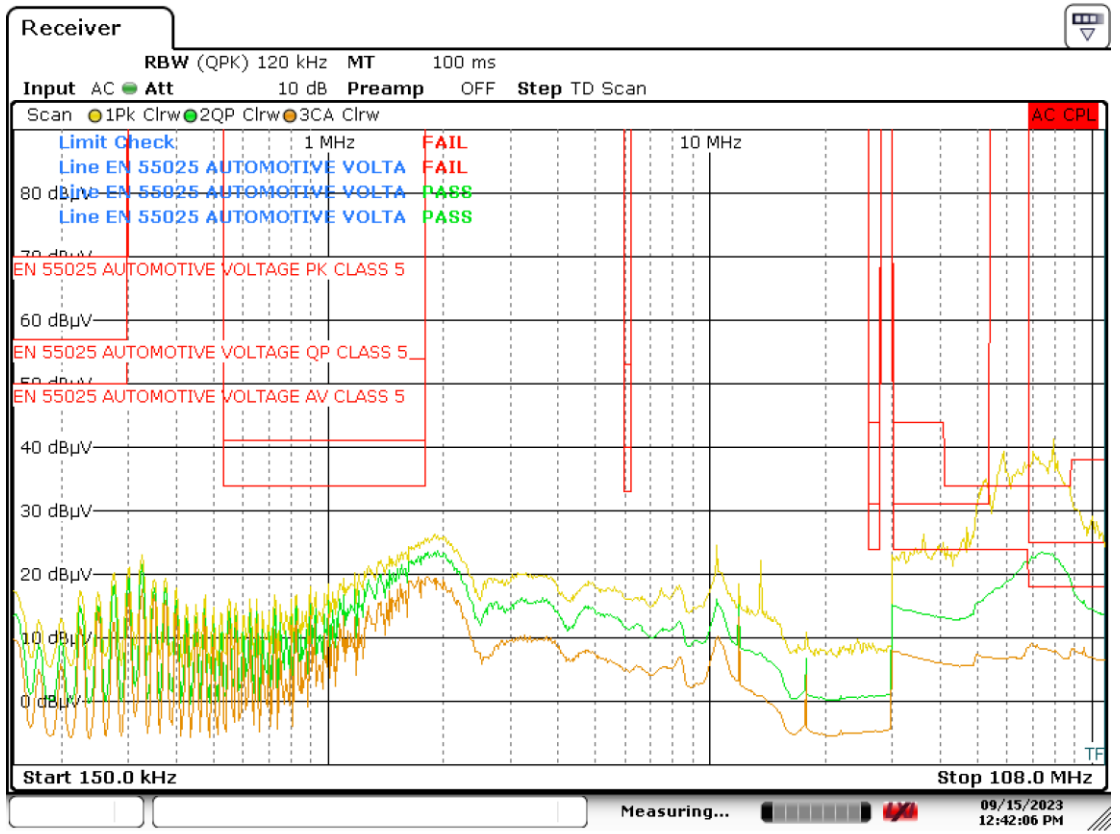




Date: 15.SEP.2023 12:02:26

CABLE SHIELDED AND GROUNDED





Date: 15.SEP.2023 12:42:05

TAKEAWAY

- Design with EMC in mind
- Identify your dV/dT and dI/dT loops and optimize them
- Define your ground
- Control Rise- and Fall-Time
- Cable Shield Grounding
- Be in control of the noise

Reference:
Design for Electromagnetic Compatibility--In a Nutshell

IT'S TIME FOR QUESTIONS!

Q&A