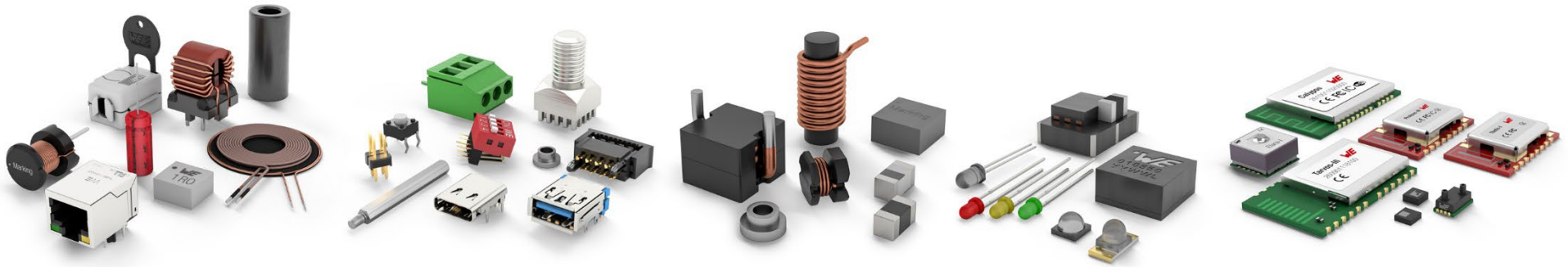


EMC WITH EMC
ELECTROMAGNETIC COMPATIBILITY WITH ELECTROMECHANICAL CONNECTIONS

Technical Academy
Dominik Zeller und Hans Peter Kaiser
Field Application Engineer

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

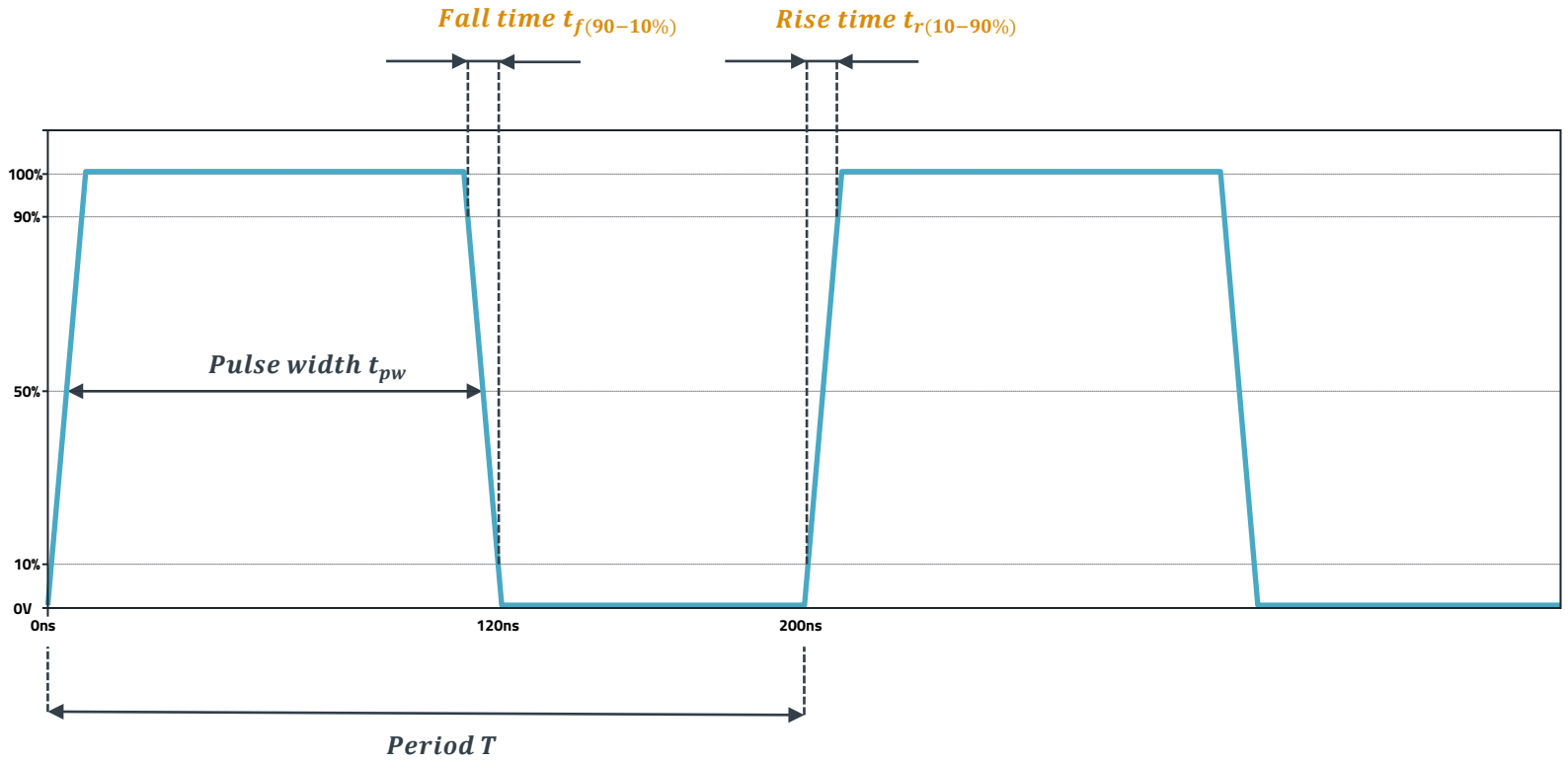
AGENDA

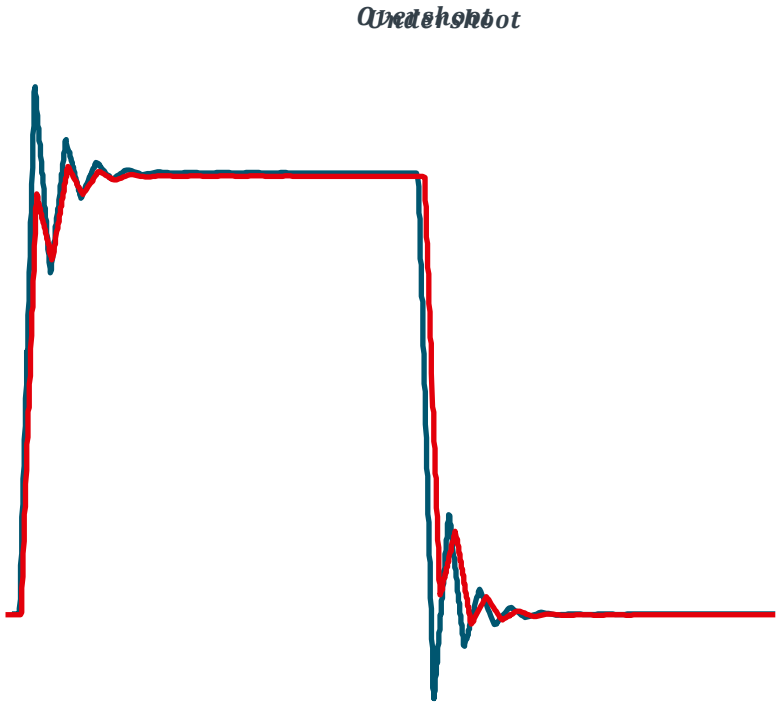
- Introduction
- Electronic circuits
- Transmission line
- Coupling effects
- Layout concepts
- Signal integrity
- Filtering
- Shielding

DIGITAL SIGNALS

Square wave

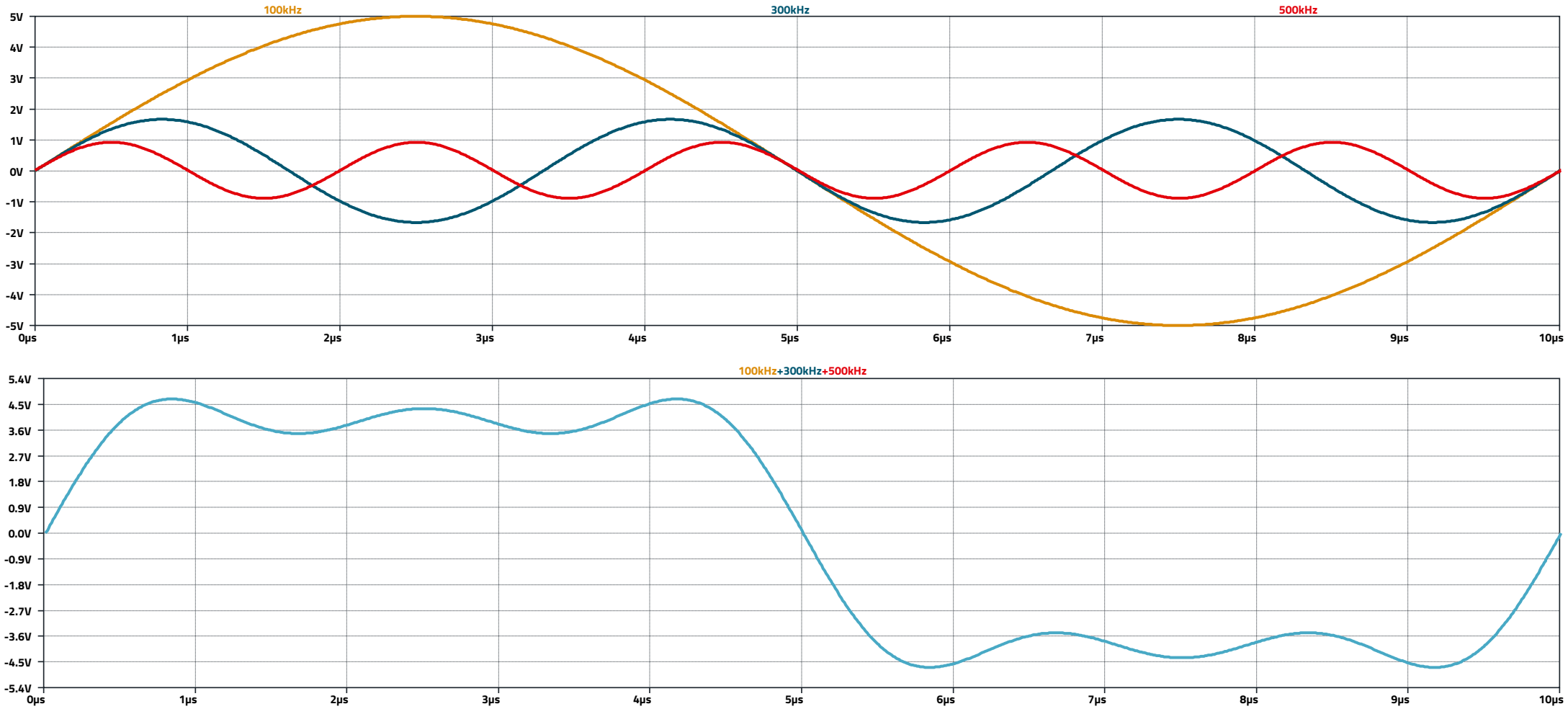
Time domain





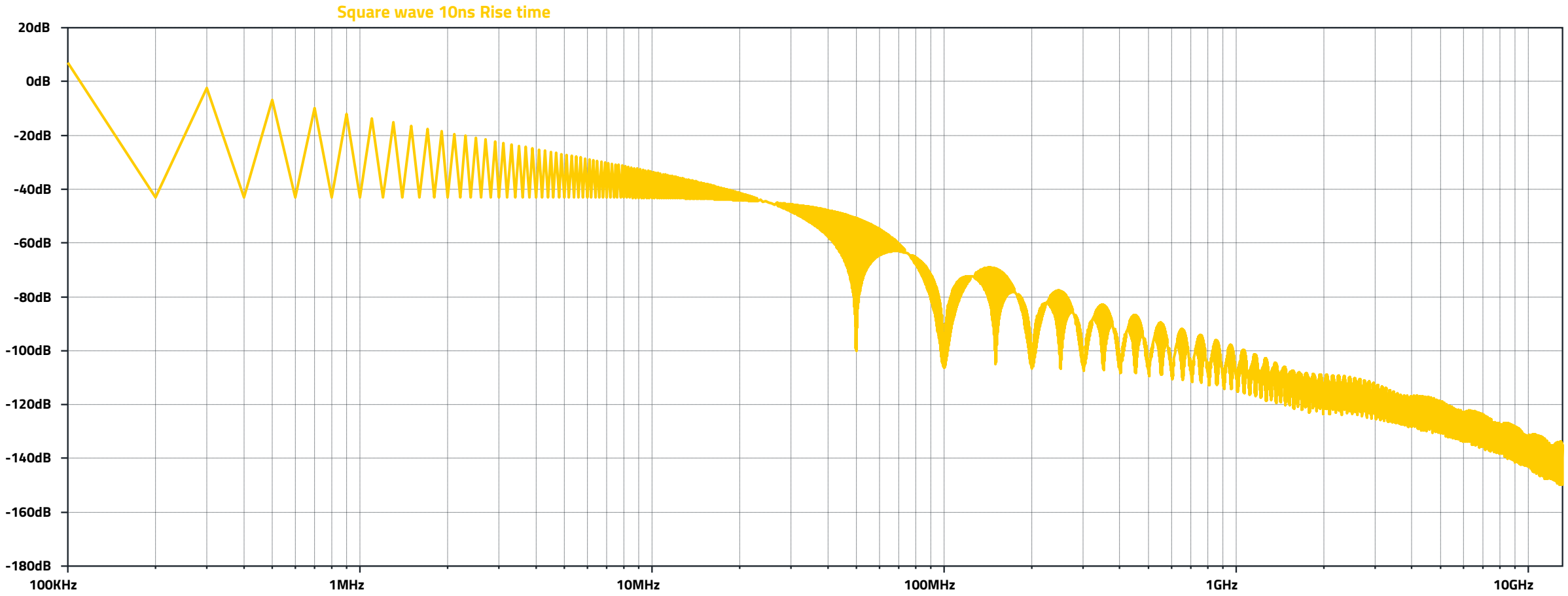
DIGITAL SIGNALS

Square wave - Fundamental wave and its odd harmonics



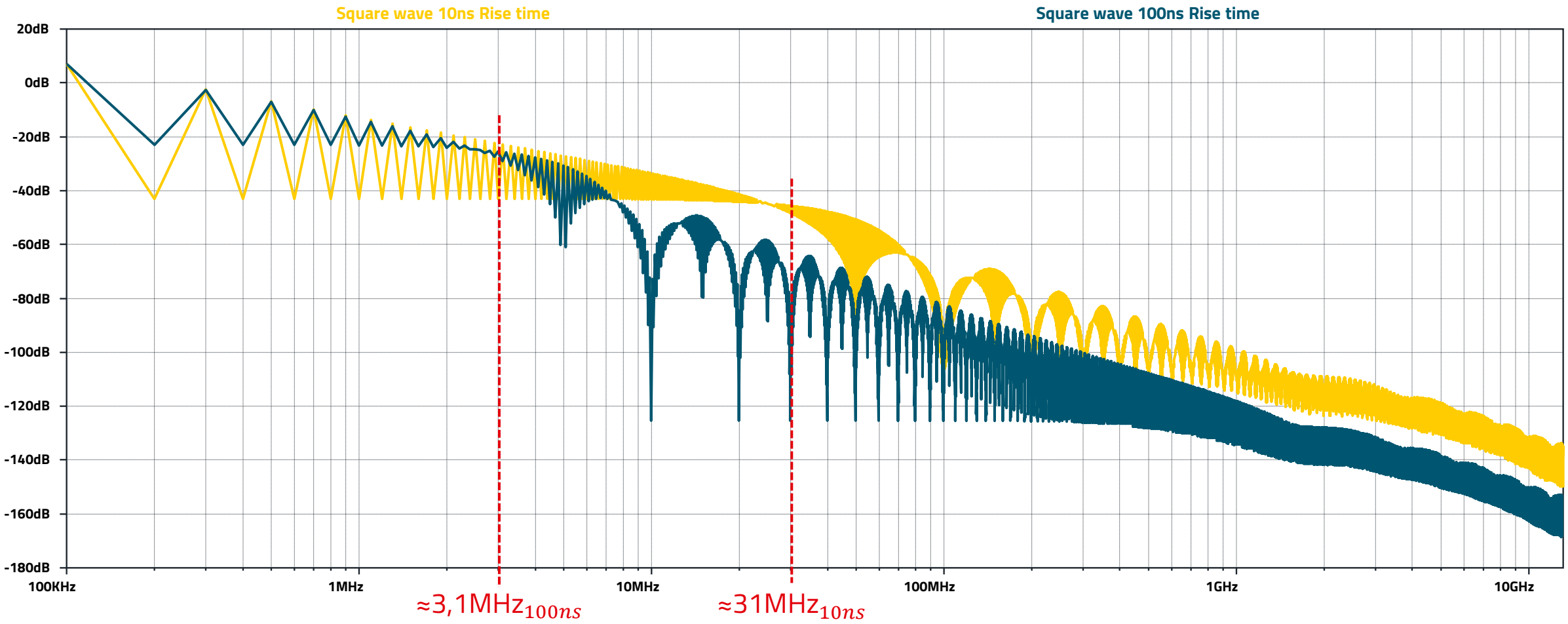
DIGITAL SIGNALS

Square wave



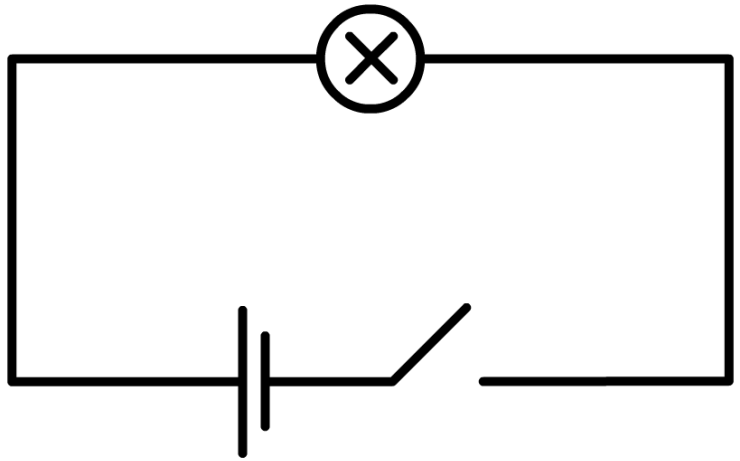
DIGITAL SIGNALS

Square wave



ELECTRONIC CIRCUIT

Simple circuit



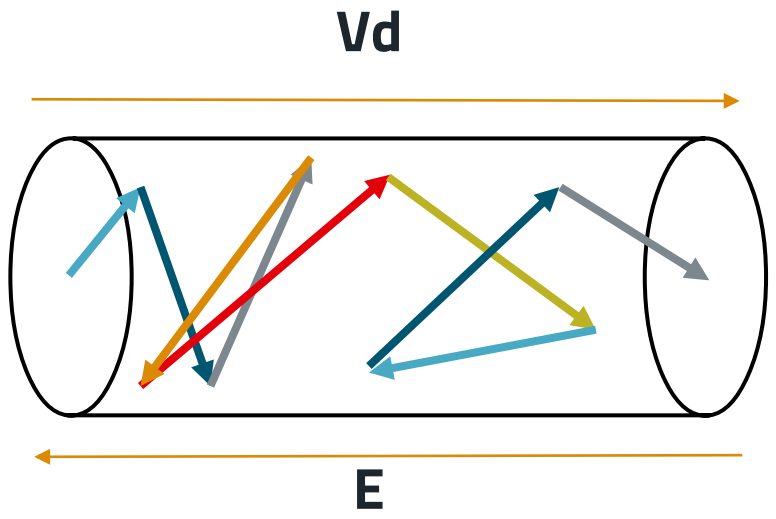
ELECTRONIC CIRCUIT

Drift velocity of an electron

$$V_d = \frac{I}{nAe}$$

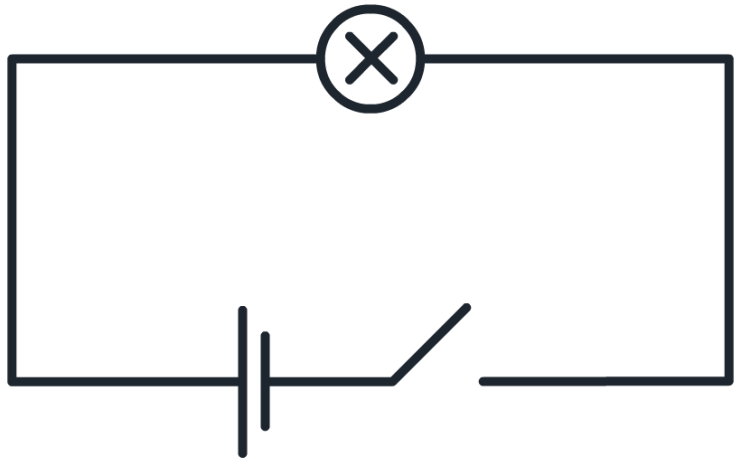
- I Electric current
- n Number of charge carriers per unit volume
- A Cross-sectional area of the conductor
- e Elementary charge $1{,}6 * 10^{-19} C$

- **5A through a copper wire ($\mathbf{n = 8,5 * 10^{28}}$) with a cross section of 1mm² would result in a drift velocity of 0,37mm/s**



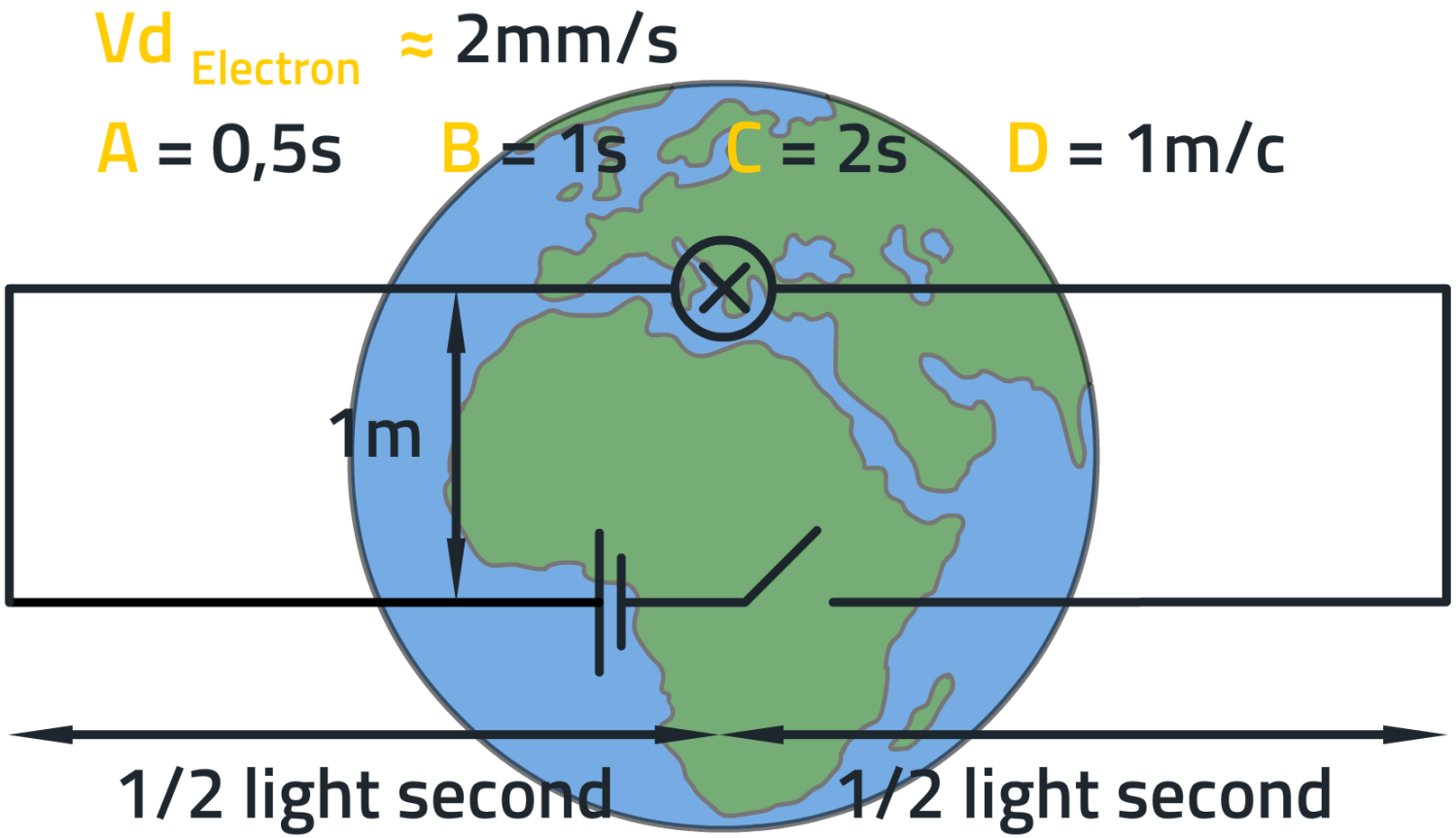
ELECTRONIC CIRCUIT

Thought experiment

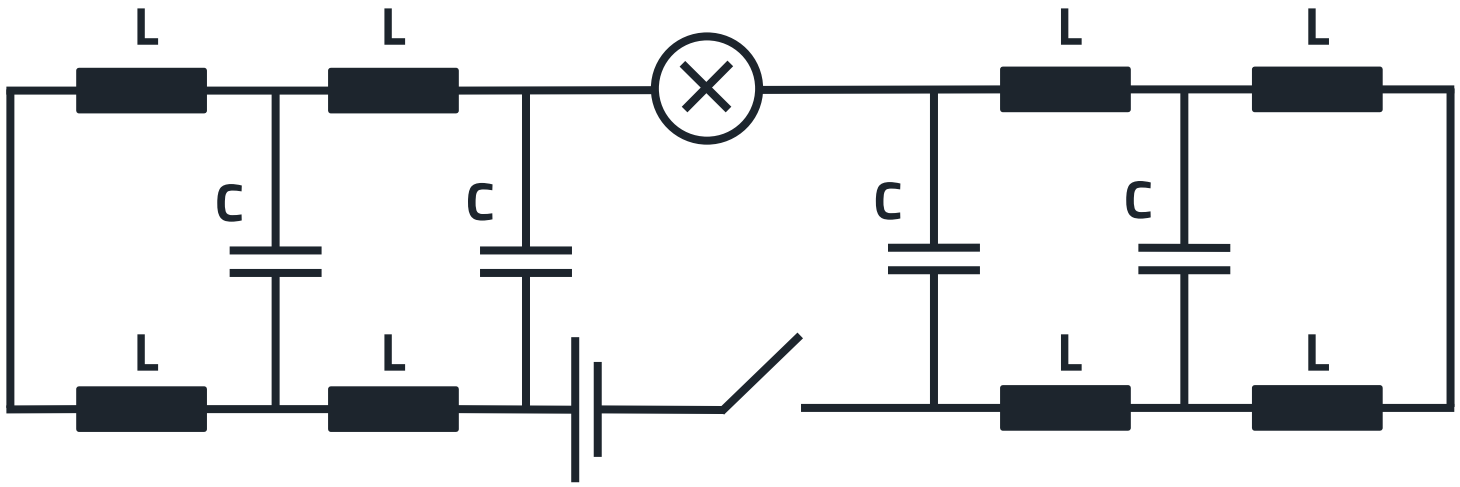


ELECTRONIC CIRCUIT

Thought experiment



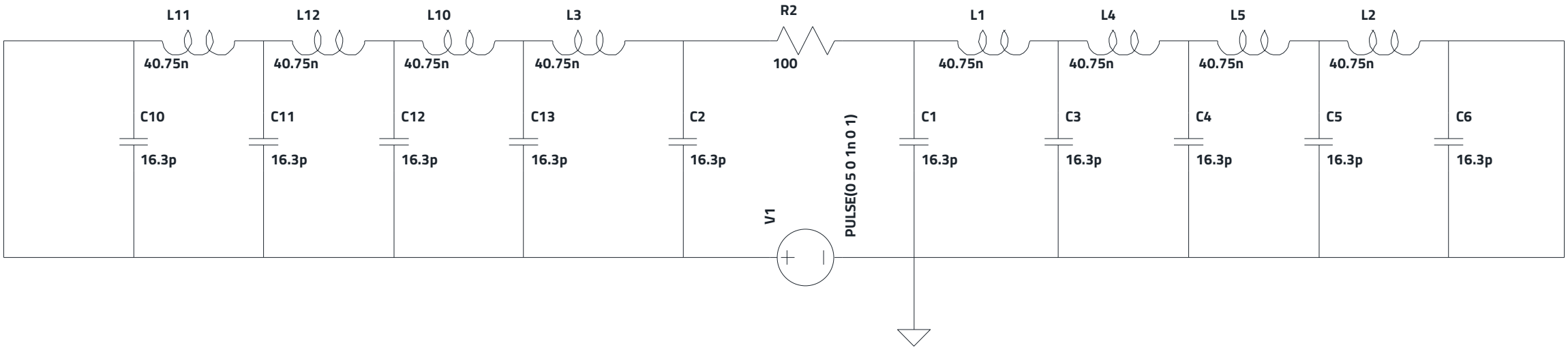
TRANSMISSION LINE



TRANSMISSION LINE

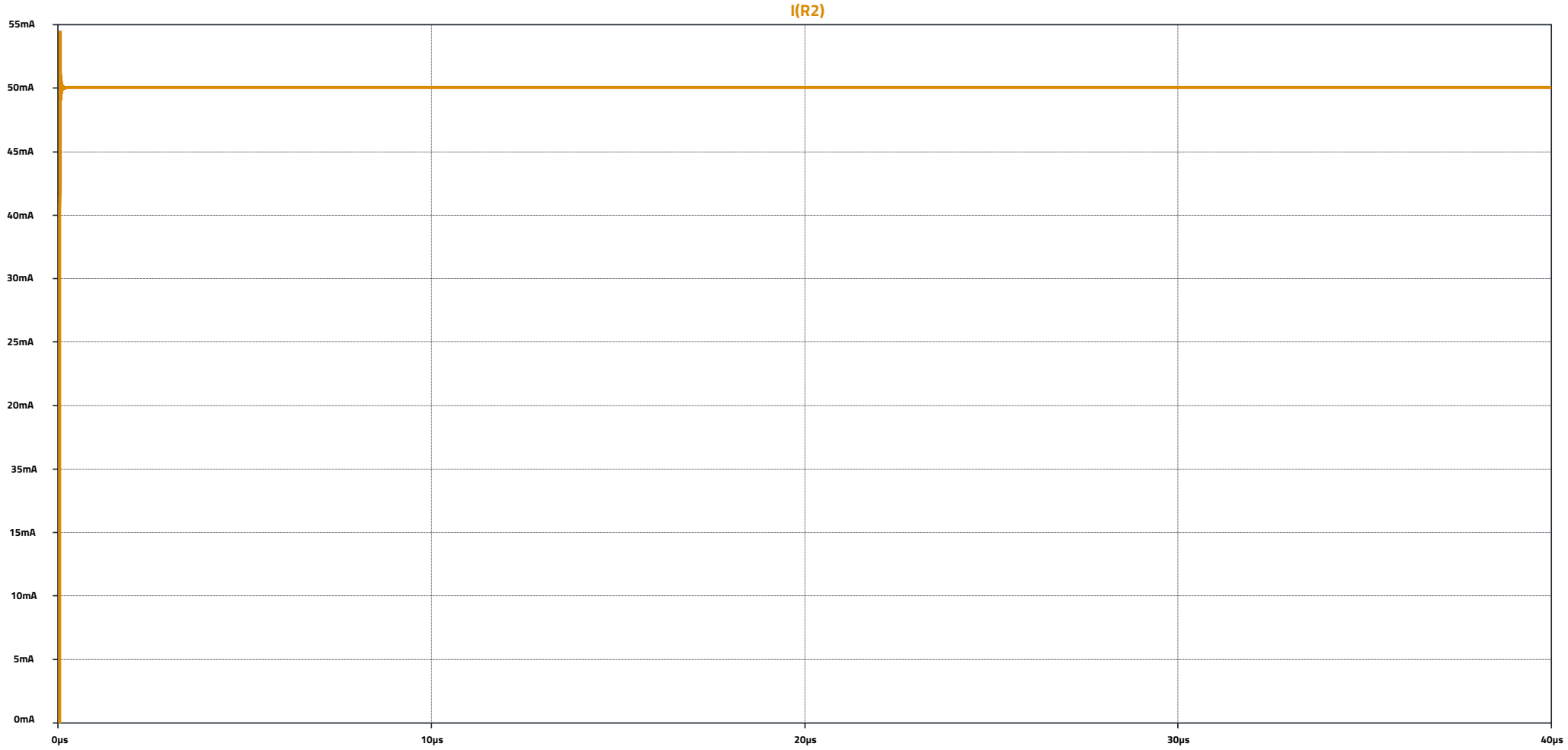
Thought experiment simulation with LT Spice

Thought experiment



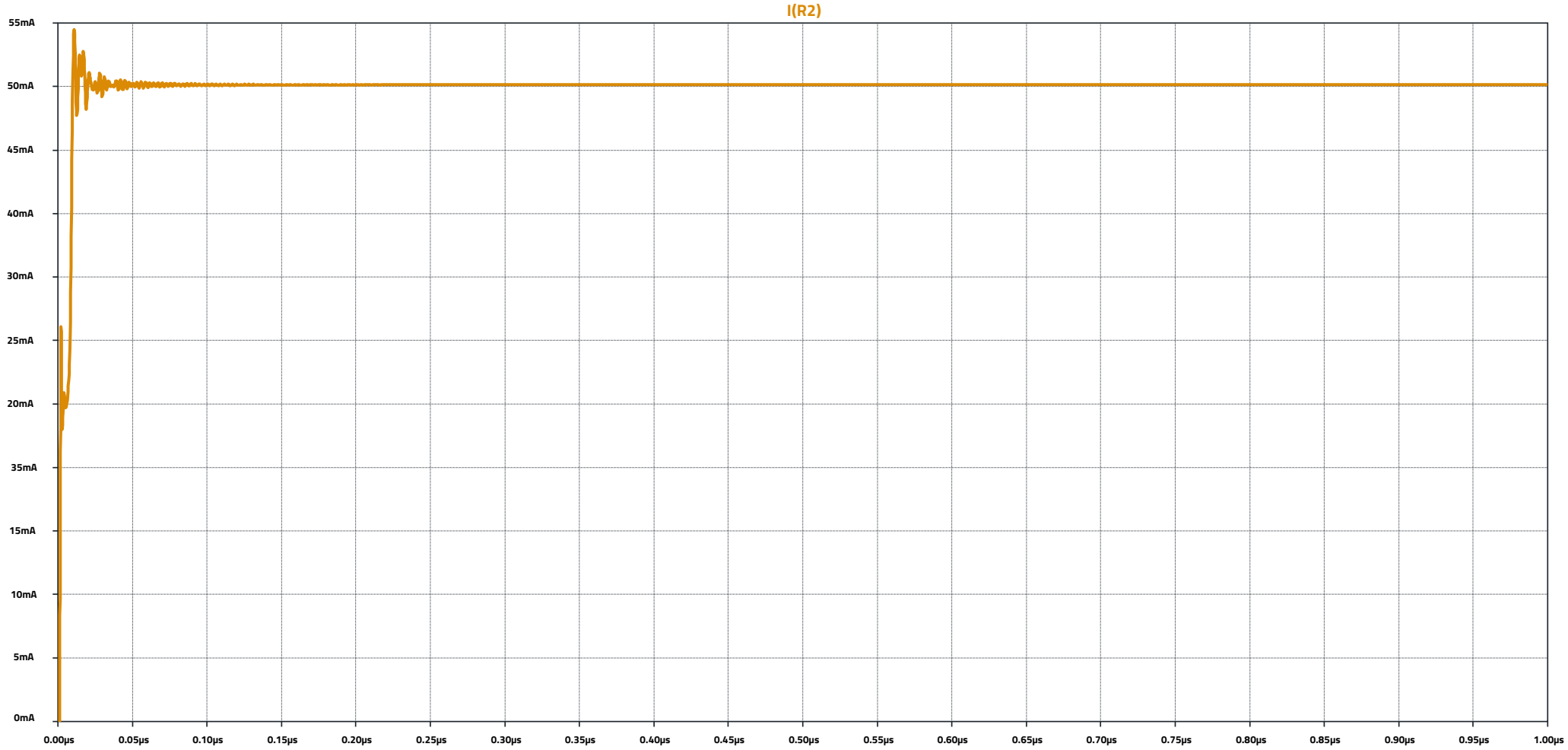
TRANSMISSION LINE

Thought experiment simulation with LT Spice



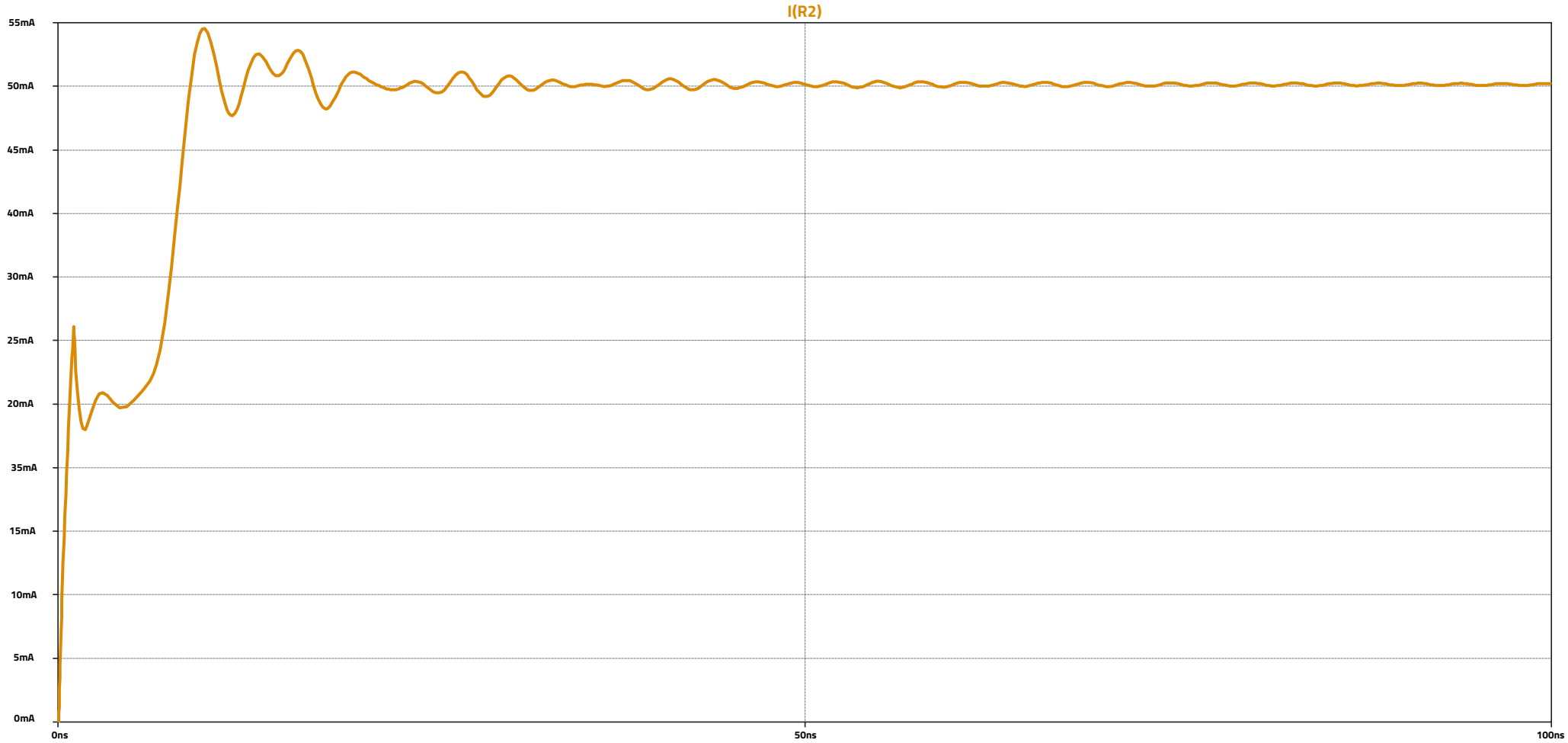
TRANSMISSION LINE

Thought experiment simulation with LT Spice



TRANSMISSION LINE

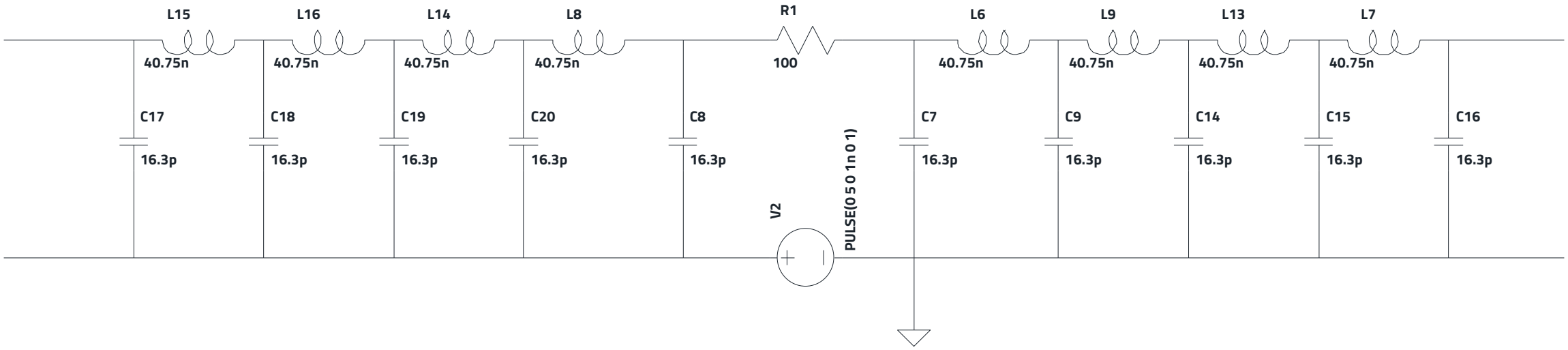
Thought experiment simulation with LT Spice



TRANSMISSION LINE

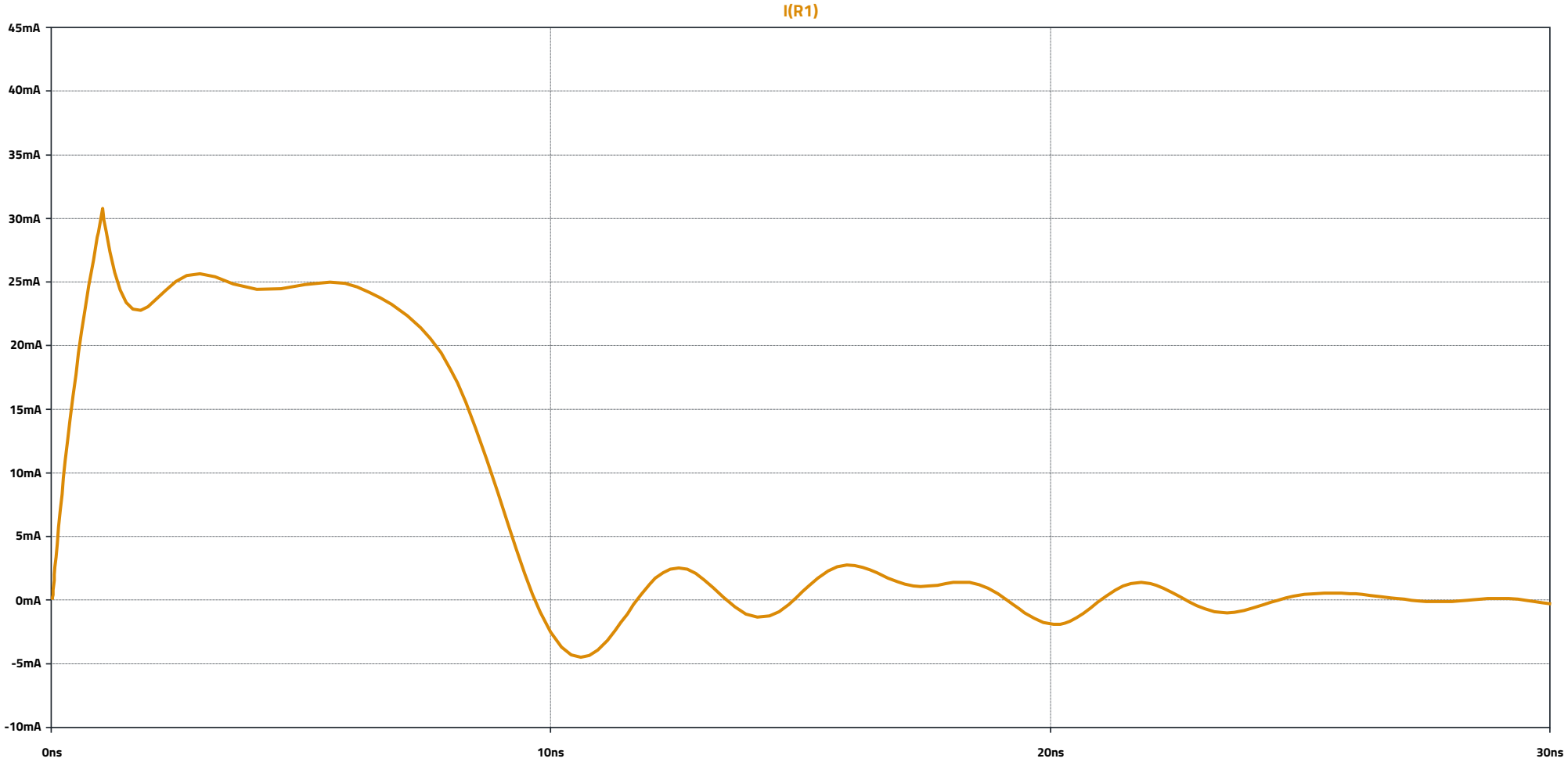
Thought experiment with open ends simulation with LT Spice

Thought experiment - where the conductor is not even connected



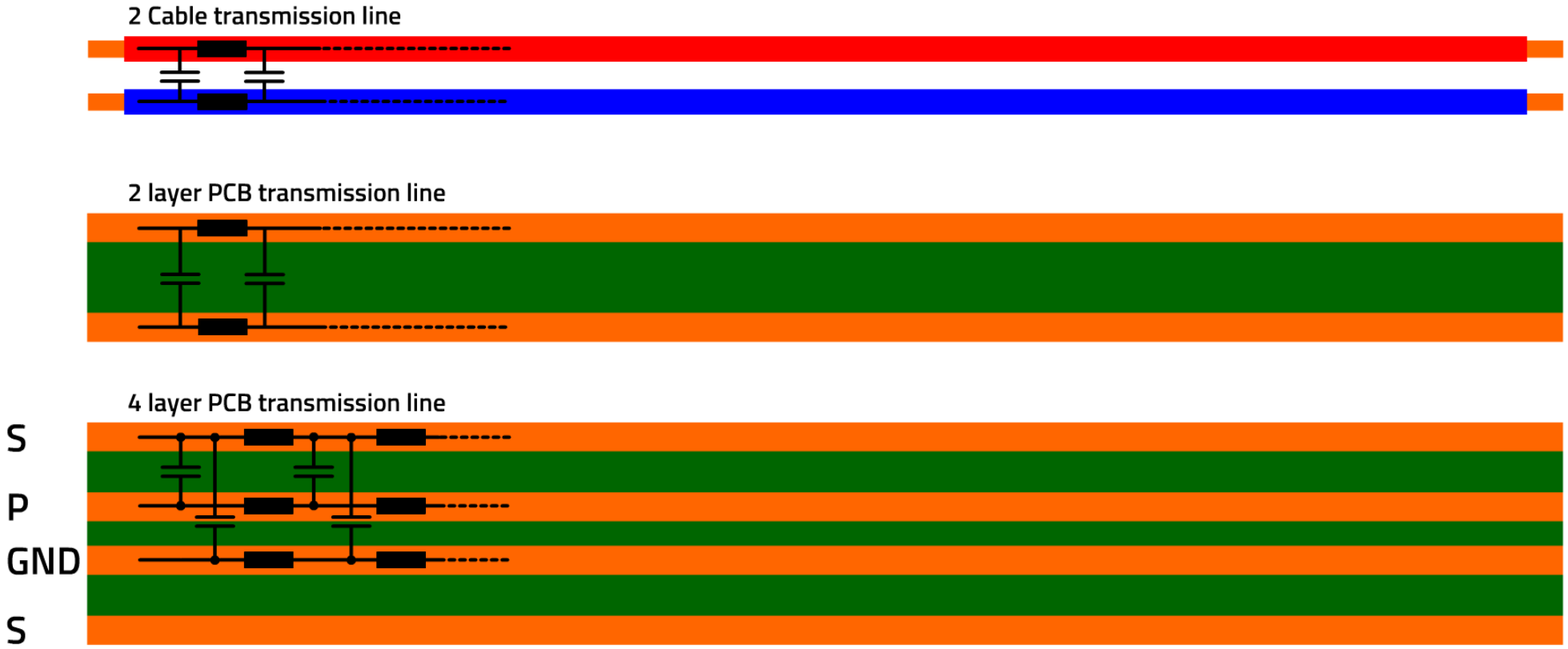
TRANSMISSION LINE

Thought experiment with open ends simulation with LT Spice



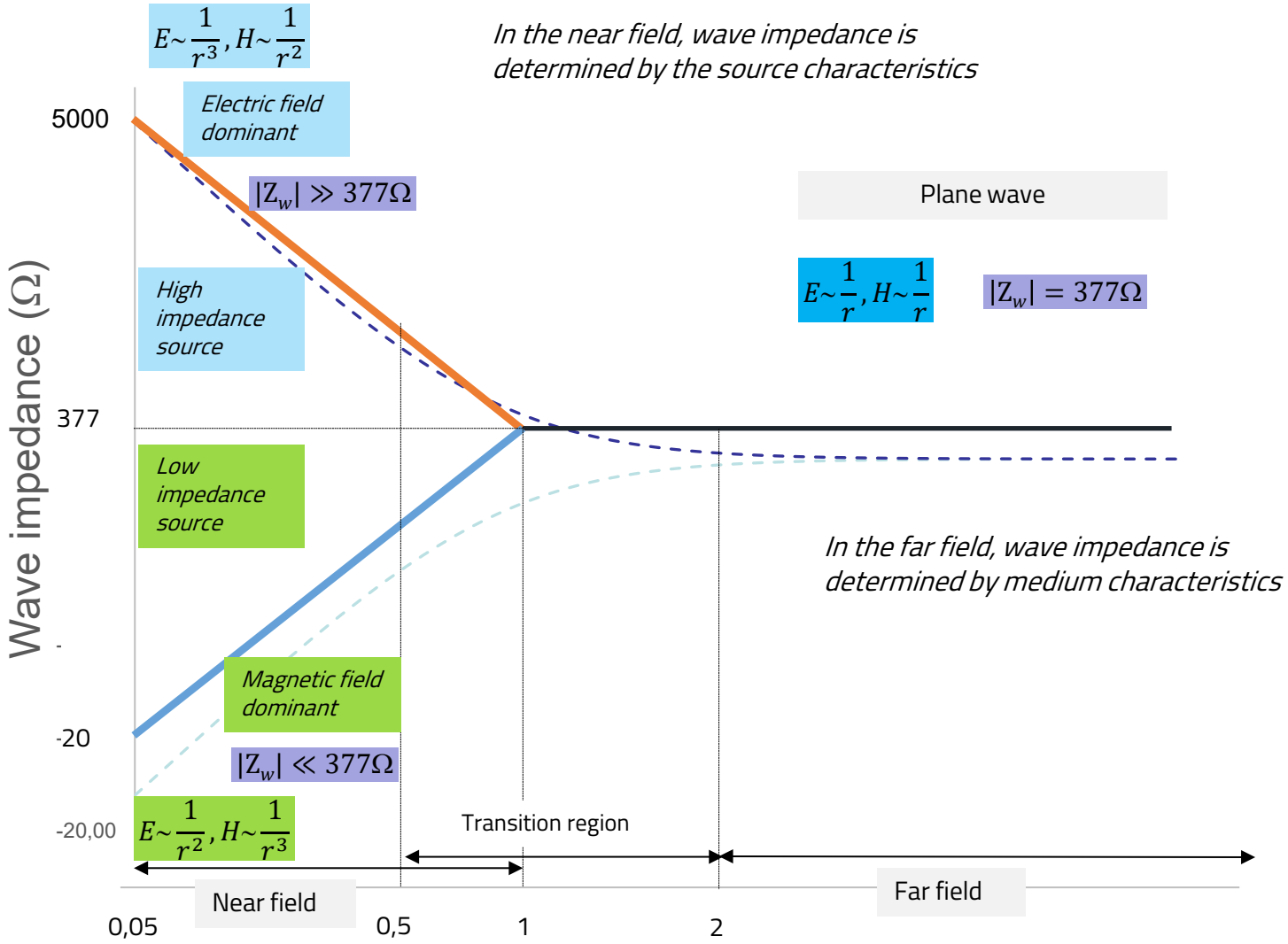
TRANSMISSION LINE

Transmission lines overview



COUPLING EFFECTS

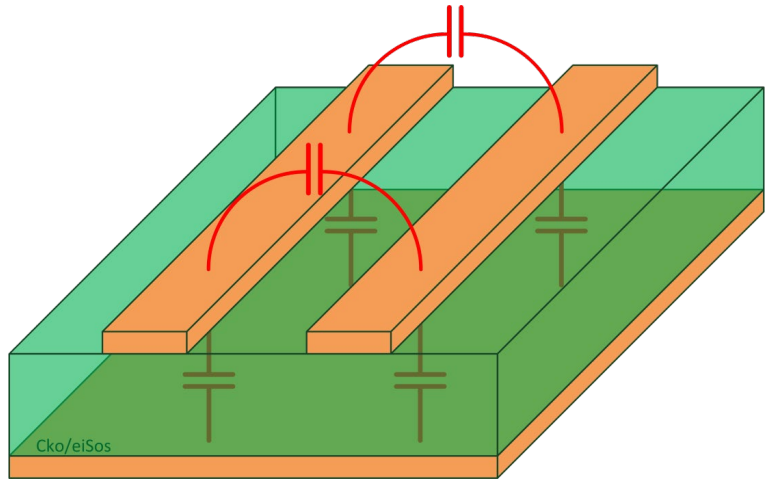
NEAR FIELD – FAR FIELD



COUPLING EFFECTS

Origin of capacitive coupling

- Originates from high dU/dt
- Parallel conductors form a parasitic capacitance
- Coupling capacitance is directly proportional to the length of the parallel trace run

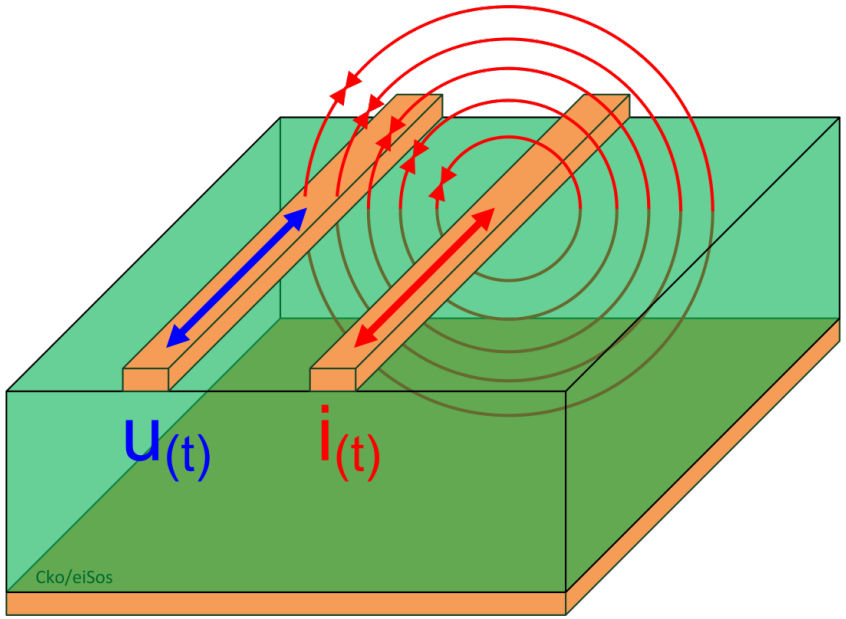


Isolating Components	typ. Coupling Capacitance
Optocoupler	1 ~ 5pF
Solid State Relay	5 ~ 10pF
Electromechanical Relay	10 ~ 100pF
Transformers in SMPS	Up to 1000 pF

COUPLING EFFECTS

Origin of inductive coupling

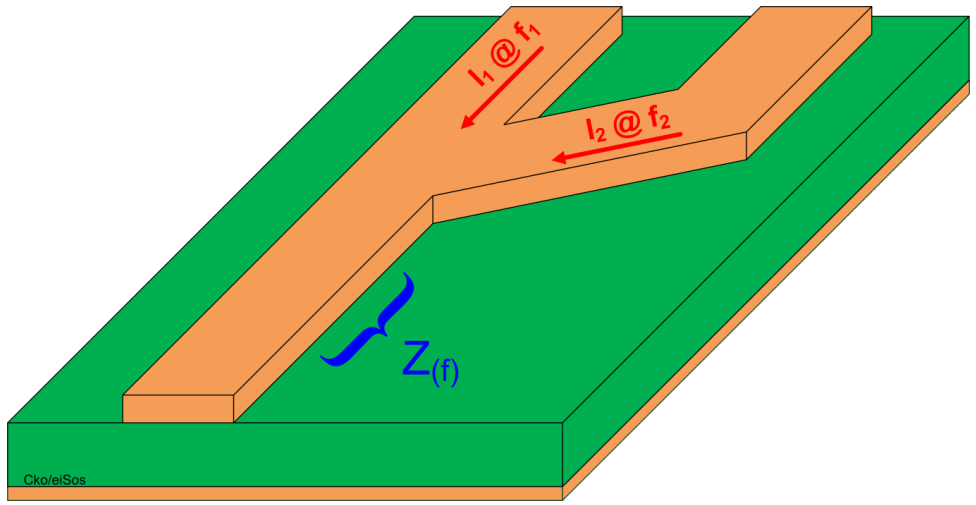
- Originates from high dI/dt
- Parallel traces form a parasitic transformer
- Mutual inductance increases with decreasing distance



COUPLING EFFECTS

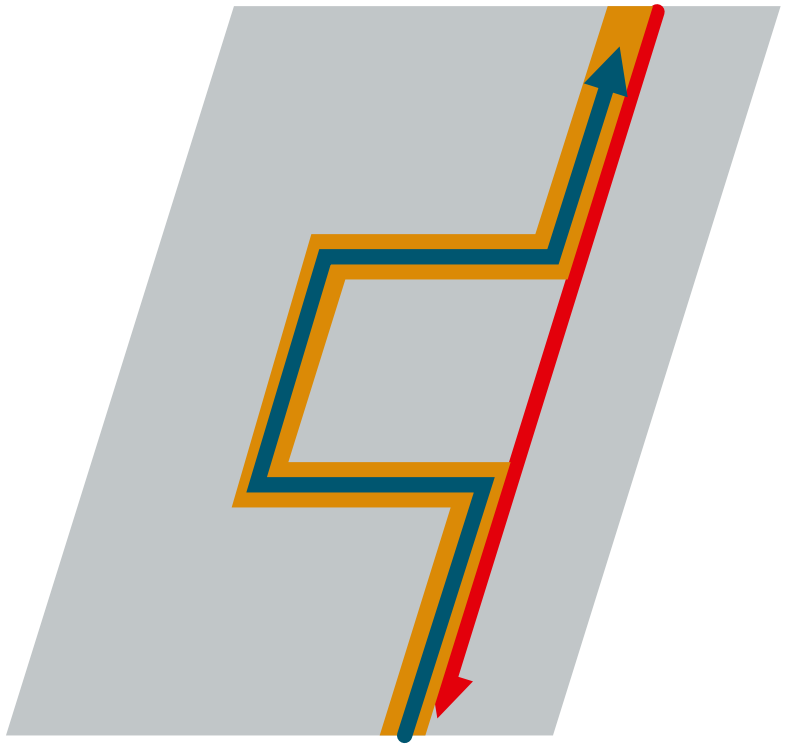
Origins of impedance/galvanic coupling

- Interference affects circuits with mutual traces
- Circuits share an impedance and therefore the voltage across that impedance
- Main cause for high mutual impedances is self-inductance across copper traces

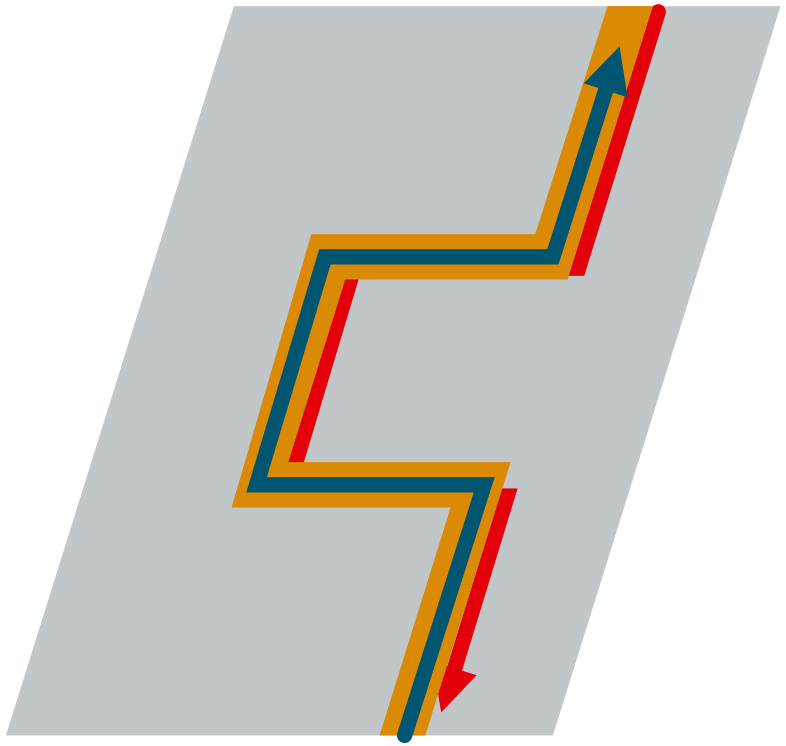


COUPLING EFFECTS

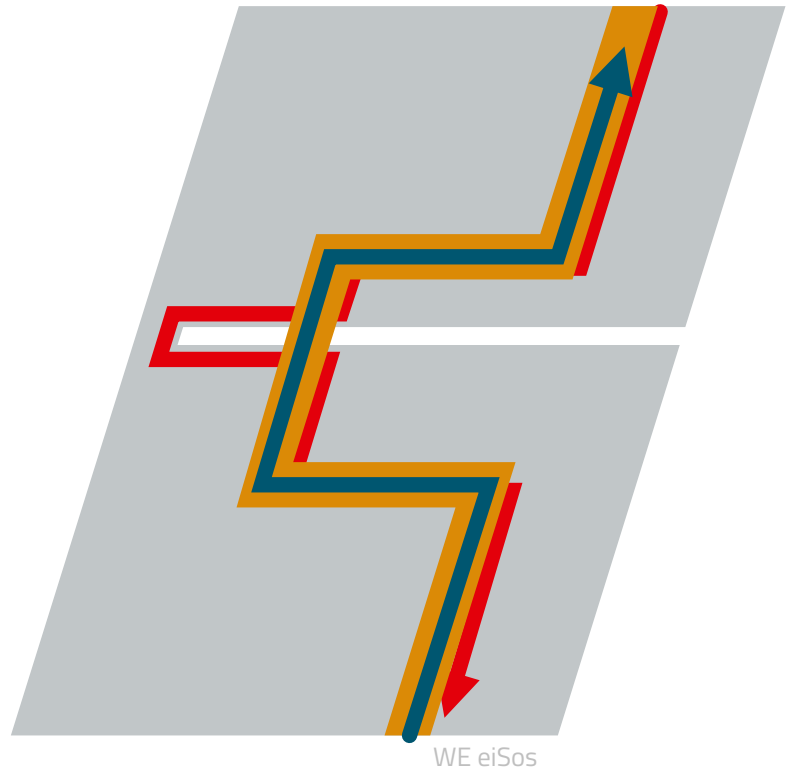
Path of least impedance



DC return path



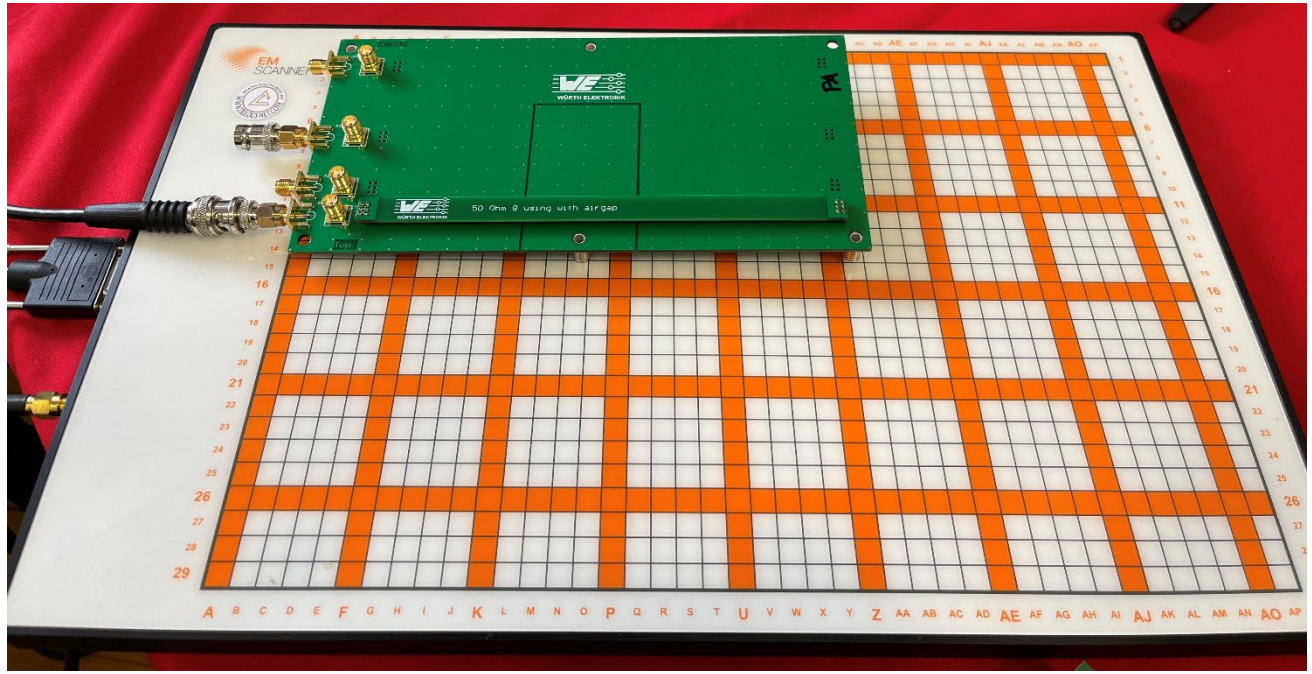
AC return path

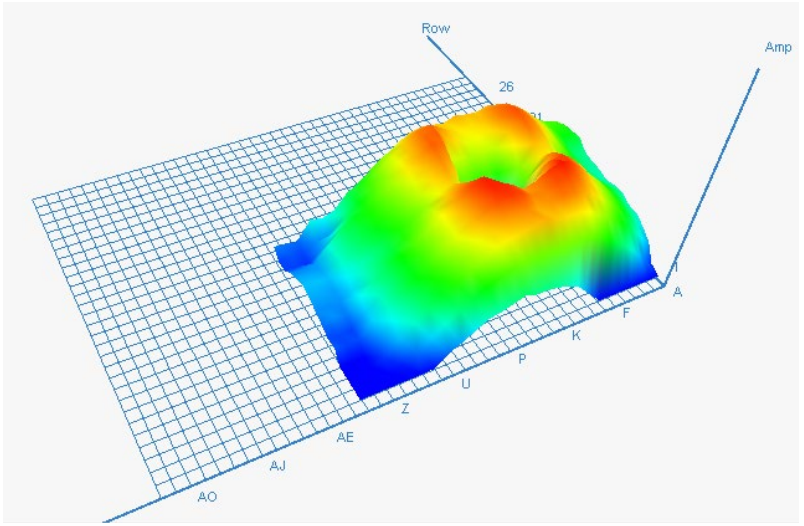


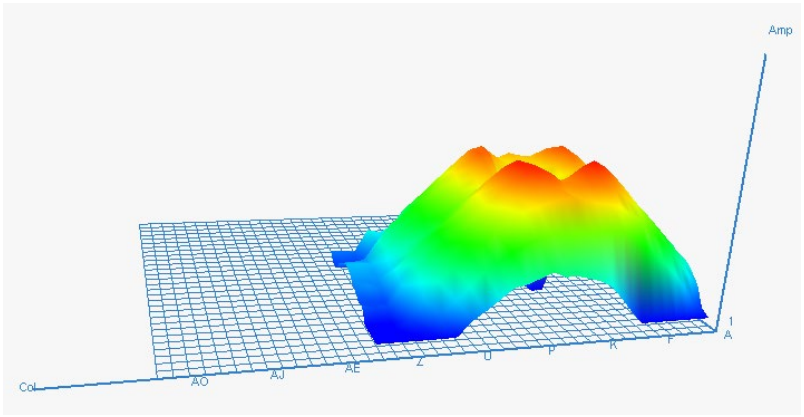
Slotted AC return path

COUPLING EFFECTS

Near field measurement

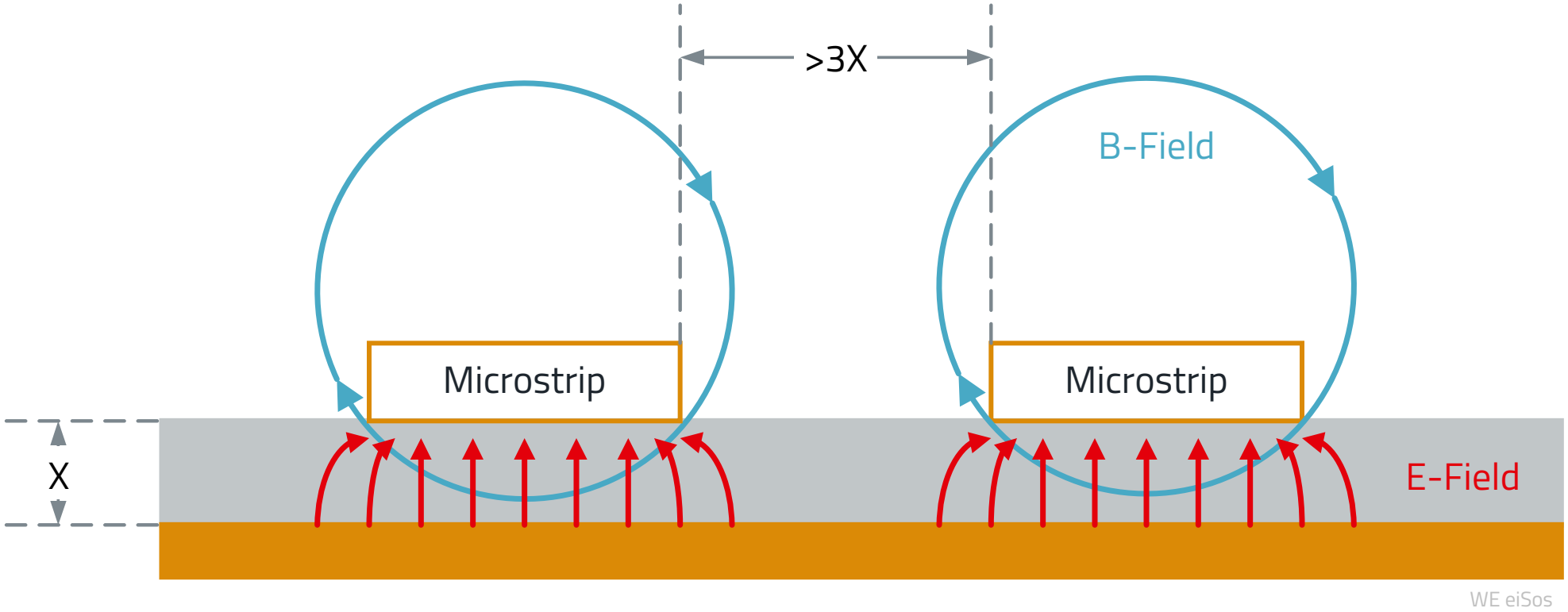






COUPLING EFFECTS

Minimizing Crosstalk - Increase distance between traces



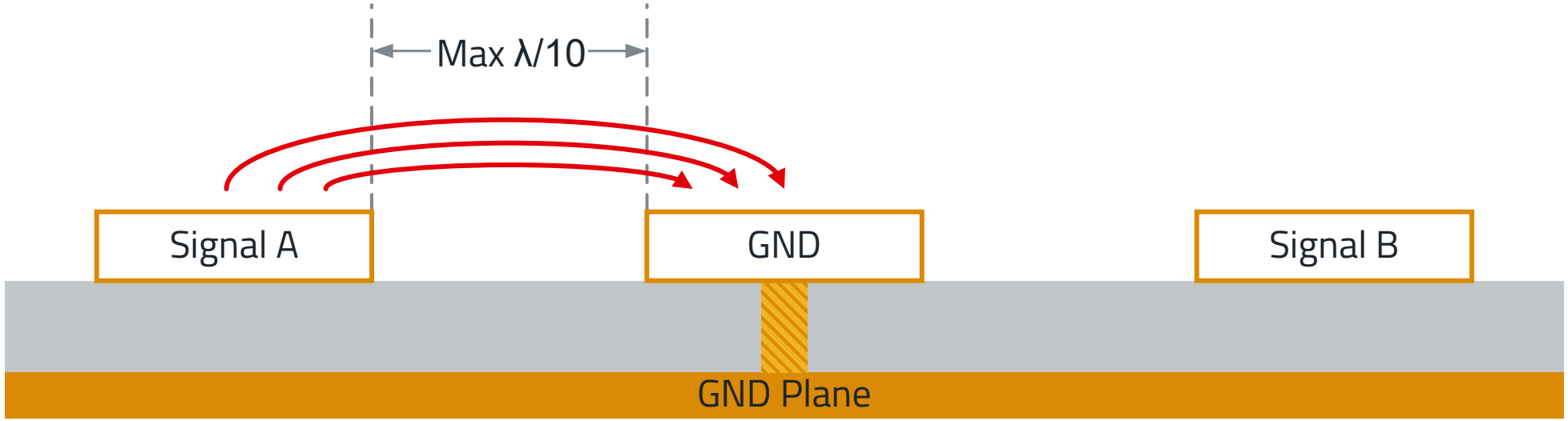
Crosstalk can be reduced to 1% by placing Strip Lines at 3 times the substrate thickness apart

COUPLING EFFECTS

Minimizing Crosstalk - GND fence

- Inserting a copper area that is tightly bound to GND
  - Shielding the noise source

- Distance between Vias: Max. λ/10 of the highest noise frequency



WE eiSos

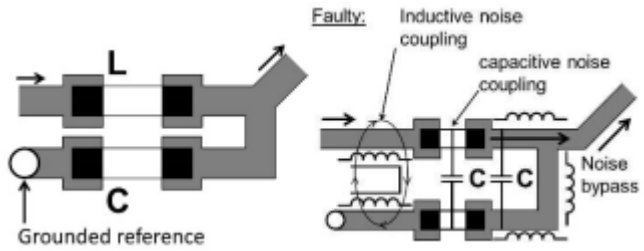
LAYOUT CONCEPTS

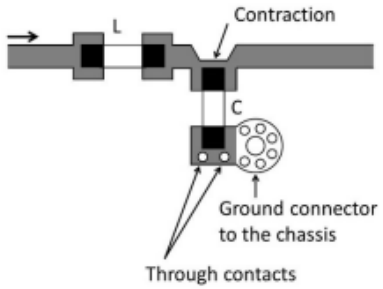
EMC

General countermeasures

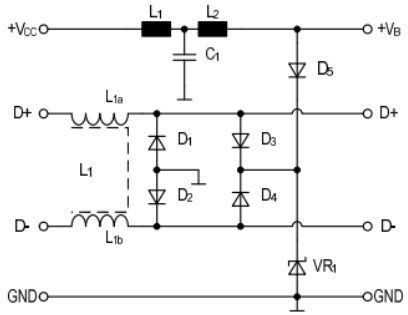
1) Improving the general layout of the circuit board and the overall construction of the device

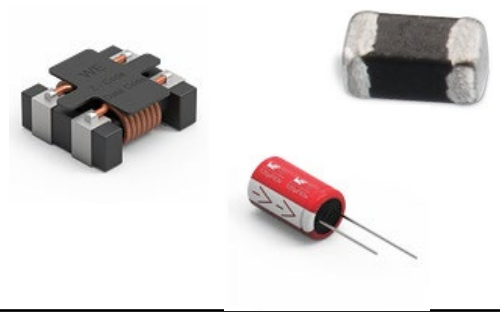
   One problem – a lot of solutions and opinions



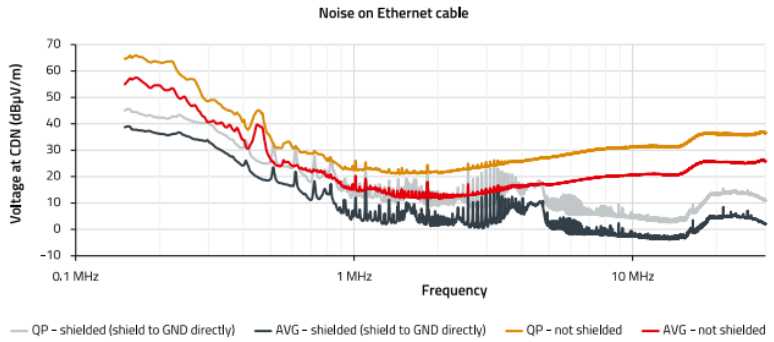


2) Filters



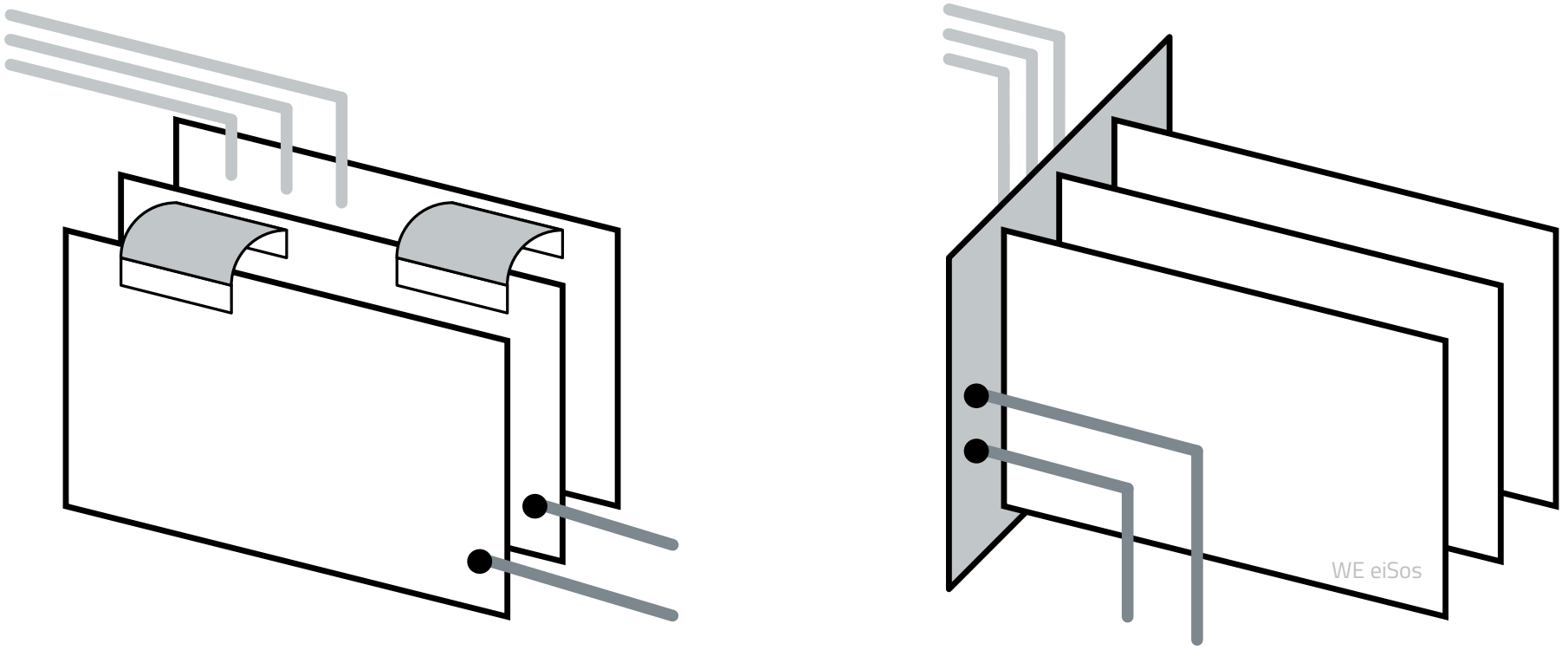


3) Shielding



LAYOUT CONCEPTS

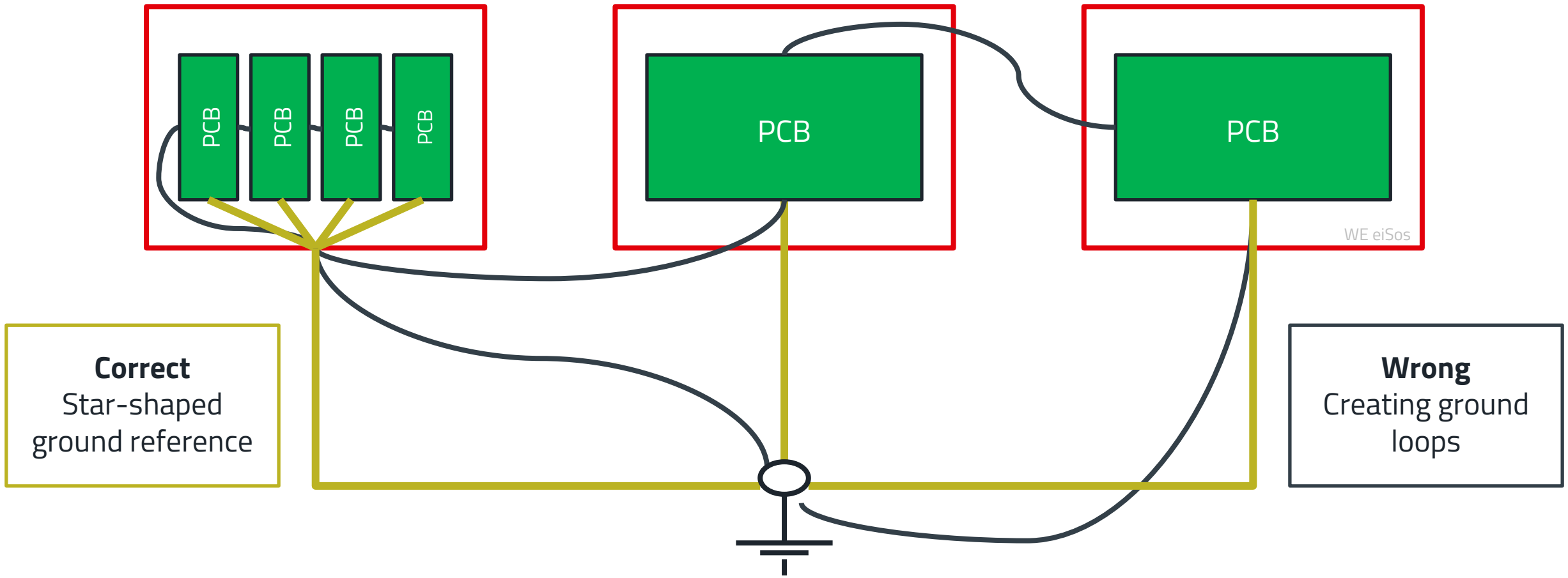
Principle of a single point grounding/multipoint grounding on system level



Susceptible to interferences (left) and a more fail-safe (right) construction of a device

GROUND CONCEPTS

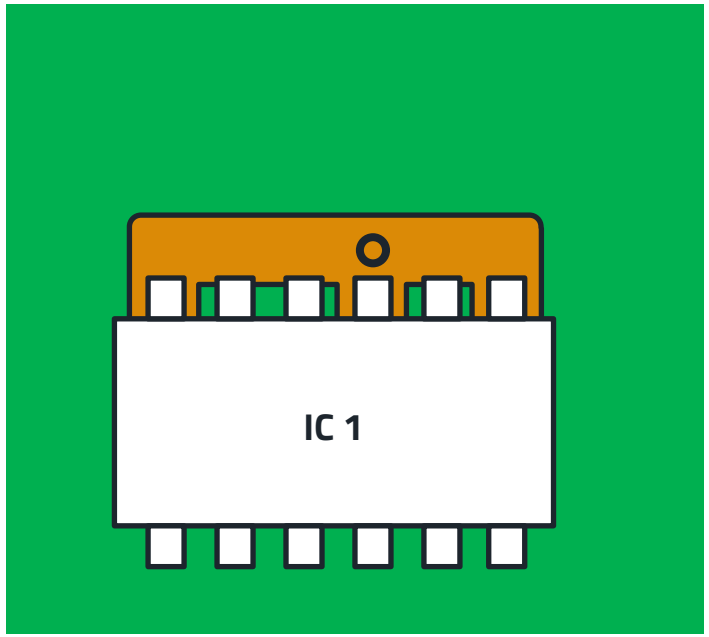
Reduce impedance coupling with a common star-shaped ground reference point



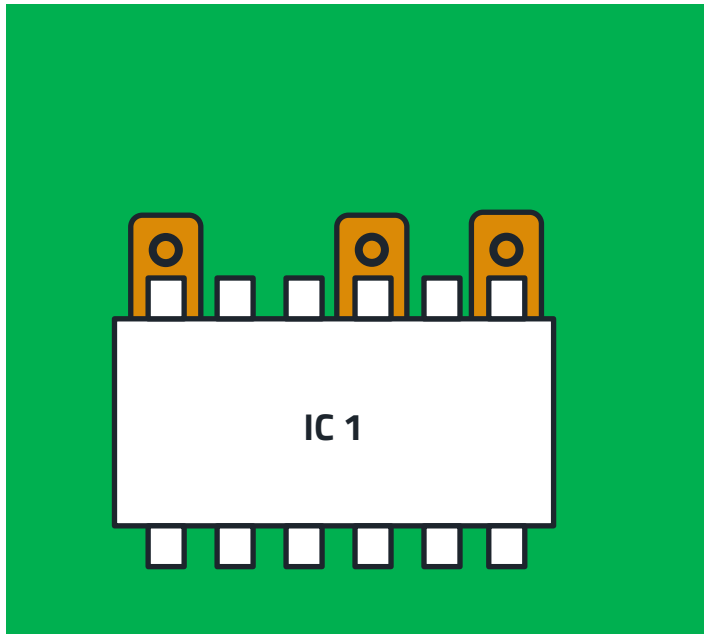
LAYOUT CONCEPTS

Low impedance connections to the GND plane(s)

High impedance connection



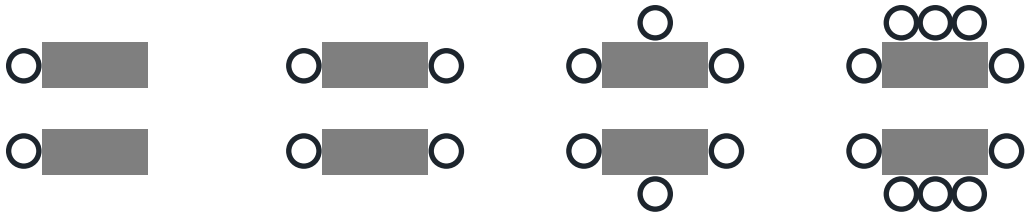
Low impedance connection

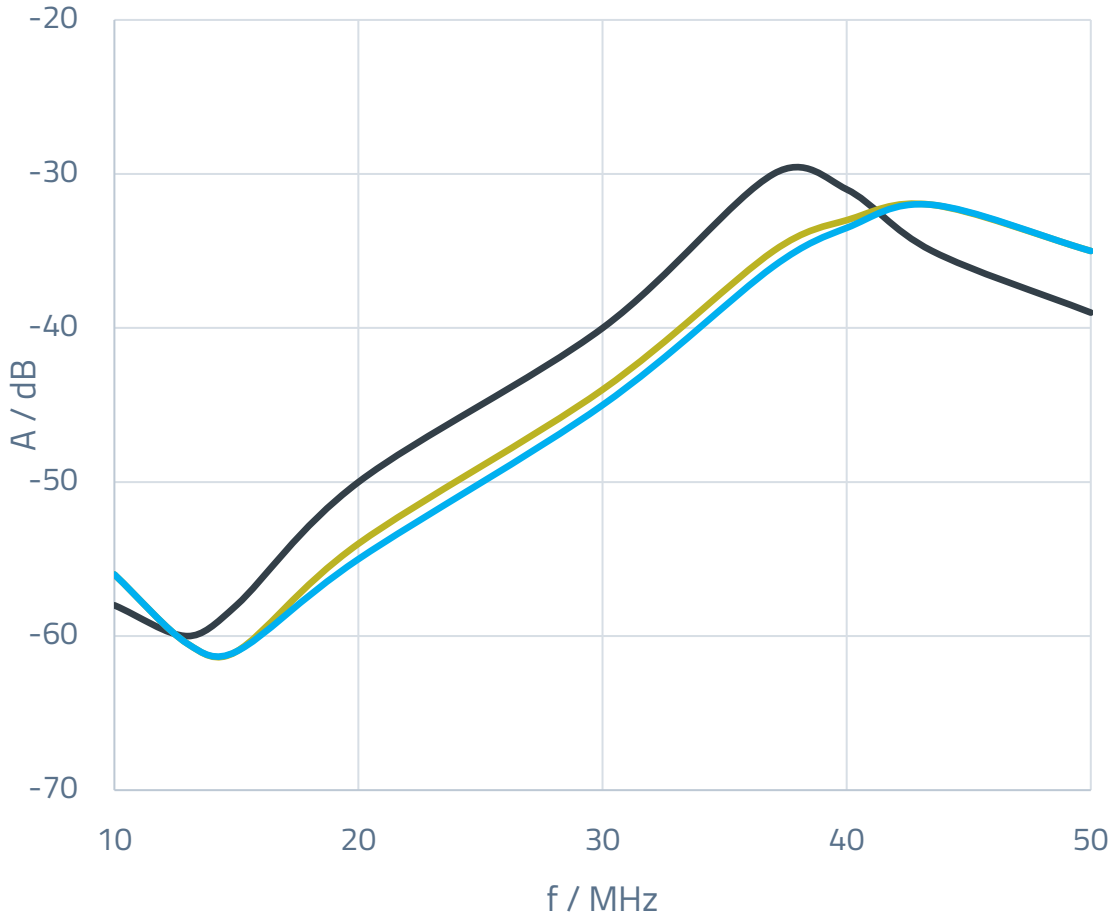


LAYOUT CONCEPTS

Simulation: Attenuation over frequency - Number of vias

Number	L / nH	ΔL / %
1	1,538	-
2	1,240	-19,4
3	1,176	-23,5
5	1,171	-23,9

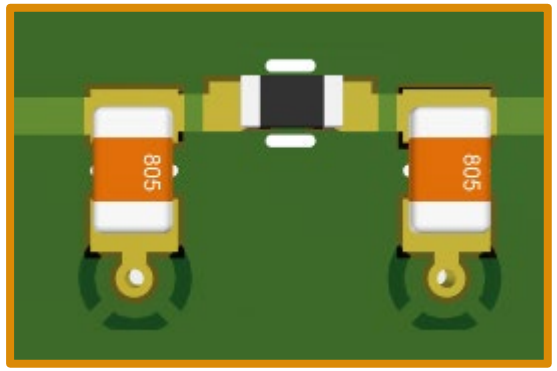




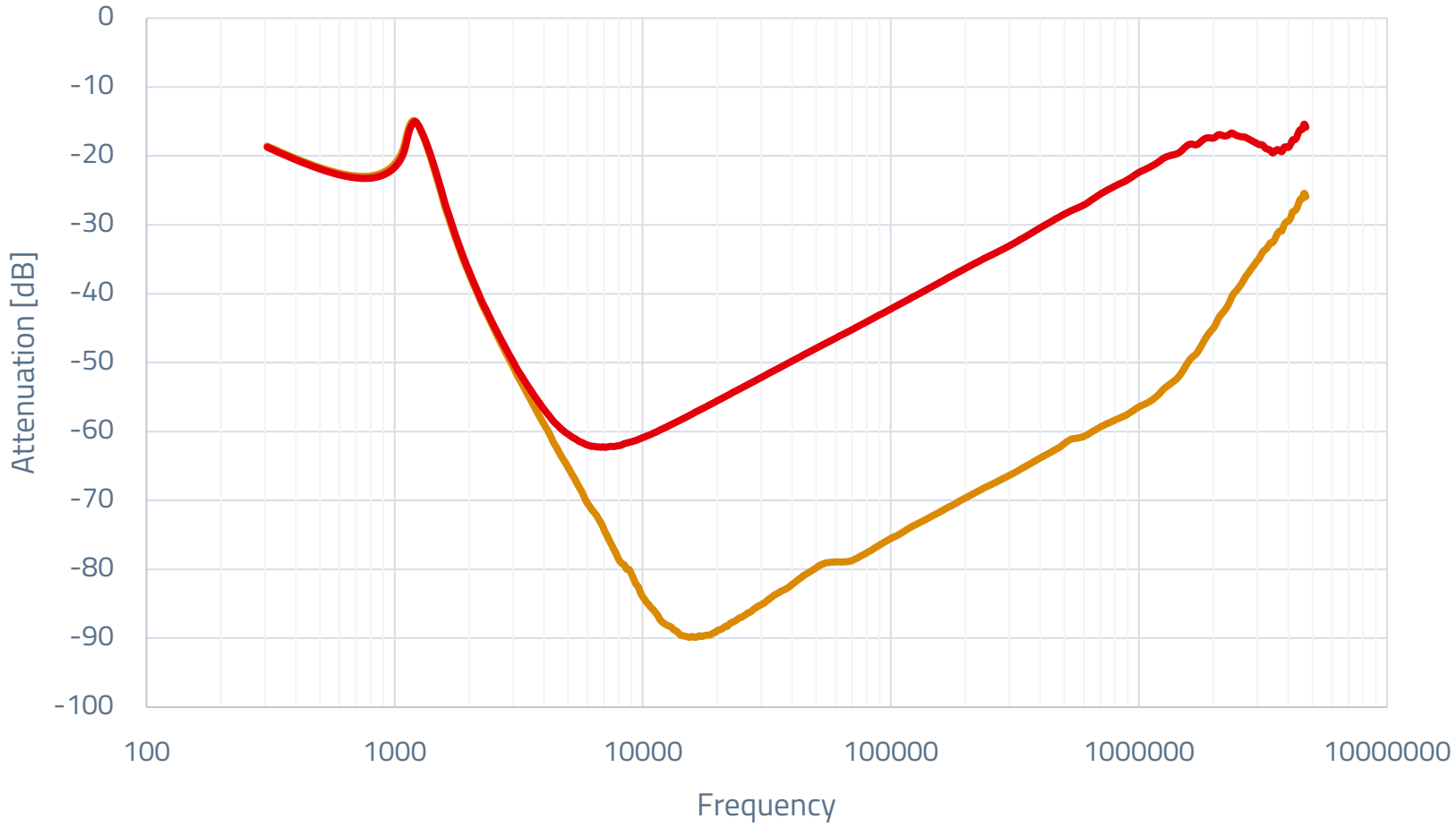
VNA MEASUREMENT S21 300KHZ – 3GHZ

Layout: Influence on the attenuation

0805, Bad layout

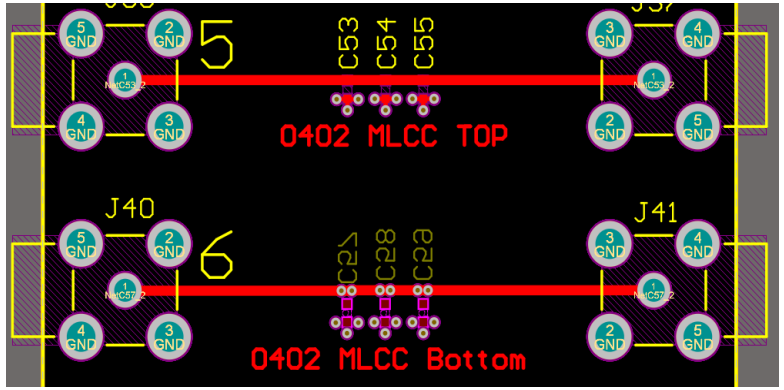


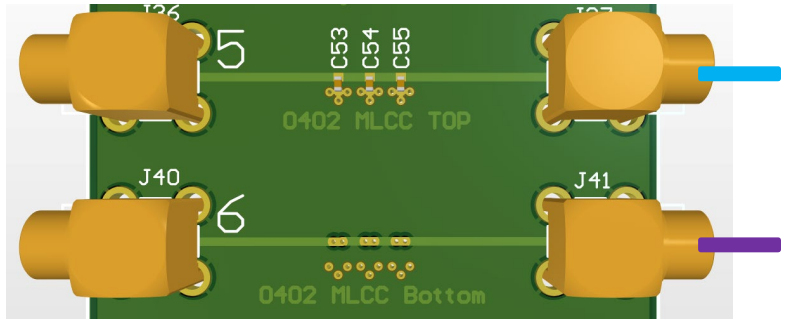
0805, Good layout

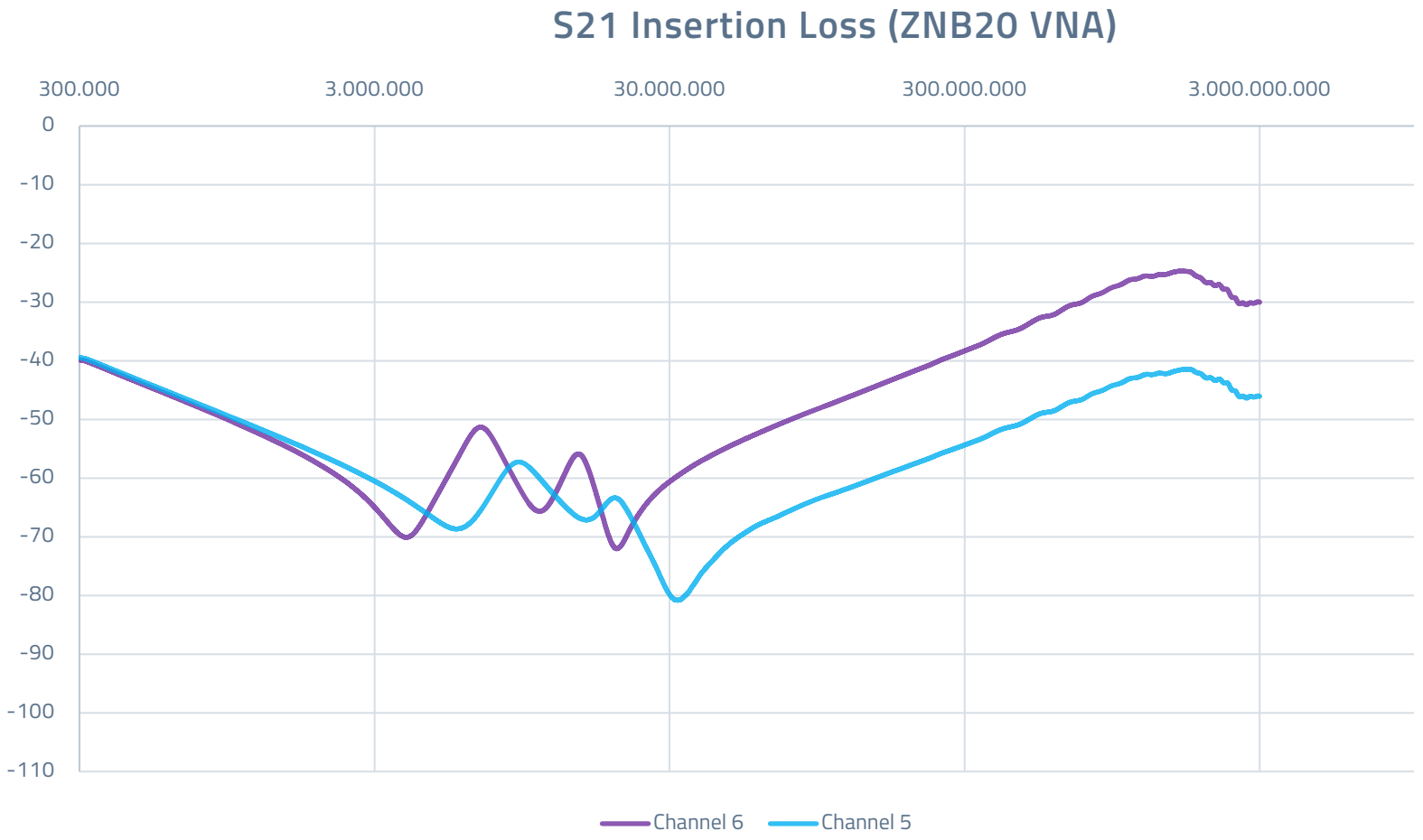


VNA MEASUREMENT S21 300KHZ – 3GHZ

Comparison: Standard vs BGA Style placing of 3xMLCCs parallel (2,2µF + 330nF + 68nF)

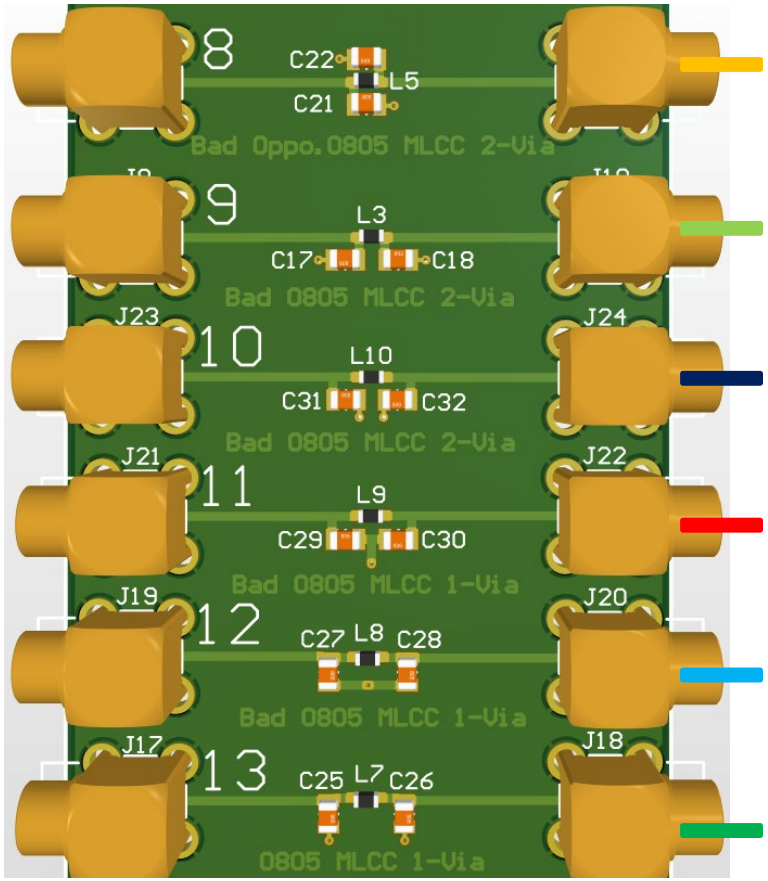


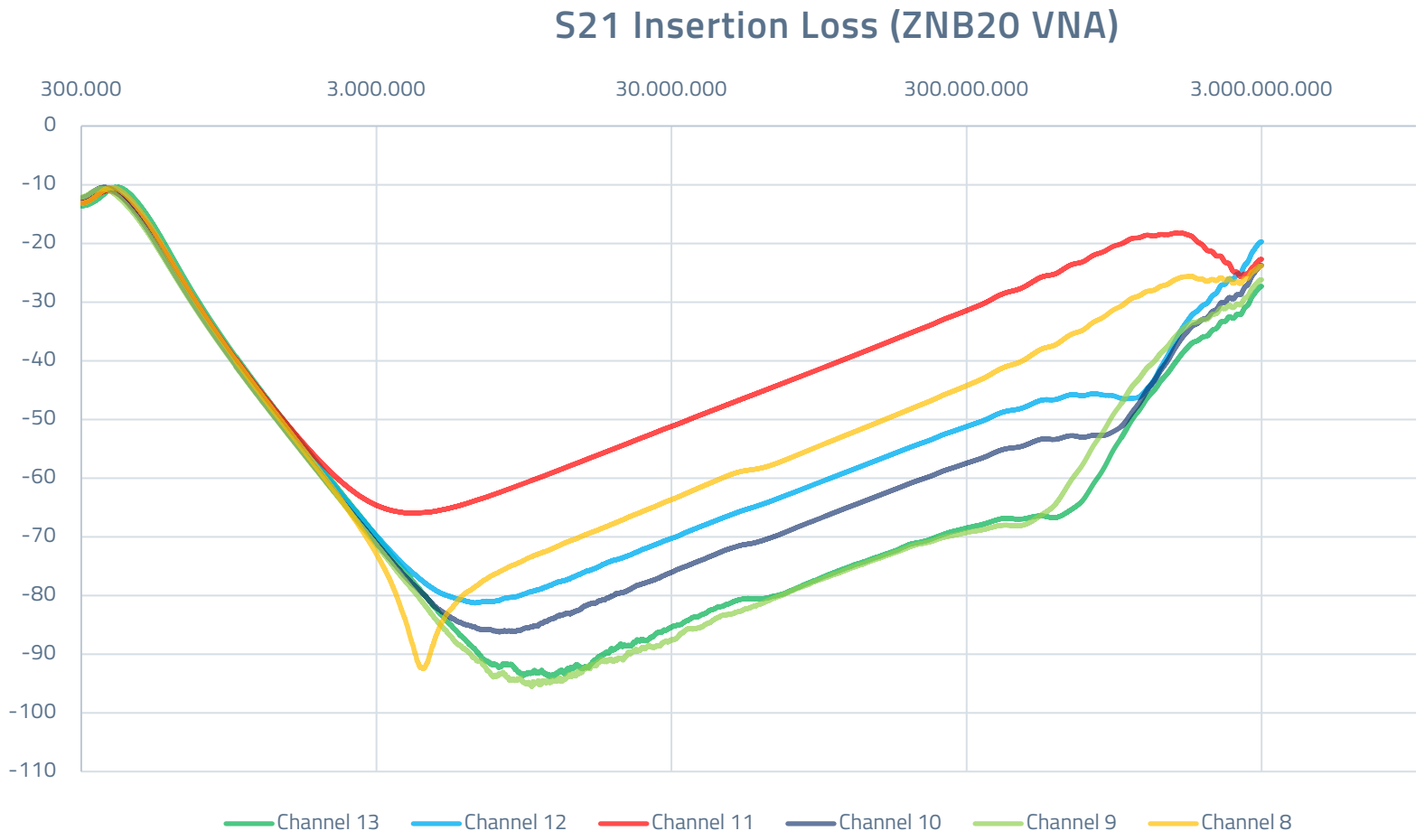




VNA MEASUREMENT S21 300KHZ – 3GHZ

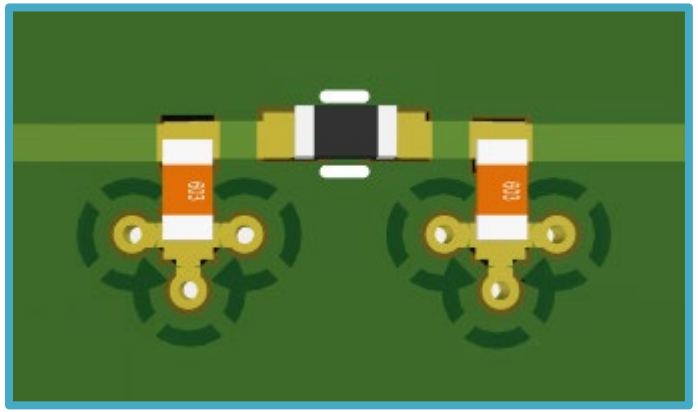
PI-Filter Layout comparison (Wideband 0603 Ferrit + 2x100nF 0805 MLCCs)



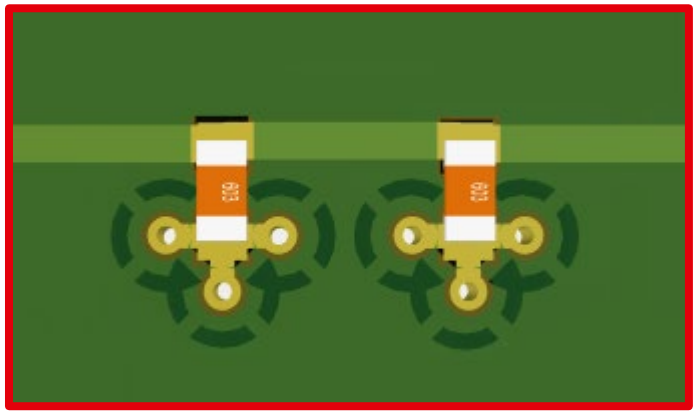


VNA MEASUREMENTS S21 300KHZ – 3GHZ

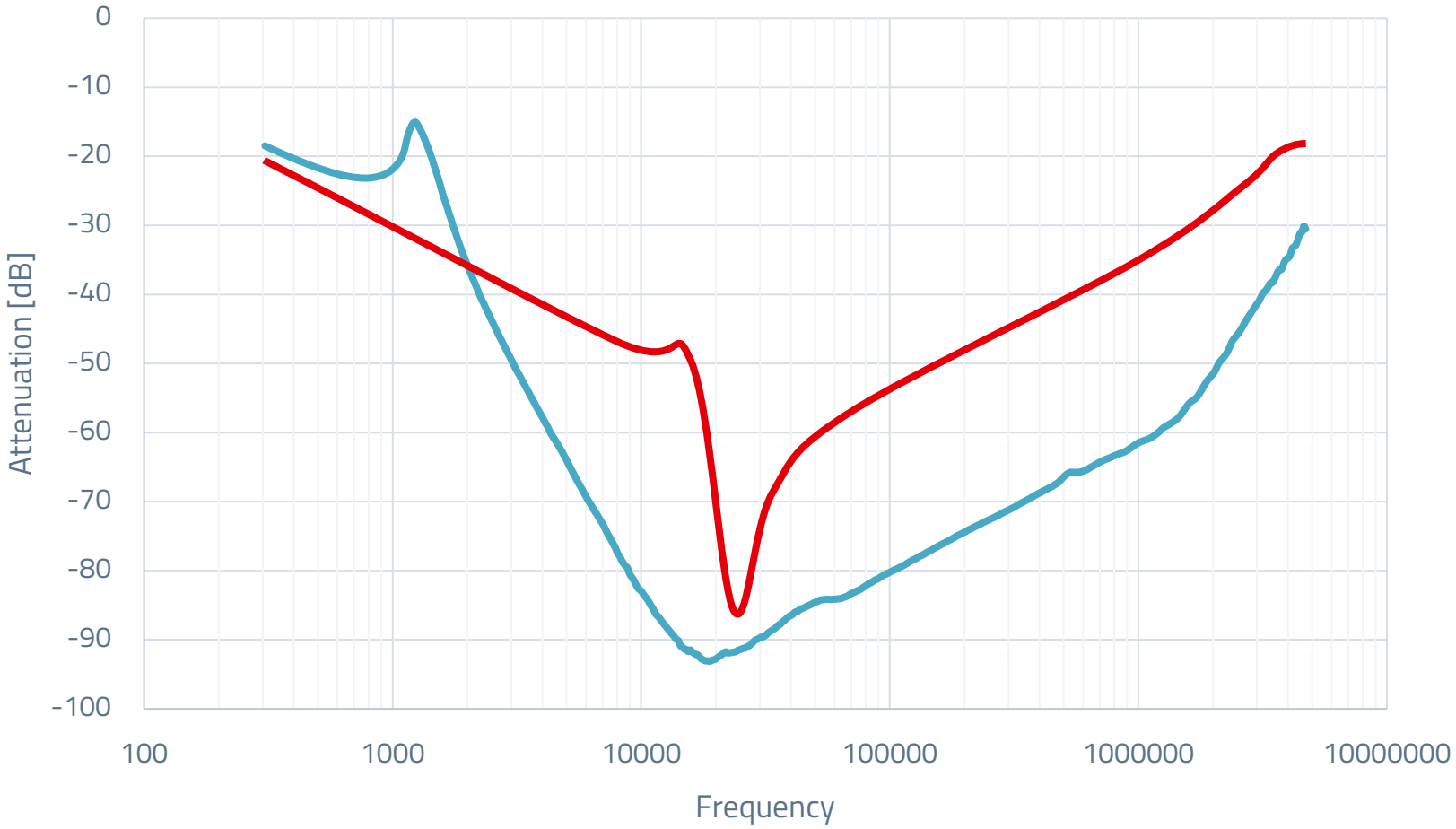
Caps vs. PI-Filter: Impact on the insertion loss with and without a ferrite



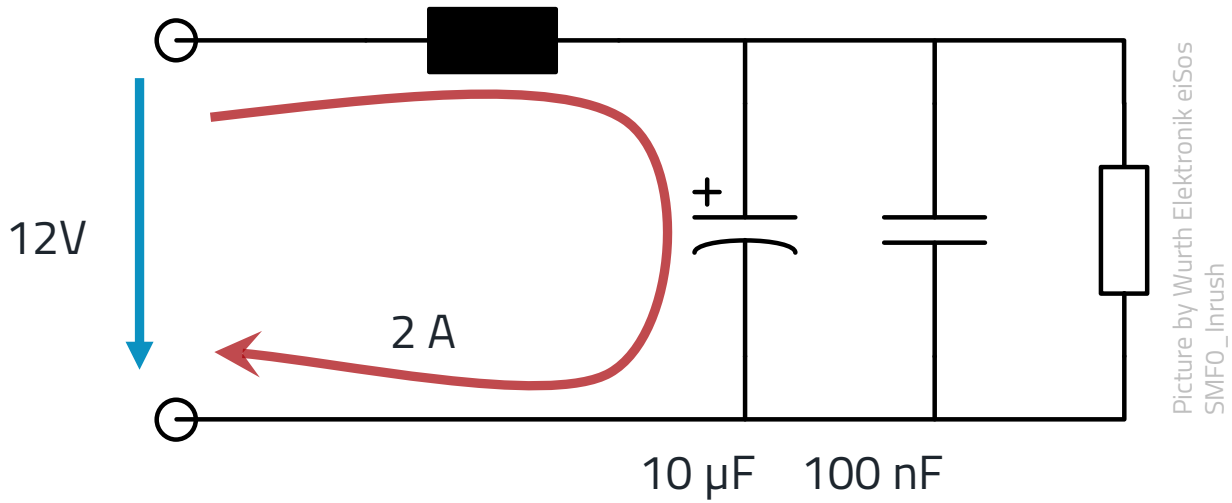
0603, with Ferrite



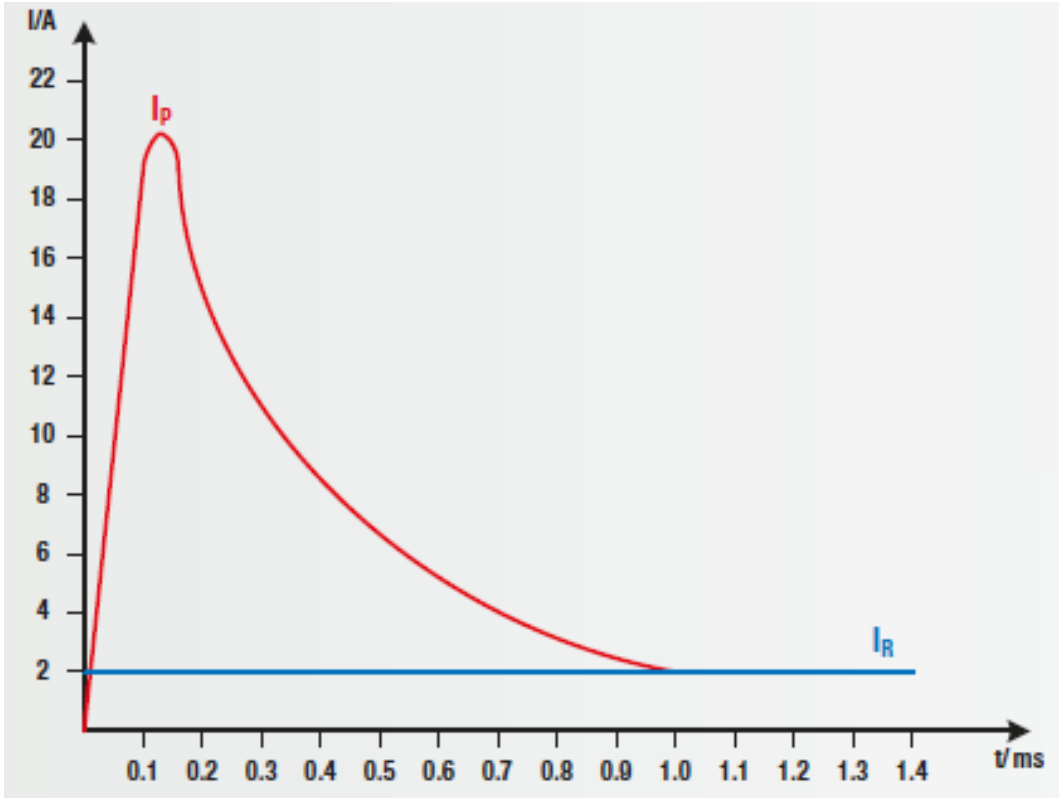
0603, without Ferrite



INRUSH CURRENT

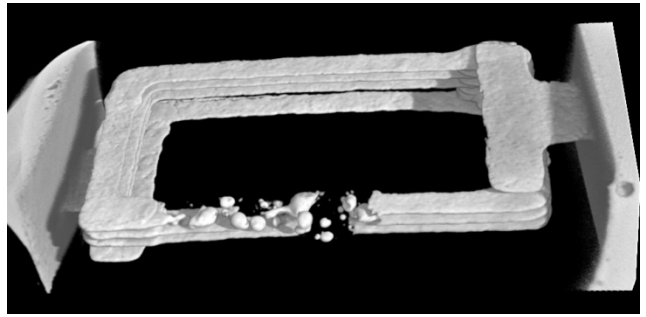


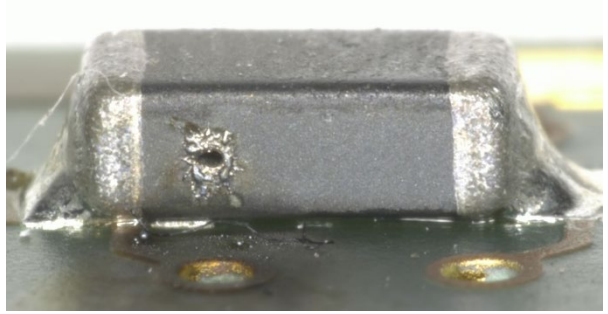
Picture by Wurth Elektronik eiSos
SMFO_Inrush

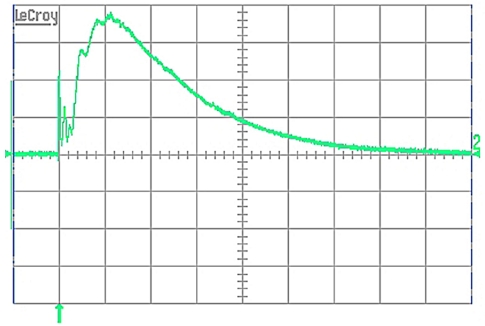


PULSE PEAK OCCURENCE

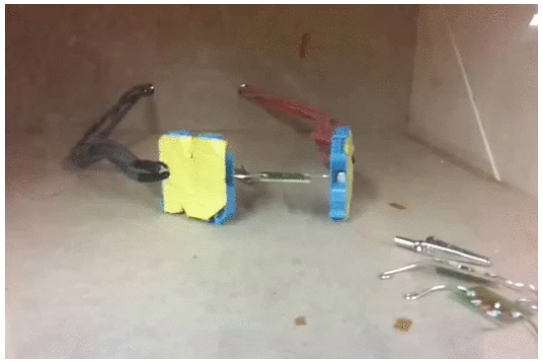
- Part destruction at current peaks over spec value
- Example: Input Line Filter
  - High peak current until capacitor is fully charged.
    - SMD ferrite damage due to peak pulse current possible



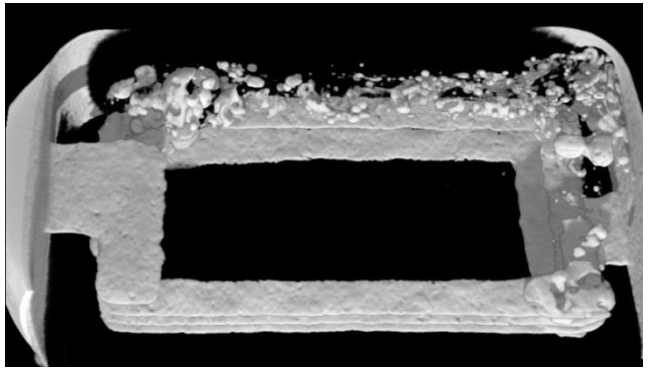




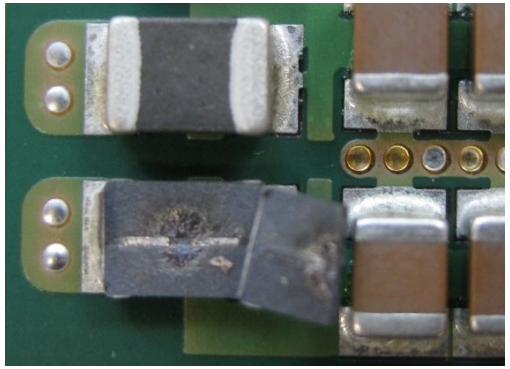
Pictures by Würth Elektronik



Pictures by Würth Elektronik



Pictures by Würth Elektronik

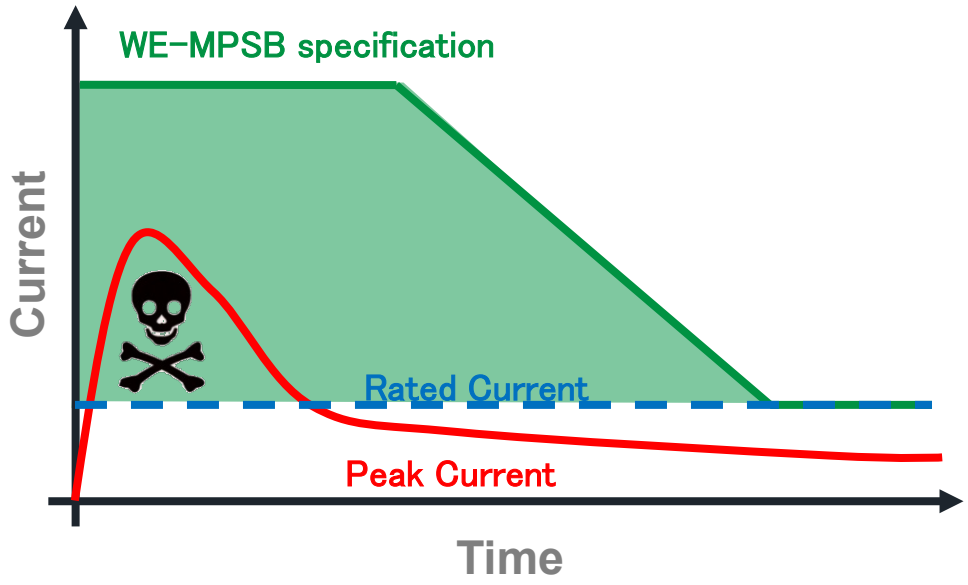


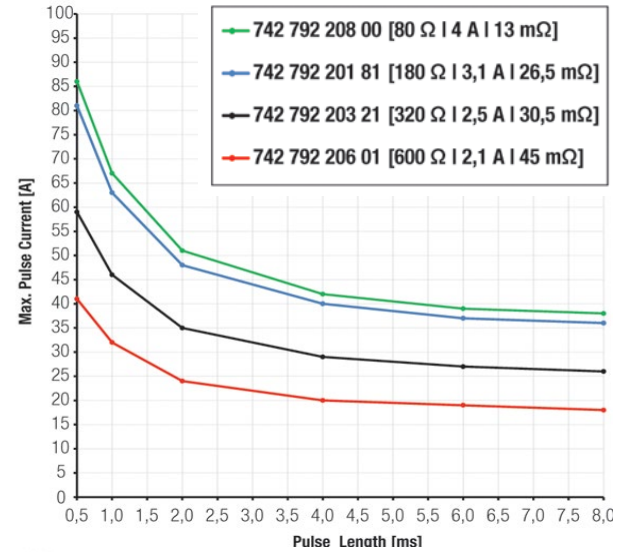
Pictures by Würth Elektronik

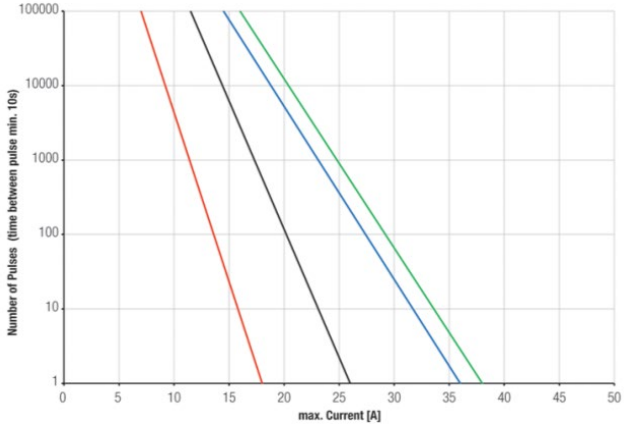
MPSB : MULTILAYER HIGH CURRENT PULSE FERRITE

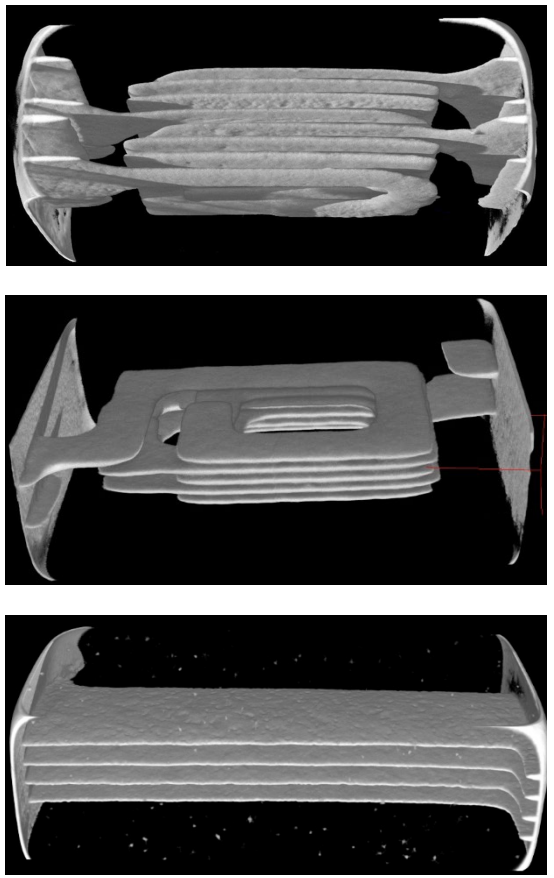
Maximum Peak Current vs Pulse Lenght

- **WE-MPSB**, Pulse definition:
  - Single Pulse 0,5ms – 8ms, 100A max.
  - Multiple Pulse 8ms 100.000 Pulse max.





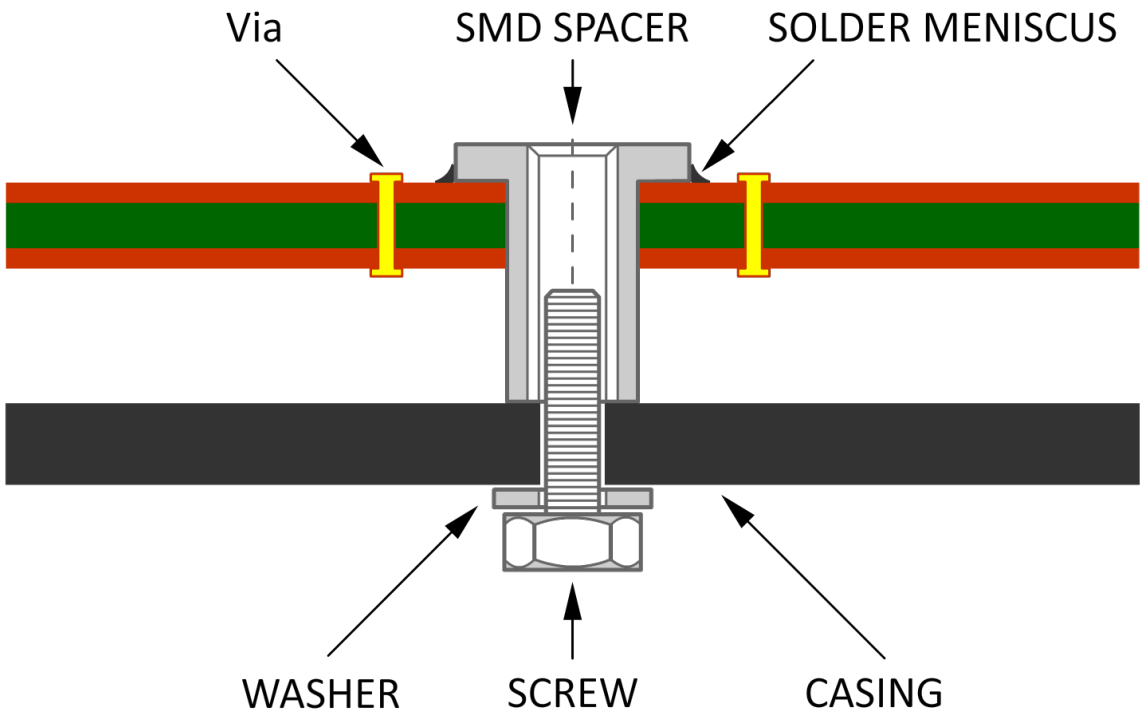




LAYOUT CONCEPTS

SMD Spacer for ground connections

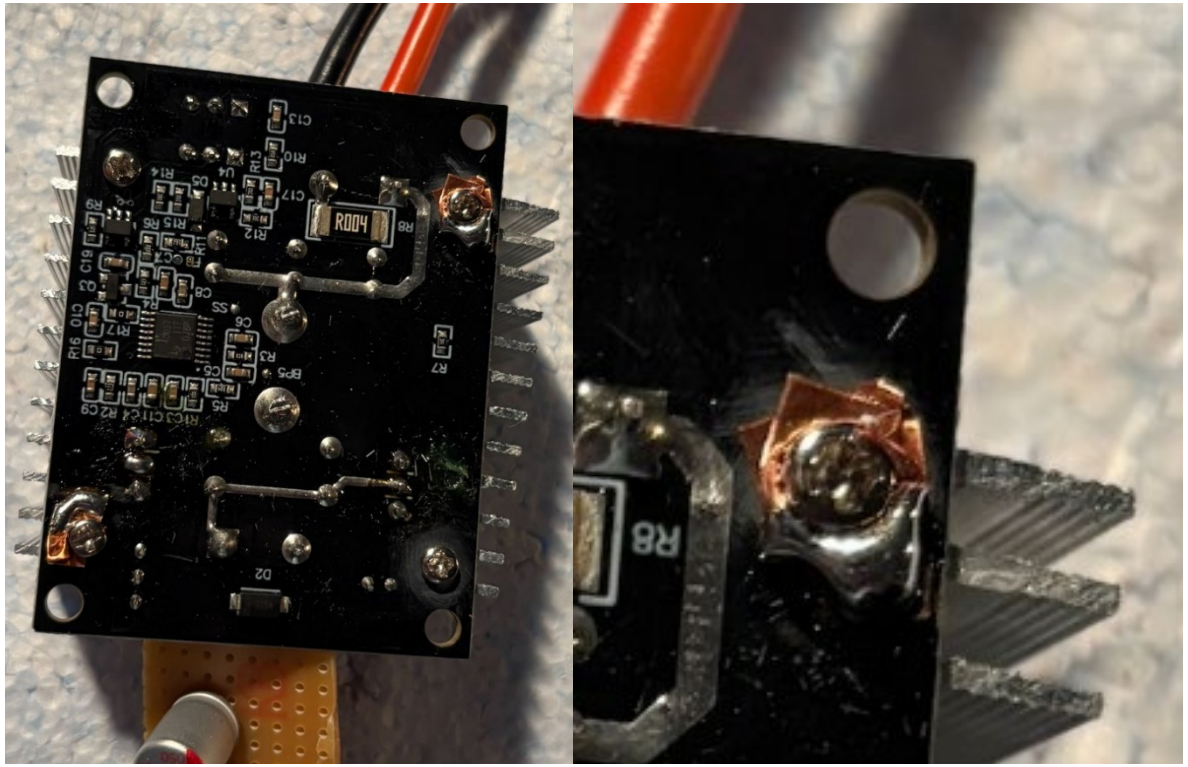
- Tin plated SMD spacers
- Solid solder pad and a big surface area
- Large contact transitions area



HEAT SINK - GND

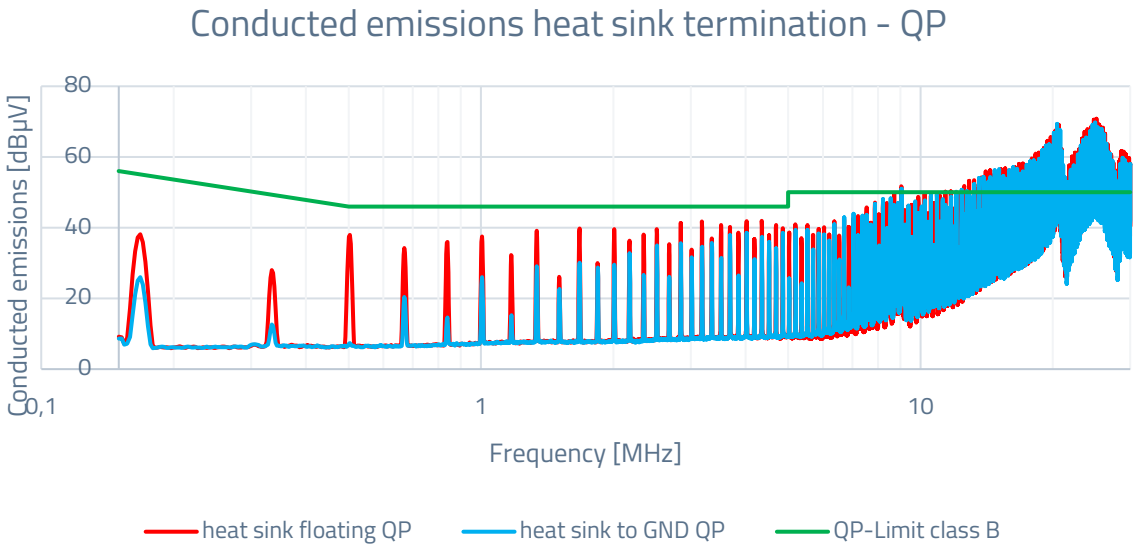
Low-impedance connection

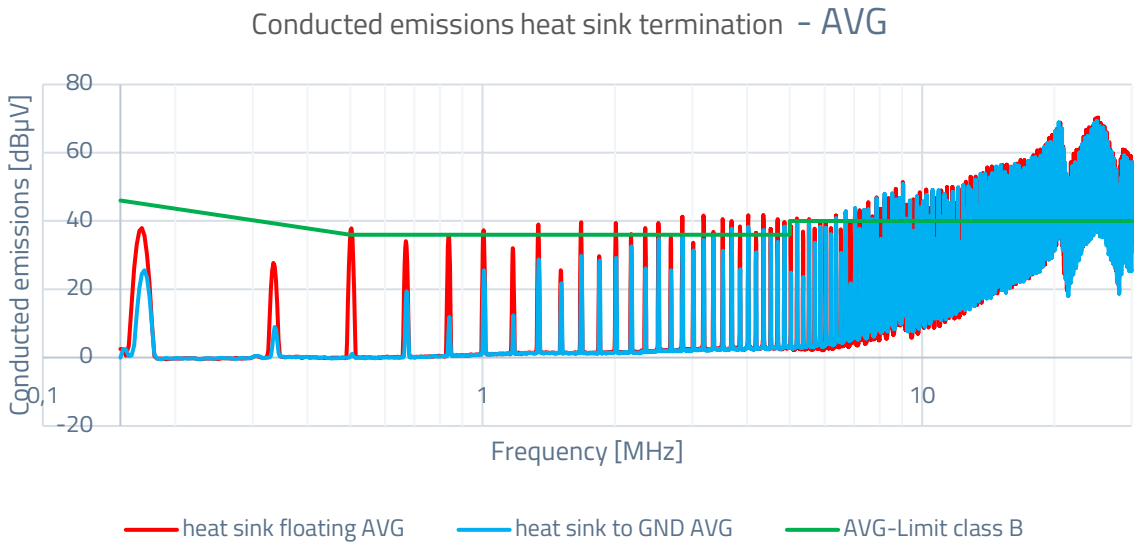
- Solder mask has been removed locally and the GND area enlarged using copper adhesive tape
- A bilateral connection of the heat sink would be preferable from an EMC perspective — not feasible due to layout constraints



HEAT SINK - GND

Low-impedance connection



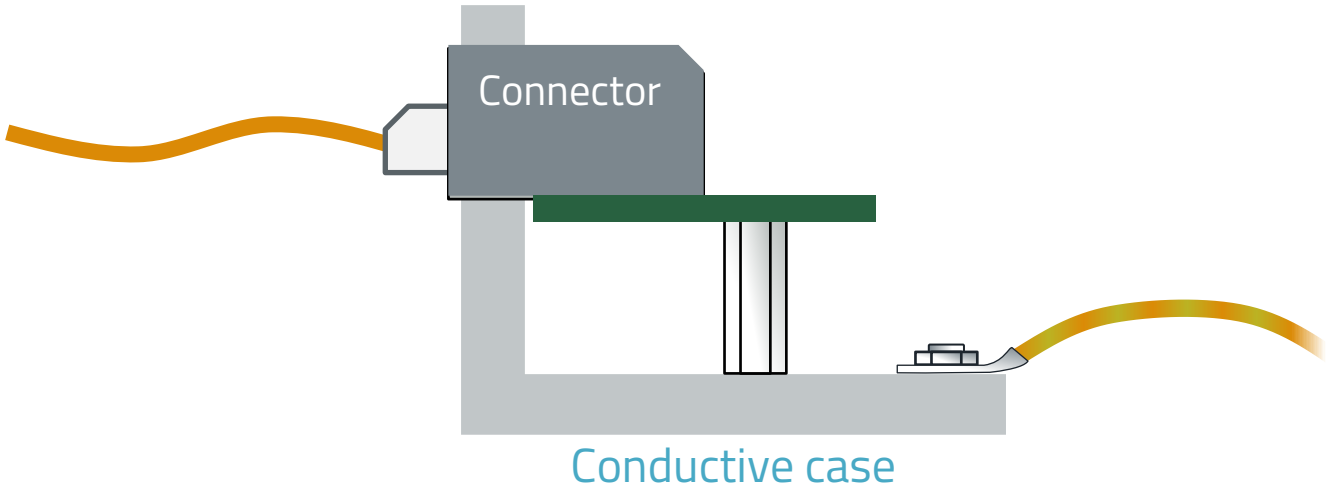


Comparison of conducted emissions on the positive supply line with a floating heat sink and a heat sink connected to GND, with input filter

LAYOUT CONCEPTS

Prevent unintended radiation

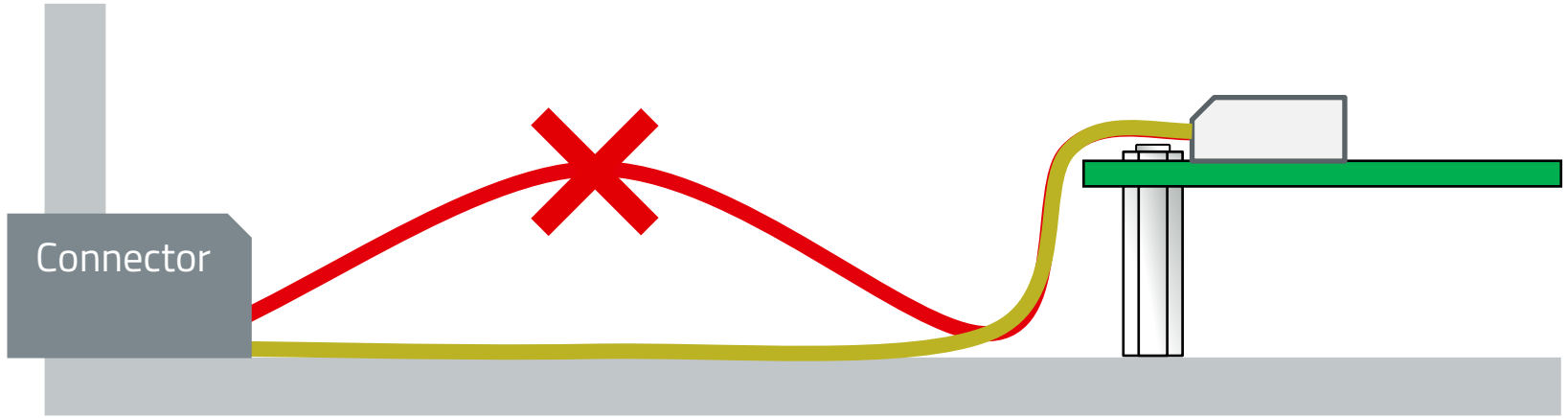
- Bound a circuit GND to chassis at the area where a cable leaves/enters the chassis.
- Connect it with very low impedance
- It is important that GND and chassis have the same potential in the IO area



LAYOUT CONCEPTS

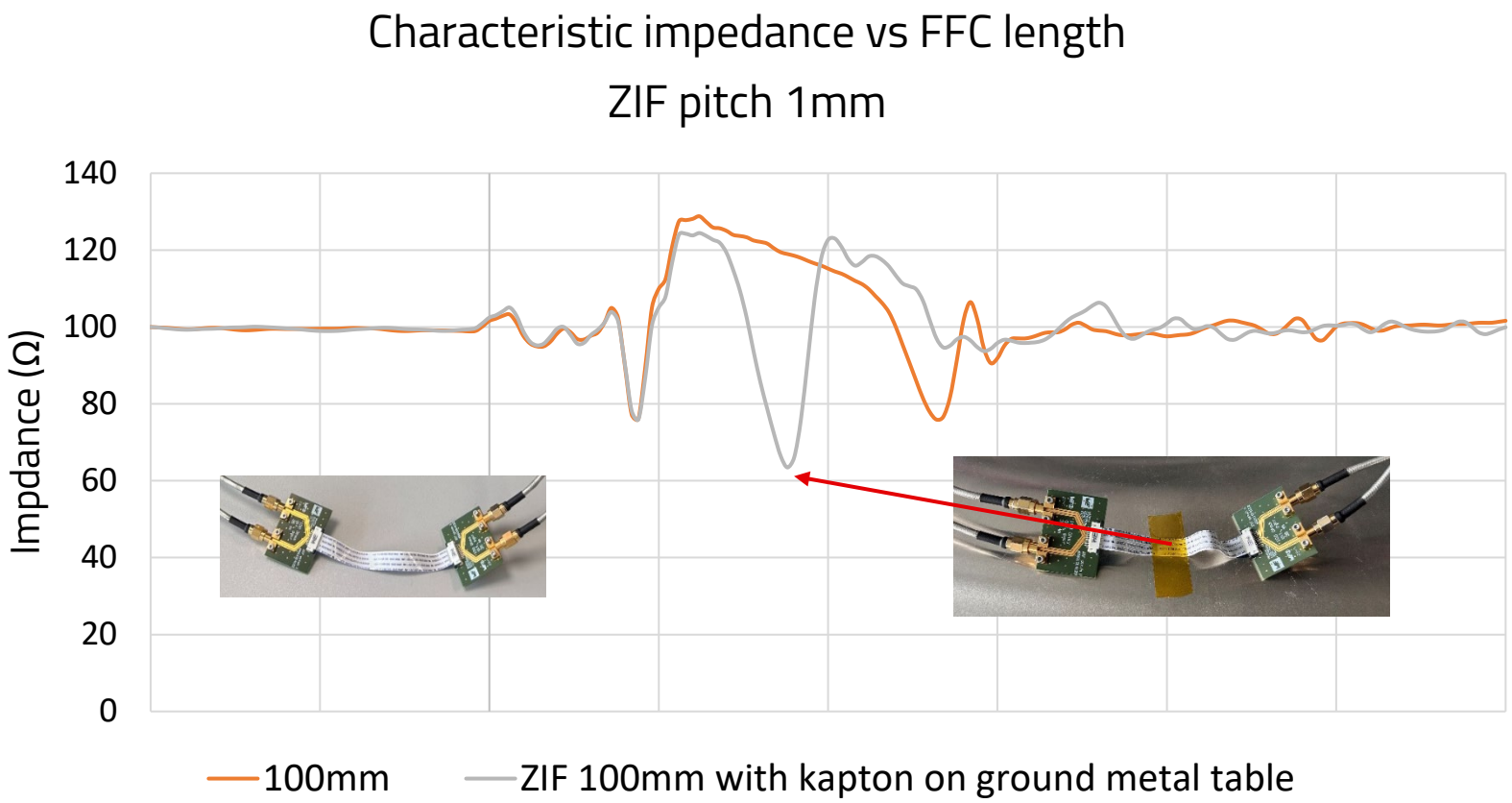
Reduce radiated emission

- Whenever possible, lay cables constantly along the chassis.
- This keeps the electromagnetic field generated by the voltages and currents in the cable at a minimum radiation level.



LAYOUT CONCEPTS

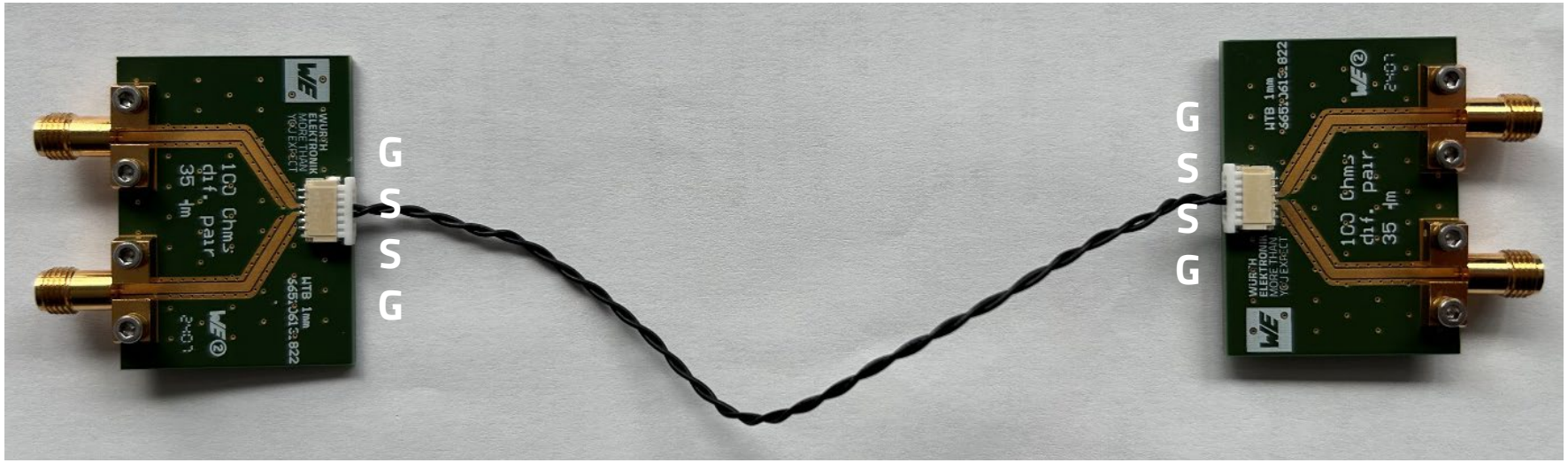
Kapton tape on ground metal plate



SIGNAL INTEGRITY OF NON IMPEDANCE CONTROLLED CONNECTORS

Test setup for wire to board connectors

- Differential pair PCB

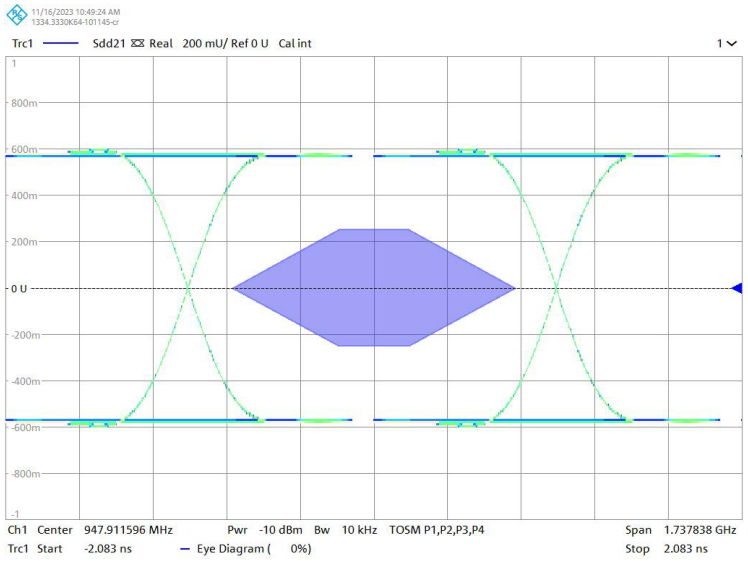


G: Ground
S: Signal

SIGNAL INTEGRITY OF NON IMPEDANCE CONTROLLED CONNECTORS

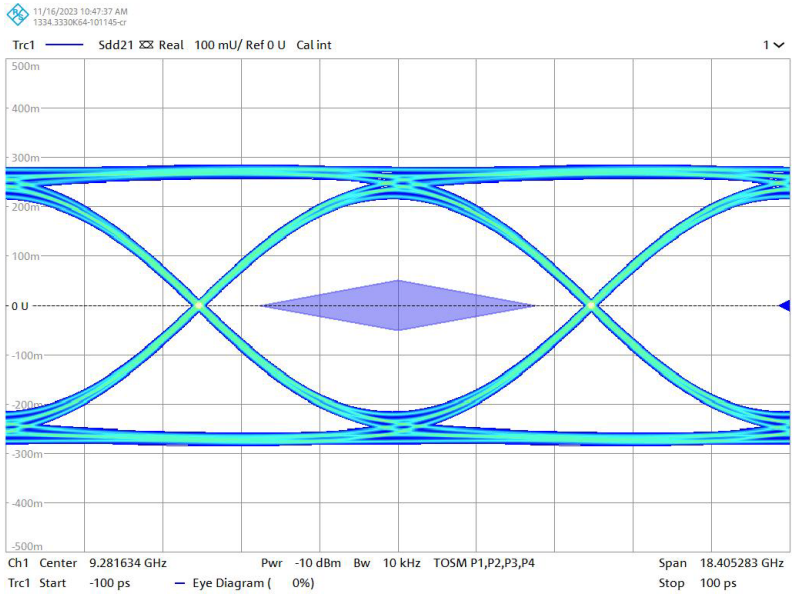
Eye diagram – Pin header 1.27 mm

USB2.0 - 480Mb/s



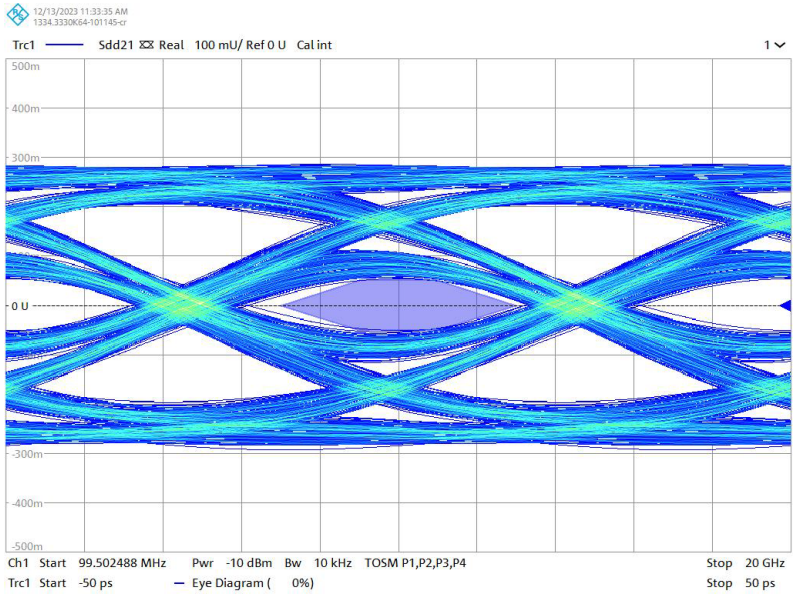
OK

USB3.2 gen 1 - 10Gb/s



OK

USB3.2 gen 2 - 20Gb/s

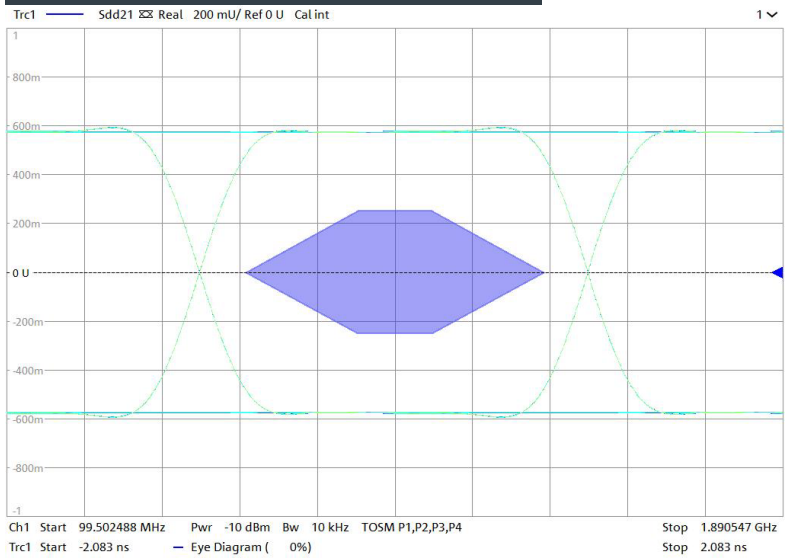


NOK

SIGNAL INTEGRITY OF NON IMPEDANCE CONTROLLED CONNECTORS

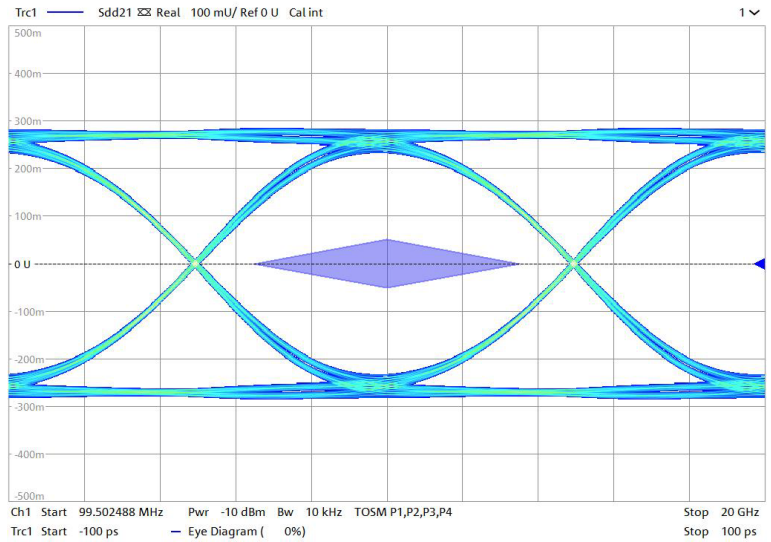
Eye diagram – Pin header 2 mm

USB2.0 - 480Mb/s



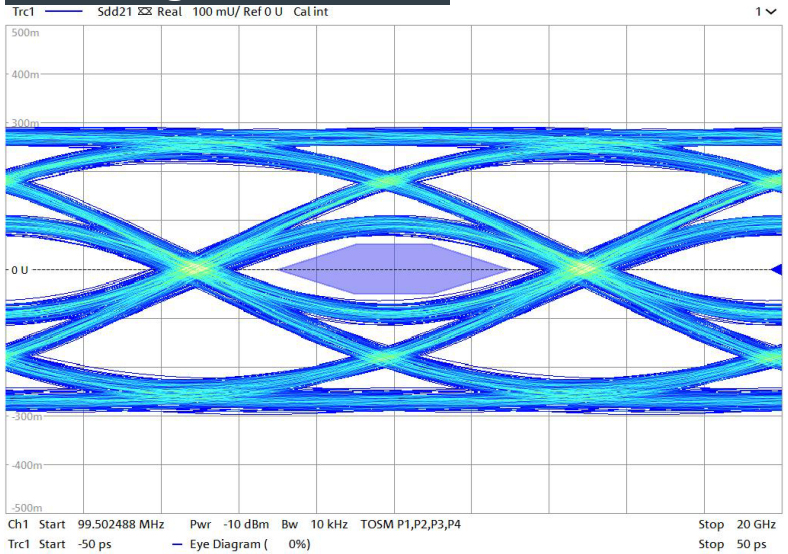
OK

USB3.2 gen 1 - 10Gb/s



OK

USB3.2 gen 2 - 20Gb/s



OK

SIGNAL INTEGRITY OF NON IMPEDANCE CONTROLLED CONNECTORS

WTB 1mm - Effect of twisting cable pairs an it’s impact on a USB 2.0 transmission