# FAN OUT OF A BGA PITCH 0.35 mm – THIS IS HOW IT WORKS!

Michael Kress & Michael Matthes

**WÜRTH ELEKTRONIK** MORE THAN YOU EXPECT

# AGENDA

1. Development flow from the point of view of the developer / designer
   - Specification of the requirements for the assembly
   - Component selection / study of data sheets
   - Clarification of parameters with PCB manufacturer

2. Requirements to the PCB manufacturer
   - What is possible? What is not possible?
   - Where are the limits?
   - Recommendations from PCB manufacturer
   - Challenge impedance
   - Reliability

3. Implementation in design
   - Impedance modules
   - Stack-up
   - Design

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Project Management

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Advanced Solution Center
Specialist Layout and Measurement

# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

Development flow from the developers or designer's point of view

- Specification of the requirements for the assembly
  - Creation of the specifications
- Component selection / study of the data sheets and verification of the required functions
  - Setup of schematic symbols and footprints in the component library
  - Creation of the schematic in the used EDA-tool
  - Clarification of the impedance requirements from the circuit and the components used
  - Entering the parameters in the constraint sets / rules (schematic / layout)
- Clarification of the parameters with the PCB manufacturer
  - Stack-Up
  - Material
  - Impedance Modules
  - Other parameters

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## Component selection and study of the data sheet

CYPRESS EMBEDDED IN TOMORROW™

**PSoC 6 MCU: CY8C63x6, CY8C63x7 Datasheet**

**PSoC 63 MCU with Bluetooth LE**

### General Description

PSoC® 6 MCU is a high-performance, ultra-low-power and secured MCU platform, purpose-built for IoT applications. The PSoC 63 with Bluetooth LE product line, based on the PSoC 6 MCU platform, is a combination of a high-performance microcontroller with low-power flash technology, digital programmable logic, high-performance analog-to-digital conversion and standard communication and timing peripherals.

The PSoC 63 product line provides wireless connectivity with Bluetooth LE 5.0 compliance.

### Features

**32-bit Dual CPU Subsystem**

- 150-MHz Arm® Cortex®-M4F (CM4) CPU with single-cycle multiply, floating point, and memory protection unit (MPU)
- 100-MHz Cortex-M0+ (CM0+) CPU with single-cycle multiply and MPU
- User-selectable core logic operation at either 1.1 V or 0.9 V
- Active CPU current slope with 1.1-V core operation
  - Cortex-M4: 40 µA/MHz
  - Cortex-M0+: 20 µA/MHz
- Active CPU current slope with 0.9-V core operation
  - Cortex-M4: 22 µA/MHz
  - Cortex-M0+: 15 µA/MHz
- Two DMA controllers with 16 channels each

**Memory Subsystem**

- 1-MB application flash, 32-KB auxiliary flash (AUXflash), and 32-KB supervisory flash (SFlash); read-while-write (RWW) support. Two 8-KB flash caches, one for each CPU.
- 288-KB SRAM with power and data retention control
- One-time-programmable (OTP) 1-Kb eFuse array

**Bluetooth Low Energy Subsystem**

- 2.4-GHz RF transceiver with 50-Ω antenna drive
- Digital PHY
- Link Layer engine supporting master and slave modes
- Programmable TX power: up to 4 dBm
- RX sensitivity: –95 dBm
- RSSI: 4-dB resolution
- 5.7-mA Tx (0 dBm) and 6.7 mA RX (2 Mbps) current with 3.3-V supply and internal SIMO Buck converter
- Link Layer engine supports four connections simultaneously
- Supports 2 Mbps data rate

**Low-Power 1.7-V to 3.6-V Operation**

- Six power modes for fine-grained power management
- Deep Sleep mode current of 7 µA with 64-KB SRAM retention
- On-chip Single-In Multiple Out (SIMO) DC-DC buck converter, <1 µA quiescent current
- Backup domain with 64 bytes of memory and real-time clock

**Flexible Clocking Options**

- 8-MHz Internal Main Oscillator (IMO) with ±2% accuracy
- Ultra-low-power 32-kHz Internal Low-speed Oscillator (ILO)
- On-chip crystal oscillators (16 to 35 MHz, and 32 kHz)
- Phase-locked loop (PLL) for multiplying clock frequencies
- Frequency-locked loop (FLL) for multiplying IMO frequency
- Integer and fractional peripheral clock dividers

**Quad SPI (QSPI)/Serial Memory Interface (SMIF)**

- Execute-In-Place (XIP) from external quad SPI Flash
- On-the-fly encryption and decryption
- 4-KB cache for greater XIP performance with lower power
- Supports single, dual, quad, dual-quad, and octal interfaces with throughput up to 640 Mbps

**Segment LCD Drive**

- Supports up to 83 segments and up to 8 commons

**Serial Communication**

- Nine run-time configurable serial communication blocks (SCBs)
  - Eight SCBs: configurable as SPI, I²C, or UART
  - One Deep Sleep SCB: configurable as SPI or I²C
- USB full-speed device interface

**Audio Subsystem**

- Two pulse density modulation (PDM) channels and one I²S channel with time division multiplexed (TDM) mode

**Timing and Pulse-Width Modulation**

- Thirty-two timer/counter/pulse-width modulators (TCPWM)
- Center-aligned, edge, and pseudo-random modes
- Comparator-based triggering of Kill signals

**Programmable Analog**

- 12-bit 1-Msps SAR ADC with differential and single-ended modes and 16-channel sequencer with result averaging
- Two low-power comparators available in Deep Sleep and Hibernate modes
- Built-in temperature sensor connected to ADC
- One 12-bit voltage-mode digital-to-analog converter (DAC) with < 2-µs settling time
- Two opamps with low-power operation modes

**Cypress Semiconductor Corporation** • 198 Champion Court • San Jose, CA 95134-1709 • 408-943-2600
Document Number: 002-18787 Rev. *Q Revised October 31, 2022

**Figure 15. 104-M-CSP-USB Power Connection Diagram**

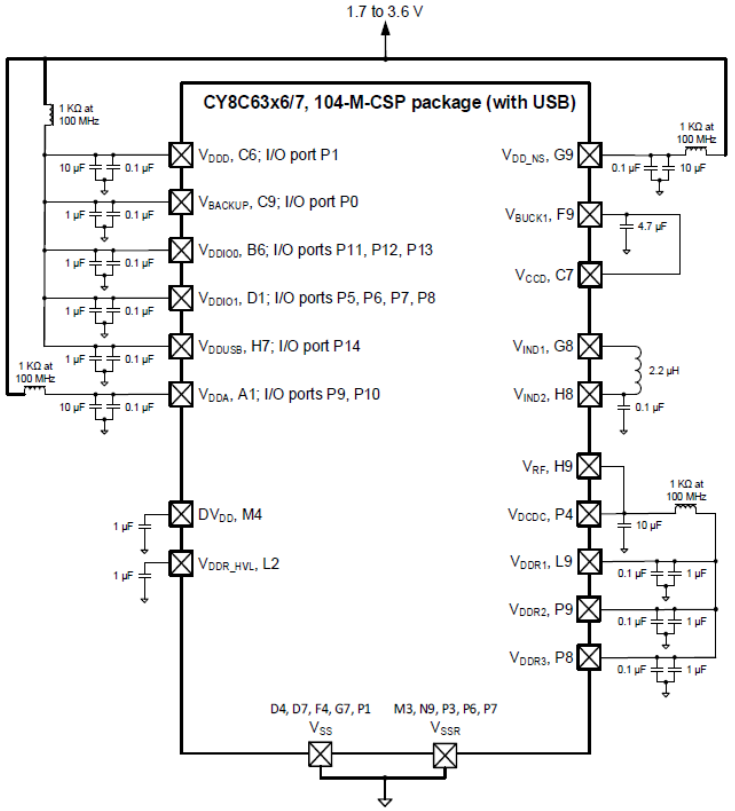
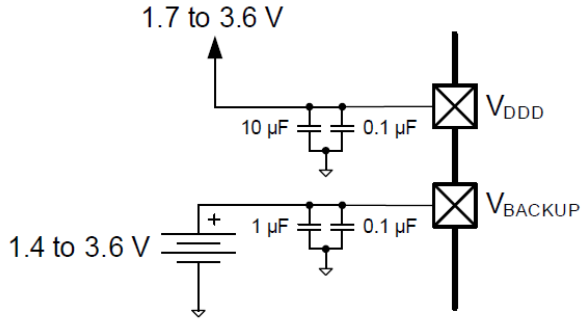



**Figure 17. Separate Battery Connection to $V_{BACKUP}$**




- $V_{DDUSB}$: the supply for the USB peripheral and the USBDP and USBDM pins. It must be 2.85 V to 3.6 V for USB operation. If USB is not used, it can be 1.7 V to 3.6 V, and the USB pins can be used as limited-capability GPIOs on I/O port 14.

Table 10 shows a summary of the I/O port supplies:

**Table 10. I/O Port Supplies**

| Port | Supply | Alternate Supply |
|---|---|---|
| 0 | $V_{BACKUP}$ | $V_{DDD}$ |
| 1 | $V_{DDD}$ | - |
| 5, 6, 7, 8 | $V_{DDIO1}$ | - |
| 9, 10 | $V_{DDIOA}$ | $V_{DDA}$ |
| 11, 12, 13 | $V_{DDIO0}$ | - |
| 14 | $V_{DDUSB}$ | - |

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## Setup of the component footprint



### Packaging

This product line is offered in four packages: 68-QFN, 116-BGA, 124-BGA, and 104-M-CSP.

**Table 60. Package Dimensions**

| Spec ID# | Package | Description | Package Drawing Number |
|---|---|---|---|
| PKG_1 | 124-BGA | 124-BGA, 9 × 9 × 1 mm height with 0.65-mm pitch | 001-97718 |
| PKG_2 | 104-M-CSP | 104-M-CSP, 3.8 × 5 × 0.65 mm height with 0.35-mm pitch | 002-16508 |
| PKG_4 | 116-BGA | 116-BGA, 5.2 × 6.4 × 0.70 mm height with 0.5-mm pitch | 002-16574 |
| PKG_5 | 68-QFN | 68-QFN, 8 × 8 × 1 mm height with 0.4-mm pitch | 001-96836 |

**Table 61. Package Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_A$ | Operating ambient temperature | – | –40 | 25.00 | 85 | °C |
| $T_J$ | Operating junction temperature | – | –40 | – | 100 | °C |
| $T_{JA}$ | Package $\theta_{JA}$ (124-BGA) | – | – | 64.3 | – | °C/watt |
| $T_{JC}$ | Package $\theta_{JC}$ (124-BGA) | – | – | 37 | – | °C/watt |
| $T_{JA}$ | Package $\theta_{JA}$ (116-BGA) | – | – | 36.5 | – | °C/watt |
| $T_{JC}$ | Package $\theta_{JC}$ (116-BGA) | – | – | 12 | – | °C/watt |
| $T_{JA}$ | Package $\theta_{JA}$ (104-CSP) | – | – | 33.7 | – | °C/watt |
| $T_{JC}$ | Package $\theta_{JC}$ (104-CSP) | – | – | 0.2 | – | °C/watt |
| $T_{JA}$ | Package $\theta_{JA}$ (68-QFN) | – | – | 21.6 | – | °C/watt |
| $T_{JC}$ | Package $\theta_{JC}$ (68-QFN) | – | – | 7.2 | – | °C/watt |

**Table 62. Solder Reflow Peak Temperature**

| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---|---|---|
| 124-BGA, 116-BGA, and 68-QFN | 260 °C | 30 seconds |
| 104-M-CSP | 260 °C | 30 seconds |

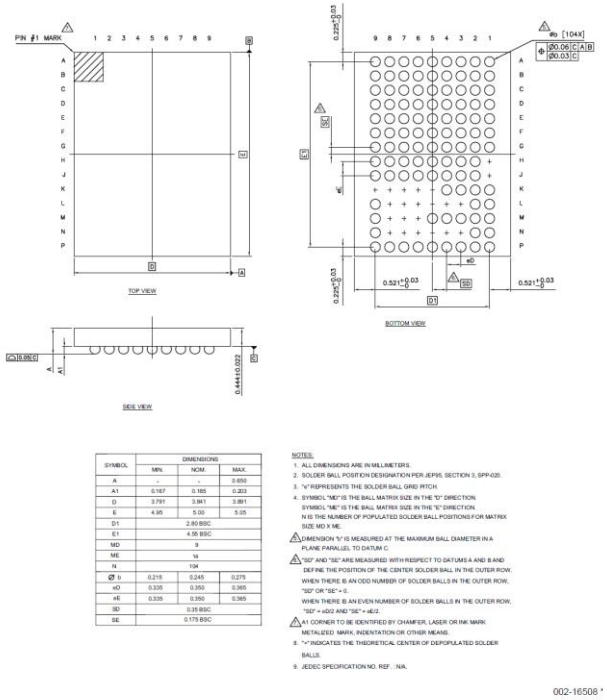
**Table 63. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

| Package | MSL |
|---|---|
| 124-BGA, 116-BGA, and 68-QFN | MSL 3 |
| 104-M-CSP | MSL 1 |

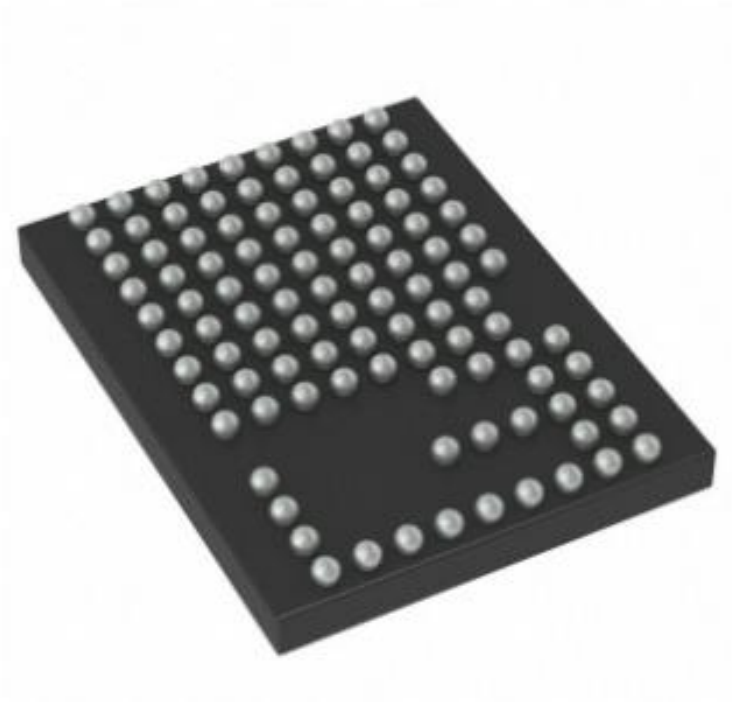




**Figure 21. 104-M-CSP 3.8 × 5.0 × 0.65 mm**



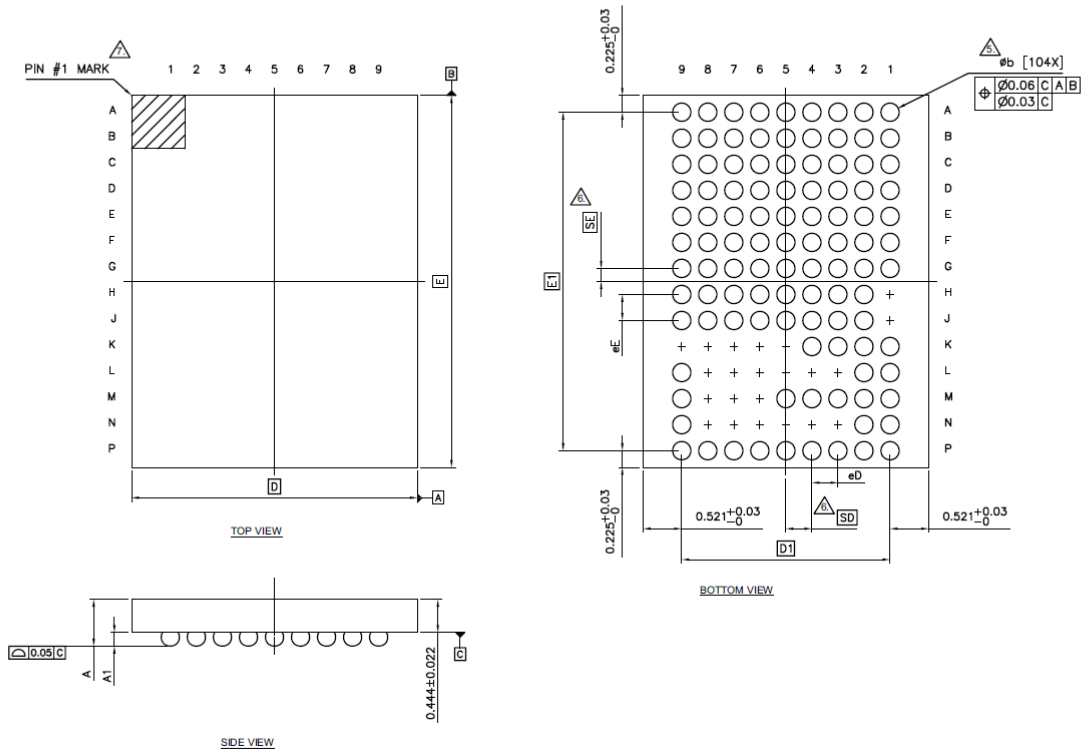

002-16508 *E



# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

PSoC 6 MCU: CY8C63x6,
CY8C63x7 Datasheet

Figure 21. 104-M-CSP 3.8 × 5.0 × 0.65 mm




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | - | 0.650 |
| A1 | 0.167 | 0.185 | 0.203 |
| D | 3.791 | 3.841 | 3.891 |
| E | 4.95 | 5.00 | 5.05 |
| D1 | 2.80 BSC | | |
| E1 | 4.55 BSC | | |
| MD | 9 | | |
| ME | 14 | | |
| N | 104 | | |
| Ø b | 0.215 | 0.245 | 0.275 |
| eD | 0.335 | 0.350 | 0.365 |
| eE | 0.335 | 0.350 | 0.365 |
| SD | 0.35 BSC | | |
| SE | 0.175 BSC | | |

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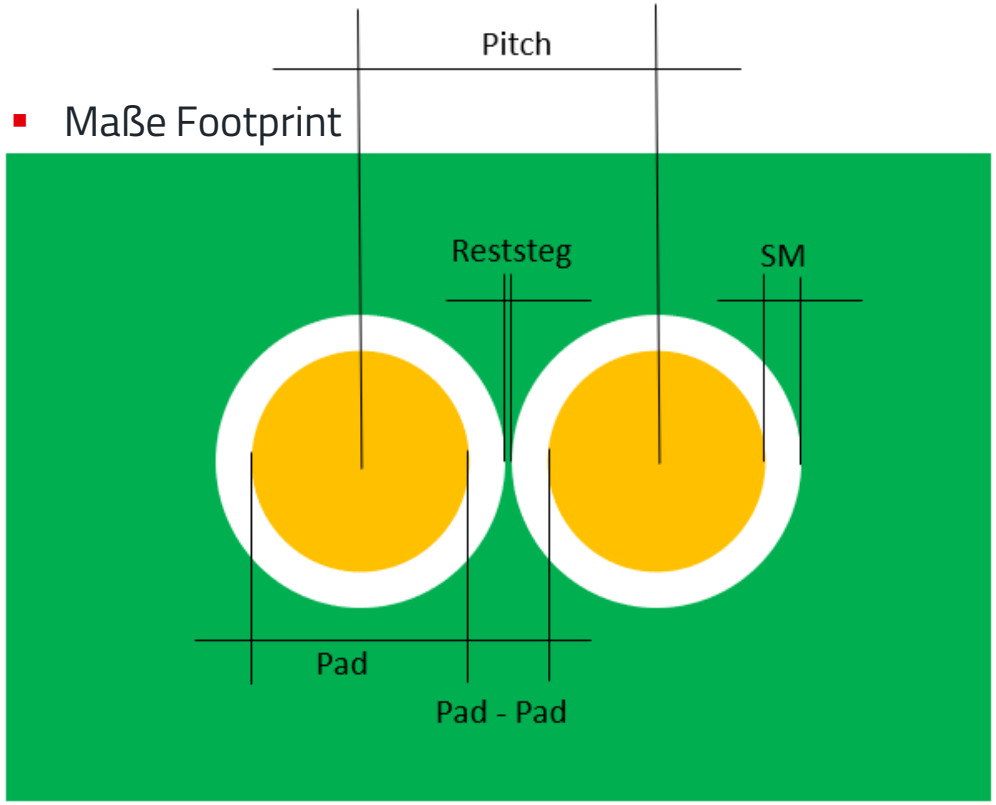
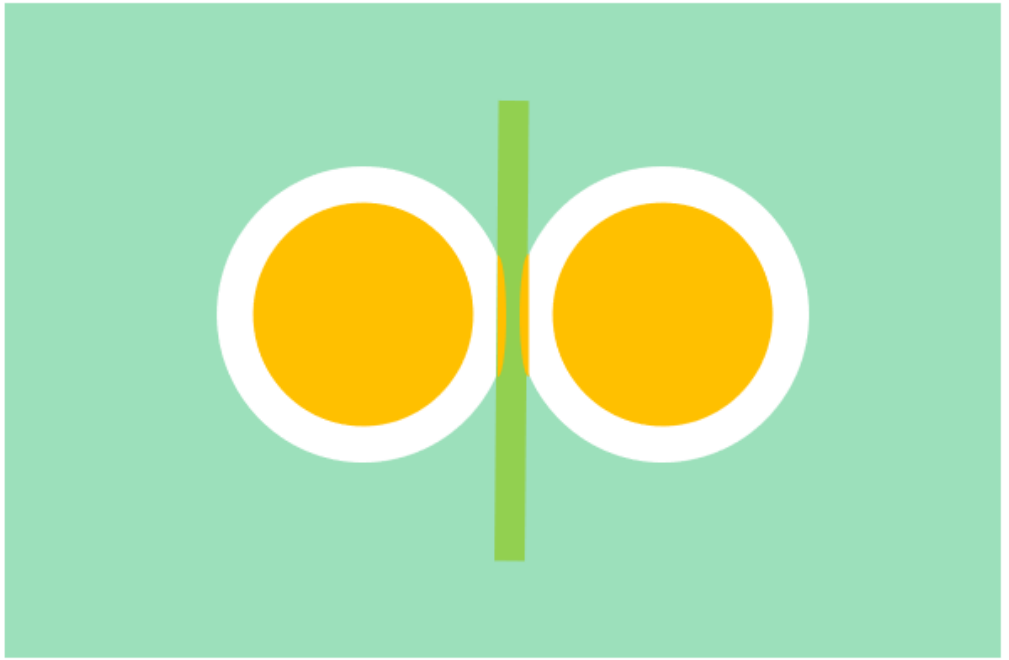
Setup with standard parameters

- Maße Footprint




| Pitch [um] | Pad [um] | SM [um] | Reststeg [um] | uVia [um] | Pad-Pad [um] | L/S [um] |
|---|---|---|---|---|---|---|
| 350 | 240 | 50 | 10 | 85/215 | 110 | |

- eine Leitung zwischen den Pads



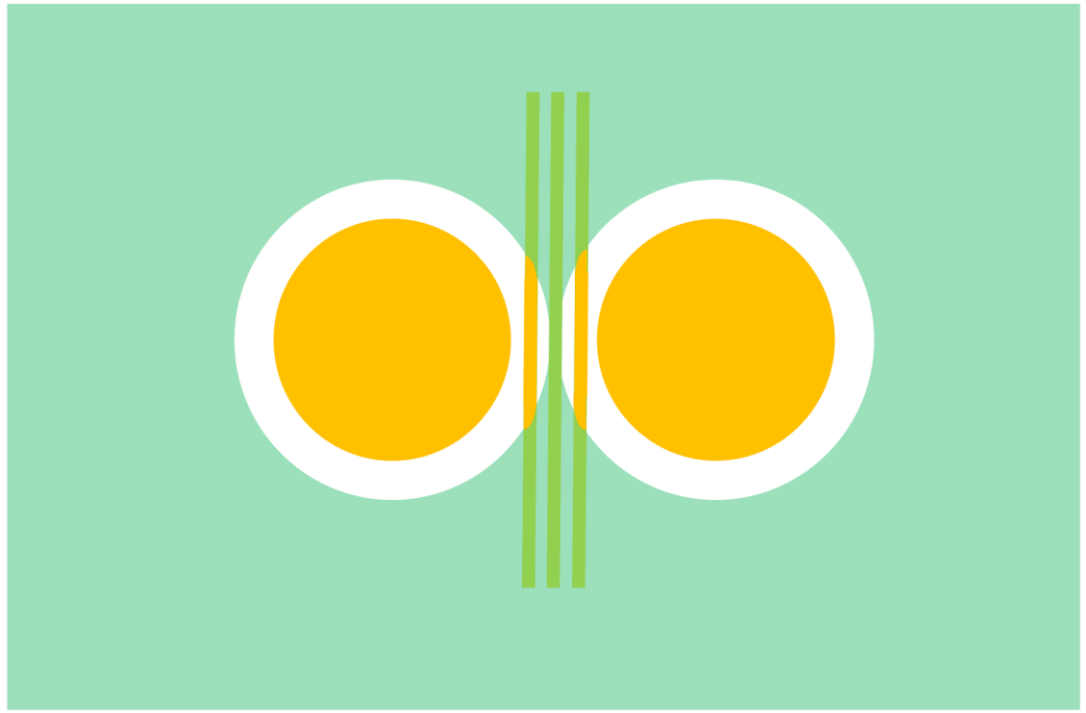
| Pitch [um] | Pad [um] | SM [um] | Reststeg [um] | uVia [um] | Pad-Pad [um] | L/S [um] |
|---|---|---|---|---|---|---|
| 350 | 240 | 50 | 10 | 85/215 | 110 | 36,67 |

# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

Anlage mit Standardparametern

- for complete routing including the inner rows of pins, 3 to 4 traces would have to be routed between the pads
- 15.71 µm line/space are currently not yet feasible in the printed circuit board process

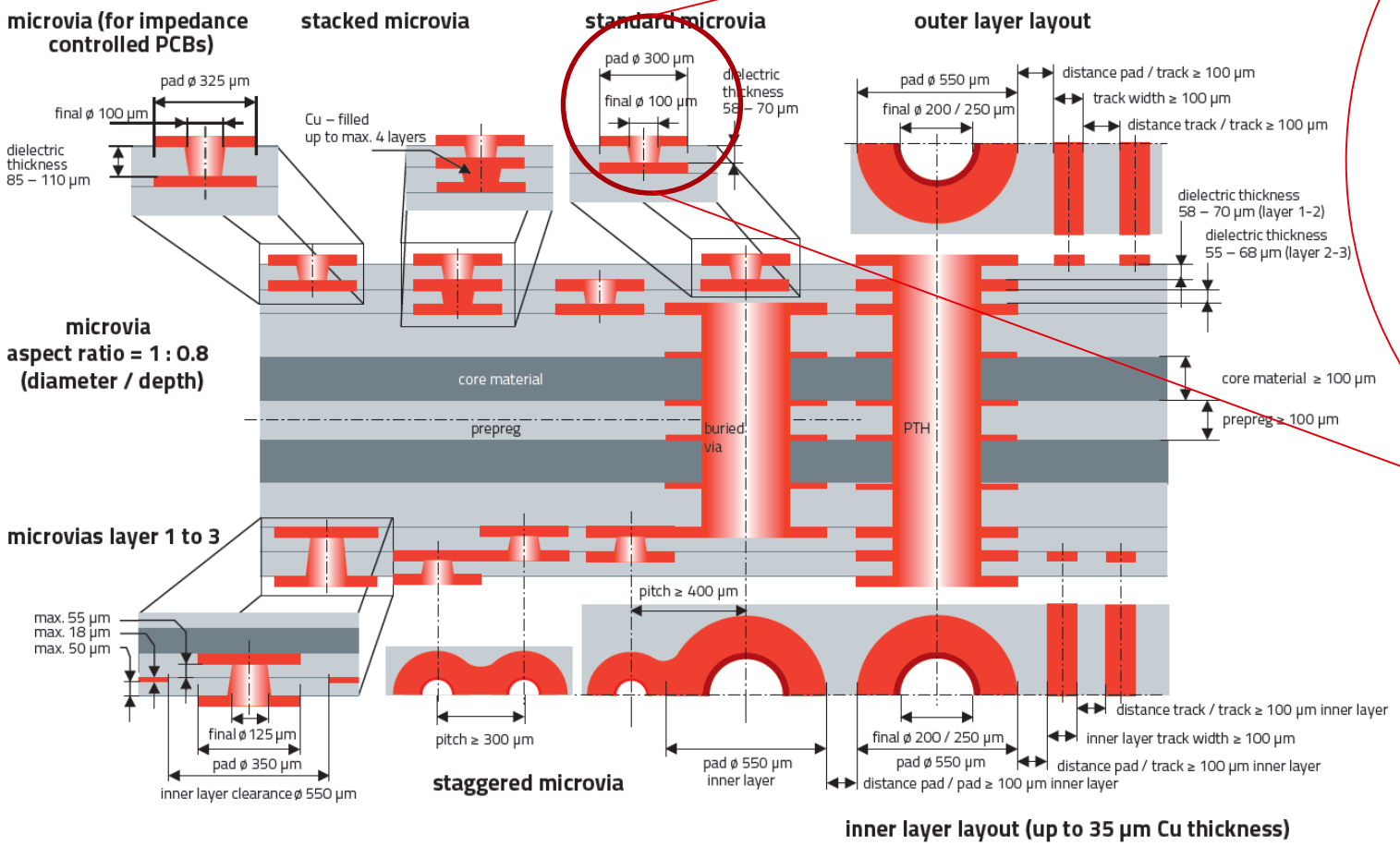
*What are the options for realization?*

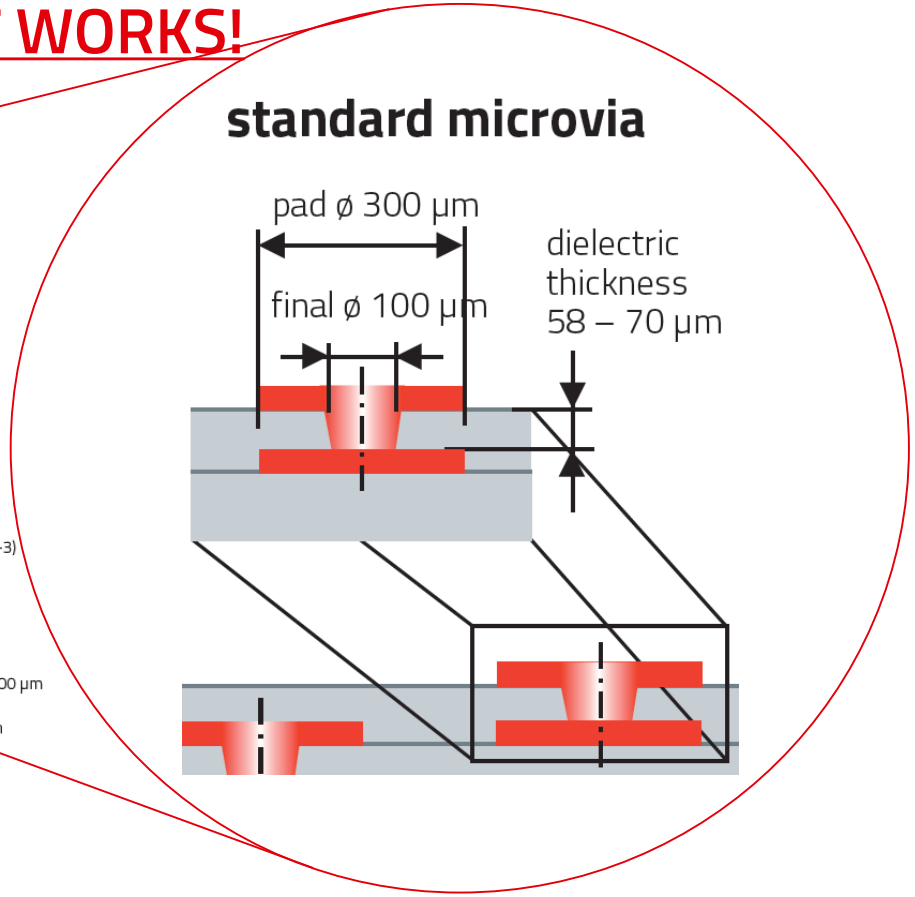


| Pitch [um] | Pad [um] | SM [um] | Reststeg [um] | uVia [um] | Pad-Pad [um] | L/S [um] |
|---|---|---|---|---|---|---|
| 350 | 240 | 50 | 10 | 85/215 | 110 | 15,71 |

# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

What is possible, what is not possible?

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# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

The limits of MICROVIA.**hdi**

- Limit soldermask - WHY?
  - min. web width = 70 µm
  - min. distance solder mask web to pad edge = 35 µm

In total: Pad edge to pad edge min.140 µm, see sketch on the right side

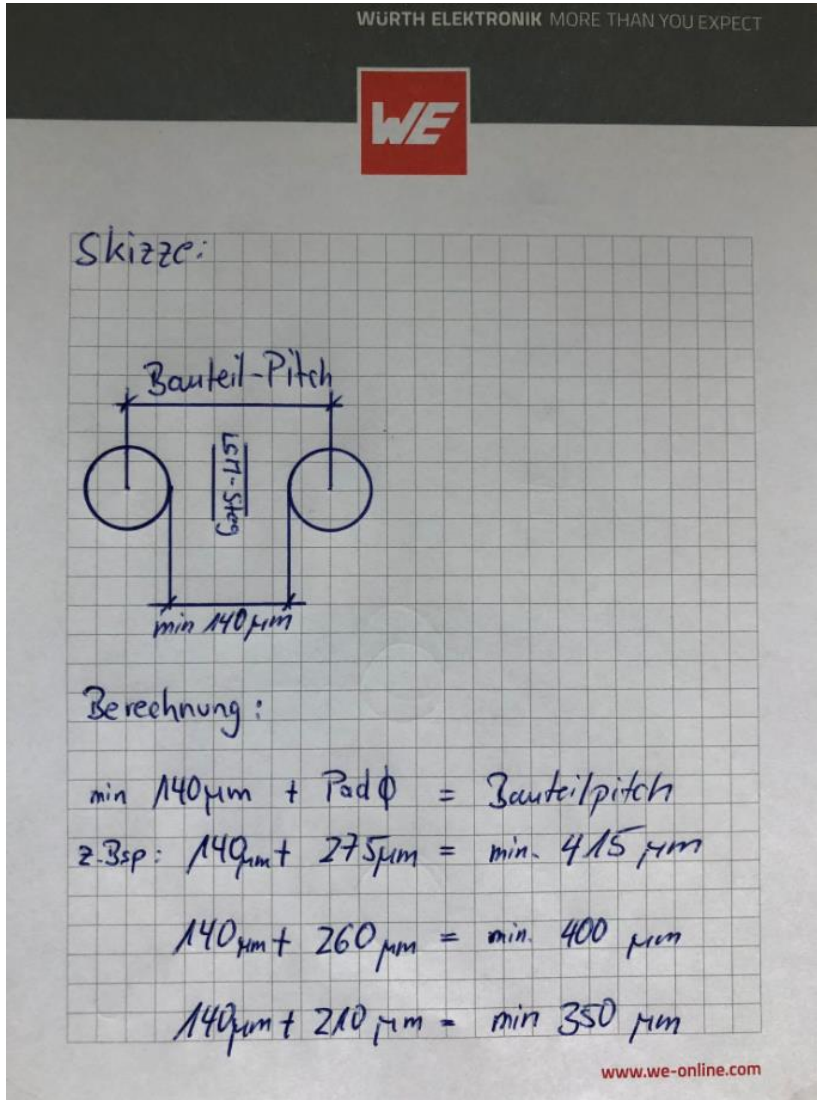
In the design for 0.40 mm BGA pitch this means:

- maximum possible solder mask web at the narrow point:

  400 µm (pitch) - 275 µm (pad) - 2x (35 µm (solder mask clearance))

  = 50 µm solder mask web

| Solder Mask | | |
|---|---|---|
| | **Standard** | **Advanced** |
| **Clearance** | **≥ 50 µm** | 35 µm |
| **Coverage** | **50 µm** | 40 µm |
| **Solder mask web** | **≥ 70 µm** | – |
| **Via-opening** | final diameter +0,25 mm | |



# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

The design recommendations from PCB manufacturer

- **Design Rules for the BGA component on the outer layer**
  - BGA solder pad = Ø215 µm
  - µVia-in-Pad design µViaØ typically 85 µm (dielectric 70 µm – 100 µm thick)

- **Design Rules soldermask for the BGA component on the outer layer**
  - solder mask – clearance component pad circumferential = 35 µm
  - solder mask web = 65 µm

**Calculation for a BGA pitch 0,35 mm:**

215 µm (component pad) + (2 x 35 µm (solder mask clearance)) + 65 µm (solder mask web)

= 350 µm ✓

# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

## Stackup from PCB manufacturer

| | |
|---|---|
| customer | WE - SLIM.hdi_Webinar Mai 2023 |
| pcb name | |
| WE-number | xyz |
| engineer | M. Kress |
| date | |

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SLIM.**hdi 1-2b-1**

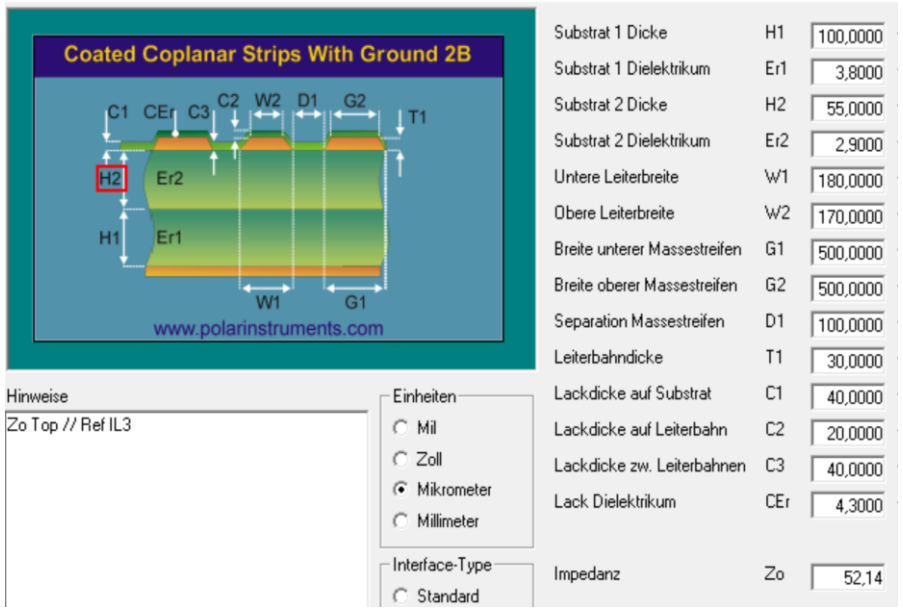
**PCB Thickness :** **0,31** **mm +/-0,05mm**

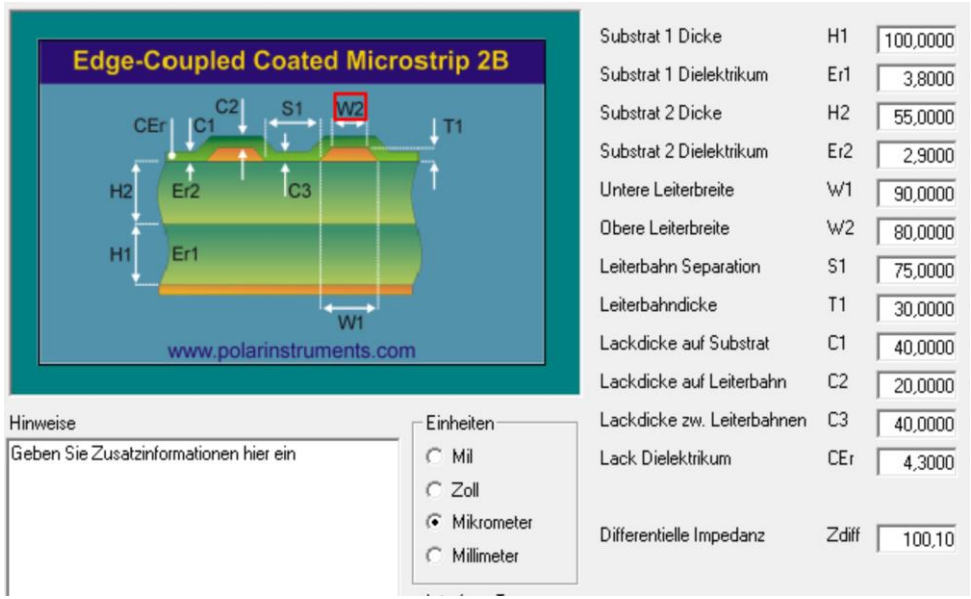
| Rigid area Structure | | Rigid area Thickness | Material description | rigid area | | Viatypes | Layer usage | Impedance Er | Impedance Z[Ohm] / Line / Space |
|---|---|---|---|---|---|---|---|---|---|
| | | 20 | Soldermask photosensitive, flexible | | | | | | |
| L1 | | 30 | 9µm copper foil + plating | Top-Layer | | | S1 | | Zo[50] = 180 // Zdiff[100] = 90 / 75 // Zdiff[90] = |
| | | 30 | Prepreg FR-4.1 | | | | | 2,9 | |
| L2 | | 25 | | | | | | | |
| | | 100 | Core FR-4.1 | | | | | 3,8 | |
| L3 | | 25 | | | | | Ref1 | | |
| | | 30 | Prepreg FR-4.1 | | | | | 2,9 | |
| L4 | | 30 | 9µm copper foil + plating | Bottom-Layer | | | | | |
| | | 20 | Soldermask photosensitive, flexible | | | | | | |

Notes: Microvia execution stacked and staggered possible

# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

## Challenge Impedance design




**Important: Signal layer Top / Reference layer Inner2 resp. layer 3**

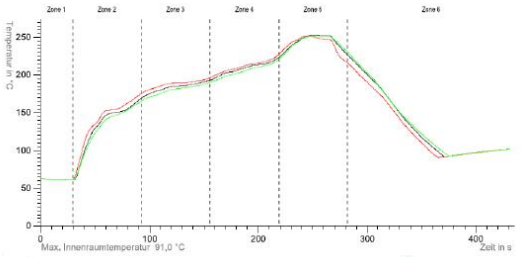
# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

A brief look at the reliability of the technology: qualification test results

## Reflow

TESTS:
- Resistance to Soldering Heat acc. AEC-Q200 / MIL-Std 202 Method 210
- Solderability acc. AEC-Q200 / J-Std 002
- 5-times Reflow WE internal Standard

FACTS:
- Full Computer Controlled
- 4 heating zones with hot air circulation
- Zone 1: Preheat Zone
- Zone 2: Preheat Zone
- Zone 3: Stabilization Zone
- Zone 4: Soldering Zone
- Zone 5: Cooling Zone
- Transport system speed : 0.05 – 0.8 m/min






## Temperature Test System VT7012-S2

TESTS:
- High Temperature Exposure acc. AEC-Q200 / MIL-Std 202 Method 108
- Thermal Shock acc. AEC-Q200 / JESD22 Method JA-104

FACTS:
- Cabinet volume of 120 l
- Dimensions: W470 x H410 x D650 mm
- Max. temperature change rate 11 K/min
- 2 chambers
- Cold chamber ->Temperature range -80 °C to +70 °C
- Warm chamber -> Temperature range -50 °C to +220 °C



**Reflow solder test: Drying 4h 120°C // Solder test acc. JEDEC 020C Peak 260°C // 6 repetitions**

**TCT Shock test: -55°C / +150°C // dwell time -55°C 15 minutes // change 15 seconds // dwell time +150°C 15 minutes**

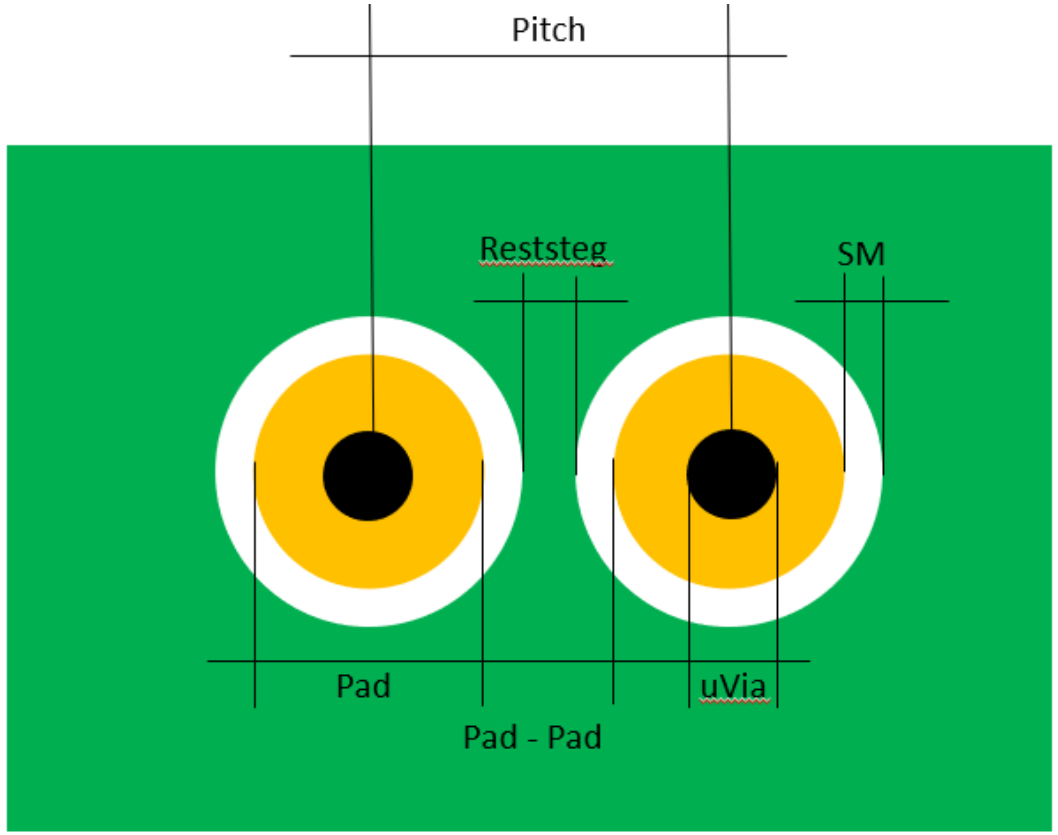
# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

Modification of parameters

- modified designrules of the PCB manufacturer
  - Pad diameter reduction
  - Reduction of the solder resist residue
  - Use of µVia in pad
  - Use of 75 µm/75 µm lines-space

**Caution!**

Here you deviate from the recommended component manufacturer specifications and should carefully examine the assembly, soldering technology and subsequent processes.

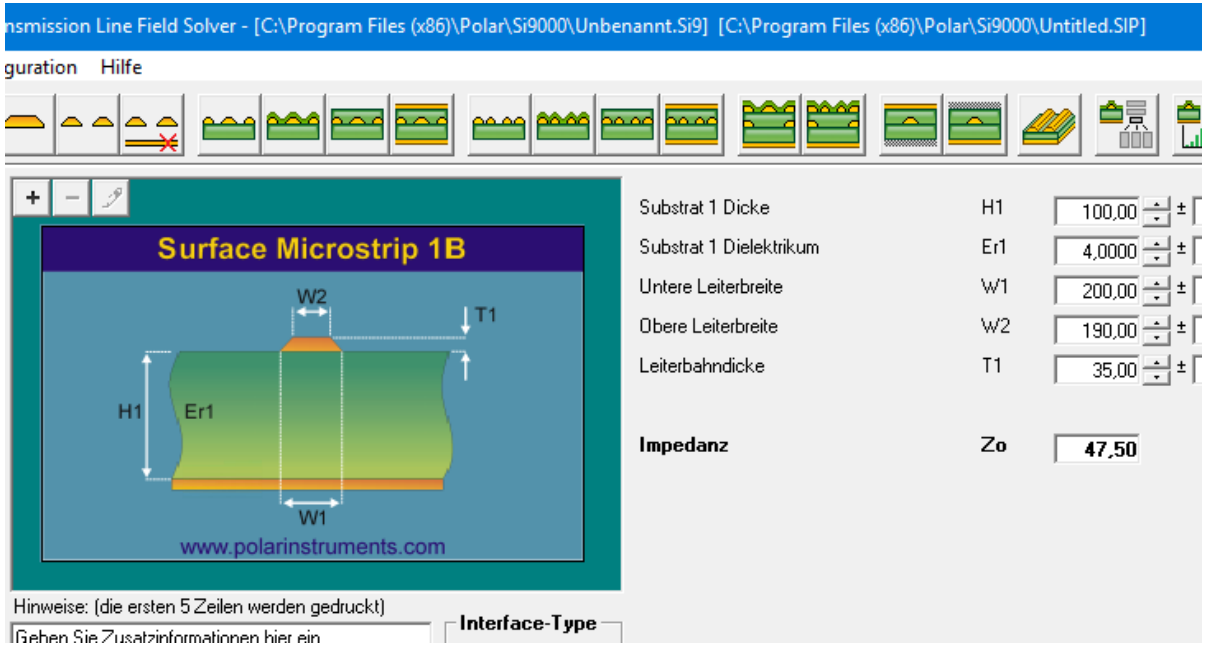



| Pitch [um] | Pad [um] | SM [um] | Reststeg [um] | uVia [um] | Pad-Pad [um] | L/S [um] |
|---|---|---|---|---|---|---|
| 350 | 215 | 35 | 65 | 85/215 | 135 | 75/75 |

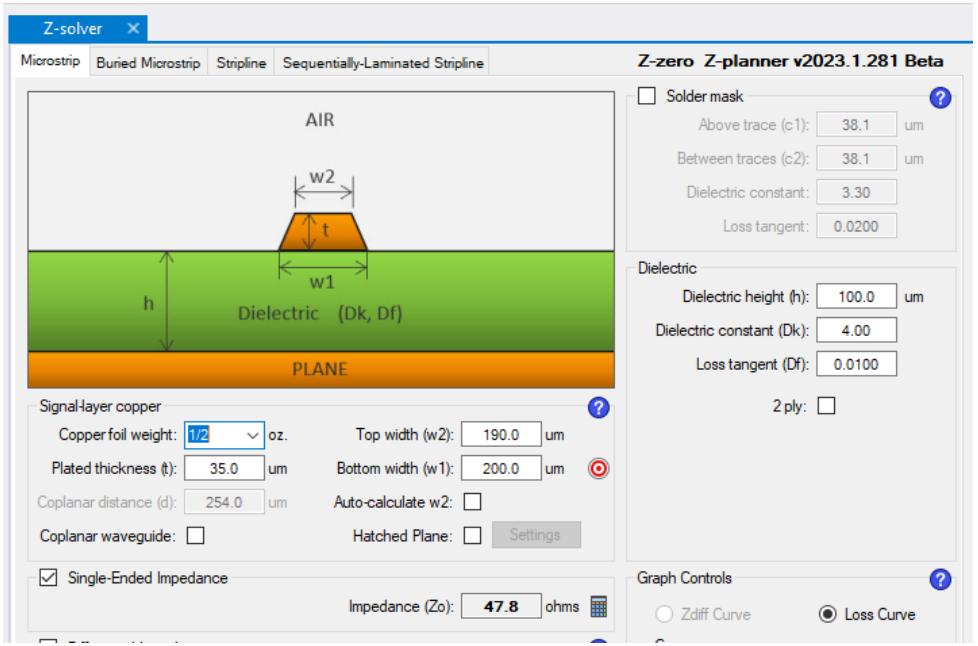
# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

## Impedance controlled traces

- The width of the head and foot of the trace are specified for the impedance calculation.
- Which value does the designer enter in the tool?
  -> according to the IPC specification, the foot, i.e. 200 µm, is specified, since this parameter can also be checked optically




Screenshot of Polar SI9000

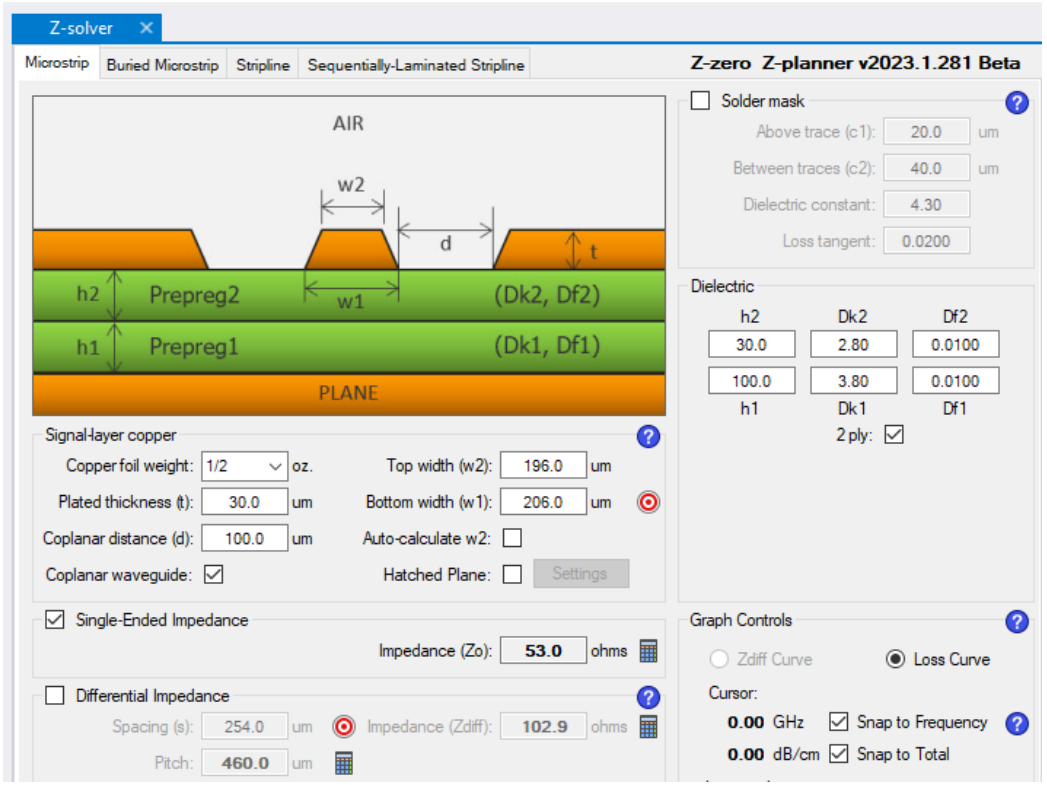



Screenshot of Siemens Z-Solver

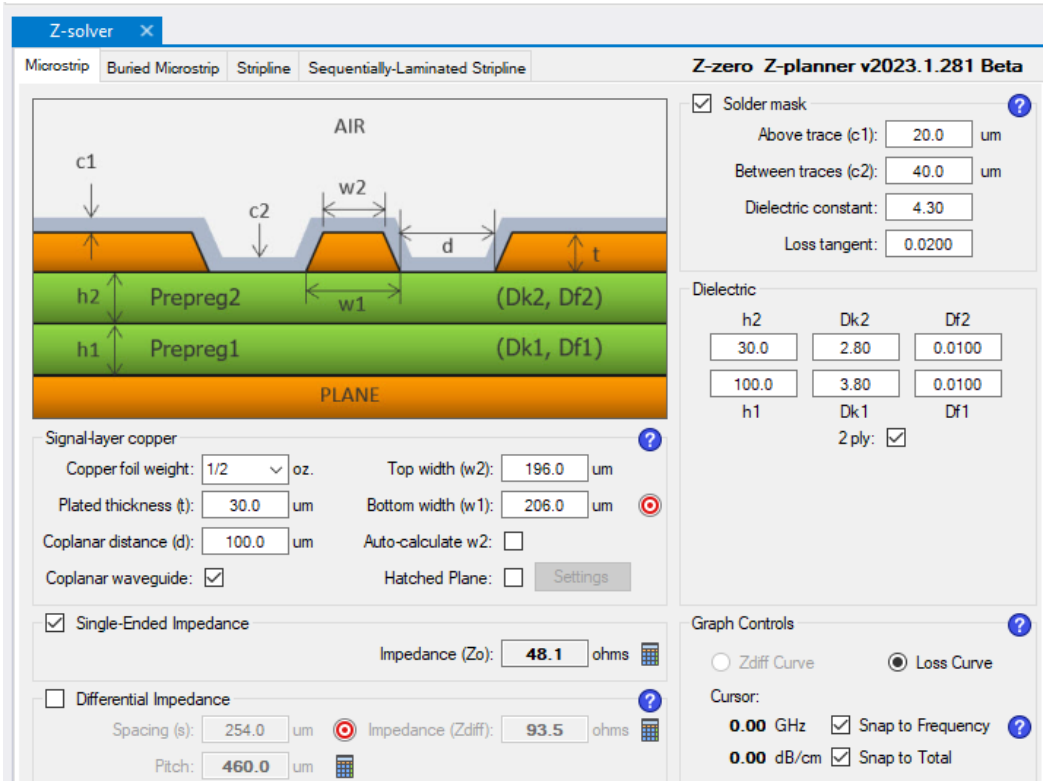
# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

## 50 Ohm Single-Ended (RF-antenna feed line)

- you have to take in account if the rf-track is realized with or without solder resist
- according to that the parameters need to be tuned to the right value




50 Ohm Single-Ended (without solder resist) -> here 53,0 Ohm

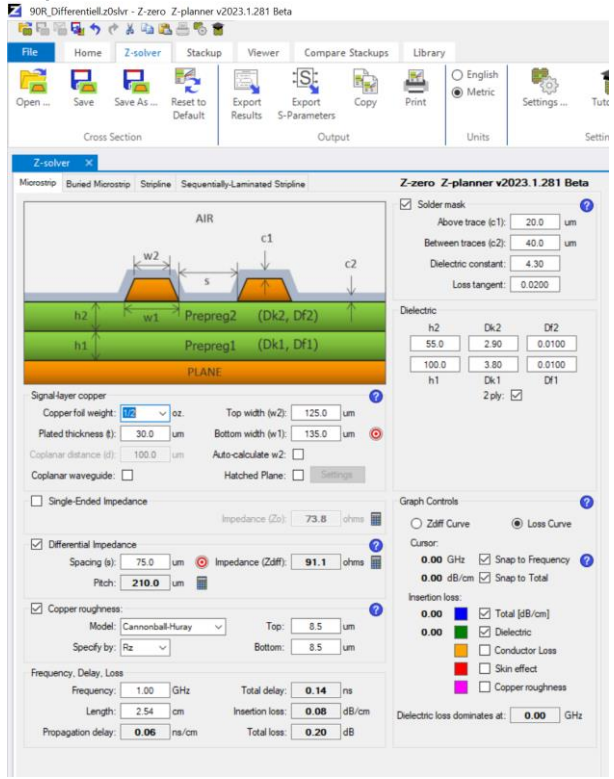



50 Ohm Single-Ended (with solder resist) -> here 48,1 Ohm

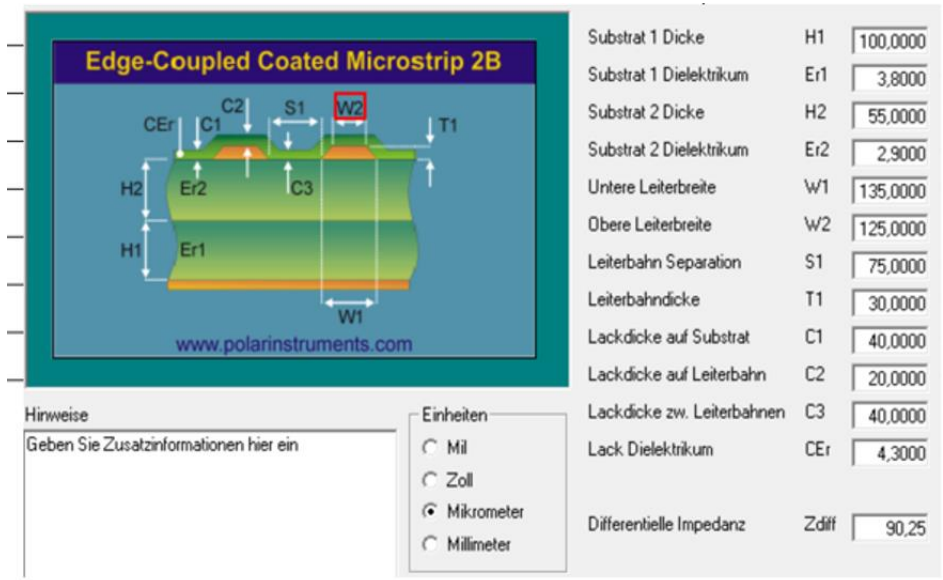
# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

## Example 90 Ohm differential pairs

- For 90 Ohm lines, the track width from the calculation corresponds to approx. 135 µm and must be entered in the EDA tool.
- The etching angle (trapezoidal shape) results in 135 µm at the base, i.e. the side facing the laminate. The conductor head then has a width of approx. 125 µm.
- In order to get an etching compensation, the CAM of the circuit board manufacturer adds approx. 30 µm. Thus, 165 µm are set in the photoresist for the exposure.




diff. 90 Ohm-tracks in Z-Solver




diff. 90 Ohm-tracks in SI9000

# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

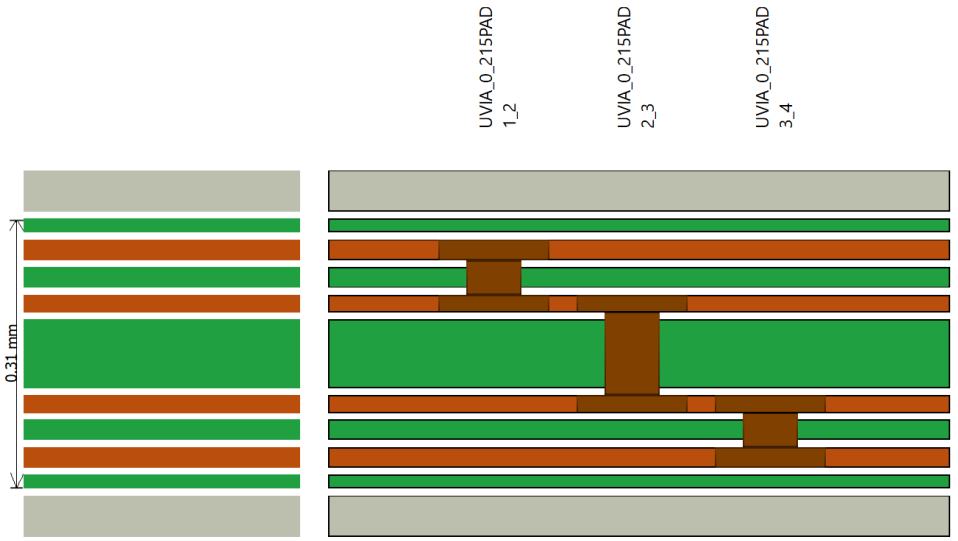
## Layer Stack-Up(using the example of Allegro/Orcad

Primary

| Row No. | Objects | | Types | | Thickness | Physical | | Embedded | Signal Integrit | |
|---|---|---|---|---|---|---|---|---|---|---|
| | # | Name | Layer | Layer Function | Value mm | Layer ID | Material | Embedded Status | Conductivity mho/cm | Dielectric Constant |
| * | * | * | * | * | * | * | * | * | * | * |
| 1 | | | Surface | | | | | | | 1 |
| 2 | | | Dielectric | Dielectric | 0.02 | | Soldermask | | 0 | 4.3 |
| 3 | 1 | TOP | Conductor | Conductor | 0.03 | 1 | Copper | Not embedded | 596000 | 1 |
| 4 | | | Dielectric | Dielectric | 0.03 | | Fr-4 | | 0 | 2.9 |
| 5 | 2 | LAYER2 | Conductor | Conductor | 0.025 | 2 | Copper | Not embedded | 596000 | 1 |
| 6 | | | Dielectric | Dielectric | 0.1 | | Fr-4 | | 0 | 3.8 |
| 7 | 3 | LAYER3 | Conductor | Conductor | 0.025 | 3 | Copper | Not embedded | 596000 | 1 |
| 8 | | | Dielectric | Dielectric | 0.03 | | Fr-4 | | 0 | 2.9 |
| 9 | 4 | BOTT... | Conductor | Conductor | 0.03 | 4 | Copper | Not embedded | 596000 | 1 |
| | | | Dielectric | Dielectric | 0.02 | | Soldermask | | 0 | 4.3 |
| | | | Surface | | | | | | | 1 |

- Layer structure with material-specific parameters such as εr, copper and prepreg thickness taken from the specifications of the PCB manufacturer.
- Ideally, the layer structure can be downloaded in digital format from the website for the respective EDA-tool.

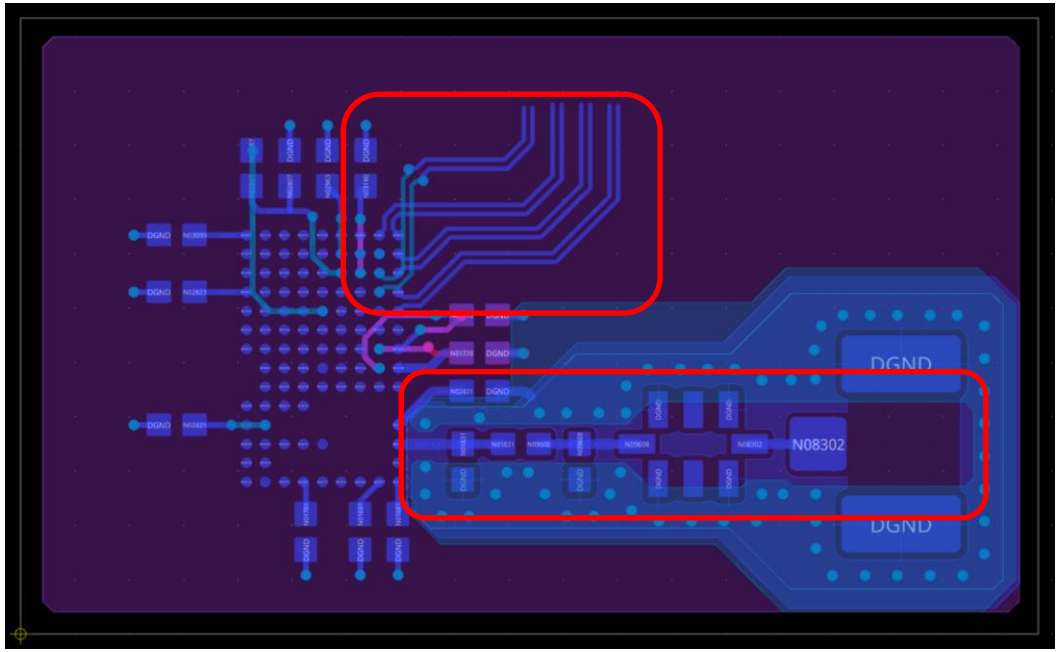
- Strategy of copper filled microvias
- Thanks to the copper filling technology, the vias can be designed staggered or stacked

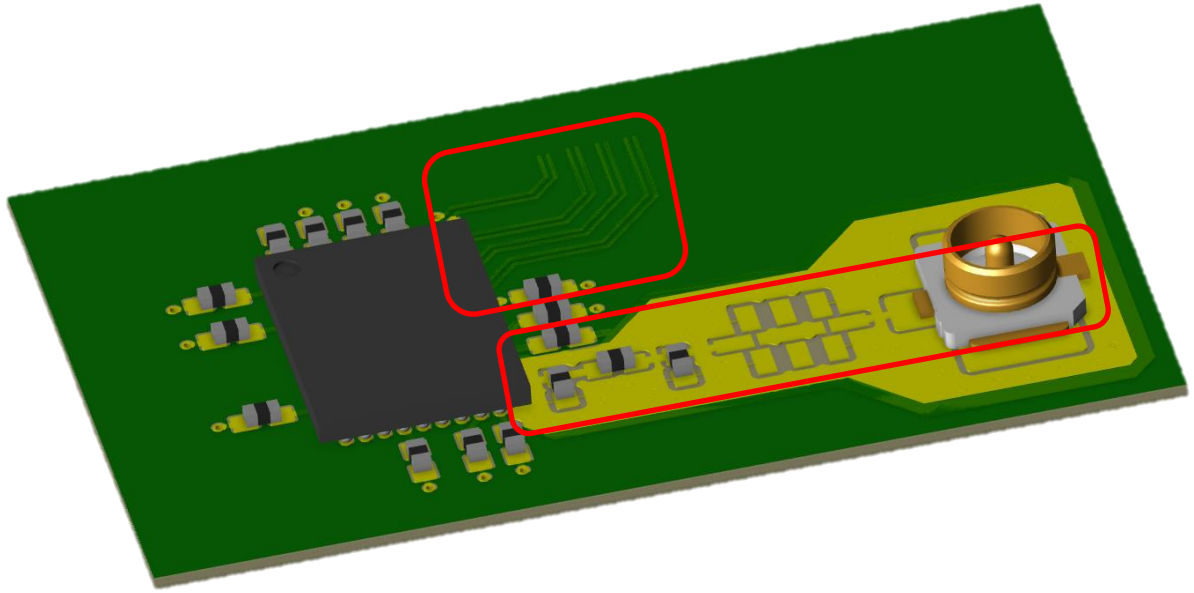


# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

Demo placement of some components

- BGA-component with 350 µm pitch and external components



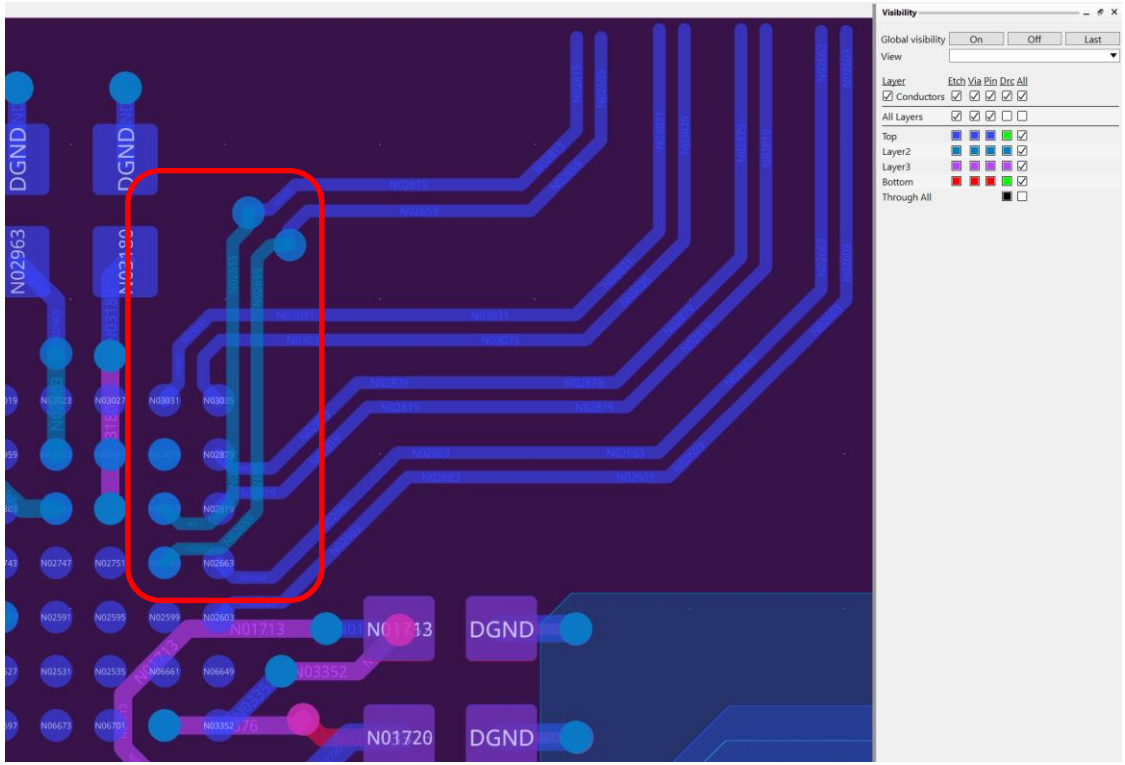



- differential 90 Ohm impedance
- Single-Ended 50 Ohm track as antenna feed line without covering with solder resist

# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

Layer change at differential lines

- in order to route the differential pairs from the inner area of the BGA, a layer change to layer 2 must be done
- this reduces the distance to the reference layer, which reduces the impedance



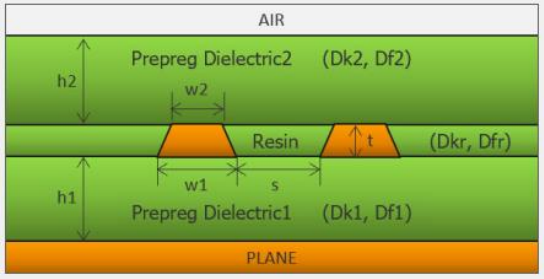

Cutout from the demo-placement

Primary

| Row No. | Objects # | Objects Name | Types Layer | Types Layer Function | Thickness Value mm | Physical Layer ID | Physical Material | Embedded Embedded Status | Signal Integrit Conductivity mho/cm | Signal Integrit Dielectric Constant |
|---|---|---|---|---|---|---|---|---|---|---|
| * | * | * | * | * | * | * | * | * | * | * |
| 1 | | | Surface | | | | | | | 1 |
| 2 | | | Dielectric | Dielectric | 0.02 | | Soldermask | | 0 | 4.3 |
| 3 | 1 | TOP | Conductor | Conductor | 0.03 | 1 | Copper | Not embedded | 596000 | 1 |
| 4 | | | Dielectric | Dielectric | 0.03 | | Fr-4 | | 0 | 2.9 |
| 5 | 2 | LAYER2 | Conductor | Conductor | 0.025 | 2 | Copper | Not embedded | 596000 | 1 |
| 6 | | | Dielectric | Dielectric | 0.1 | | Fr-4 | | 0 | 3.8 |
| 7 | 3 | LAYER3 | Conductor | Conductor | 0.025 | 3 | Copper | Not embedded | 596000 | 1 |
| 8 | | | Dielectric | Dielectric | 0.03 | | Fr-4 | | 0 | 2.9 |
| 9 | 4 | BOTT... | Conductor | Conductor | 0.03 | 4 | Copper | Not embedded | 596000 | 1 |
| | | | Dielectric | Dielectric | 0.02 | | Soldermask | | 0 | 4.3 |
| | | | Surface | | | | | | | 1 |

Since the layer structure of the printed circuit board is symmetrical, there are two possible solutions:

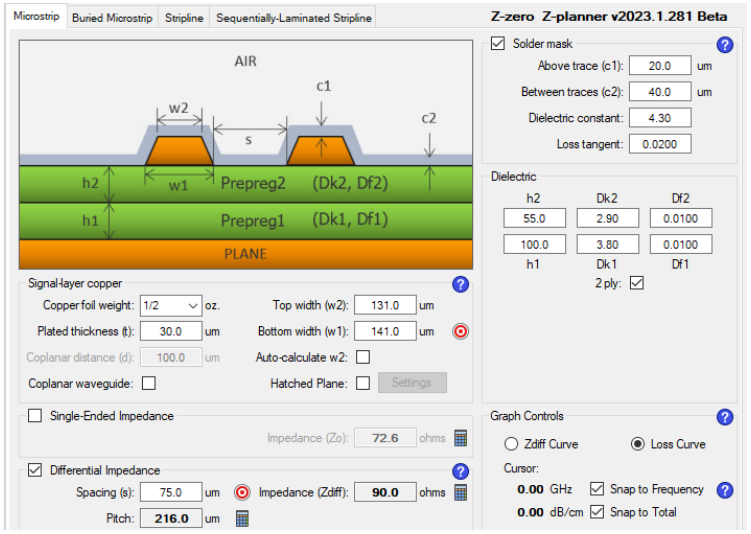
- you adjust the track width and spacing to achieve the required impedance
- the bottom layer is used as the reference layer, but it must be noted that a buried microstrip structure is created and other parameters must therefore be taken into account



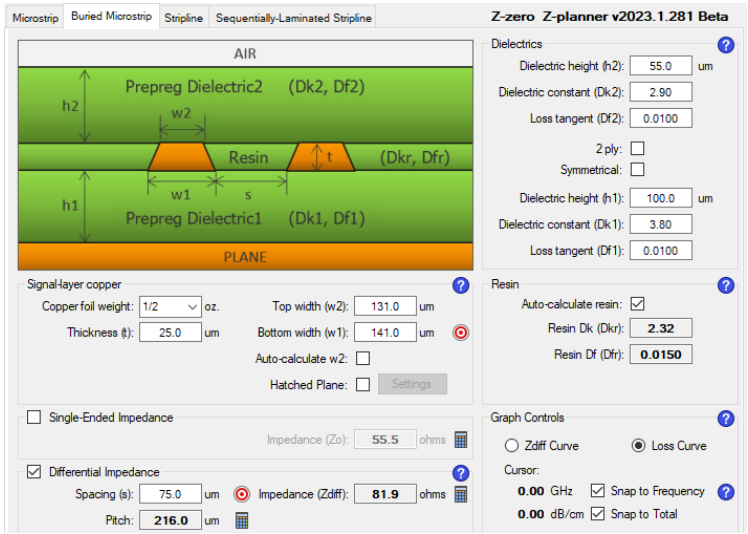
# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

90 ohms differential impedance module

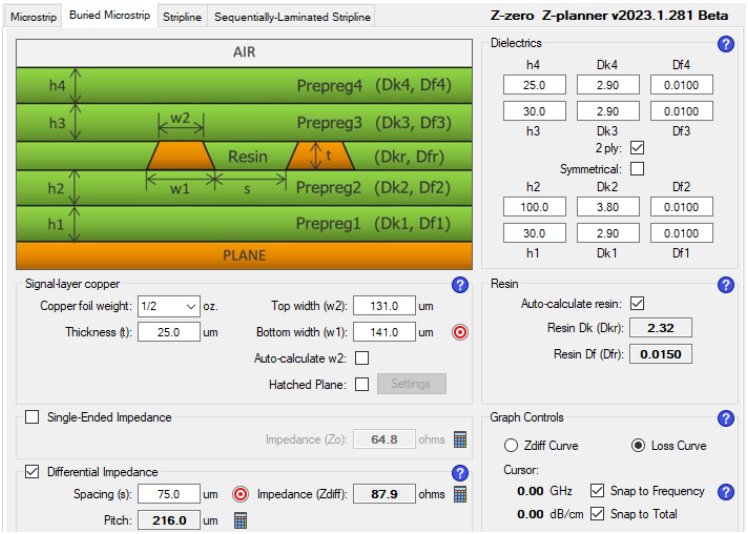
- To get a feeling for the impedance changes, the differential 90 ohm microstrip module is divided into a buried microstrip module with reference to layer 3 (100 µm spacing) and a buried microstrip module with reference to the bottom layer (130 µm spacing). The line-space parameters remain.



original impedance module (90 Ohm)



buried impedance module with reduced spacing (81,9 Ohm)



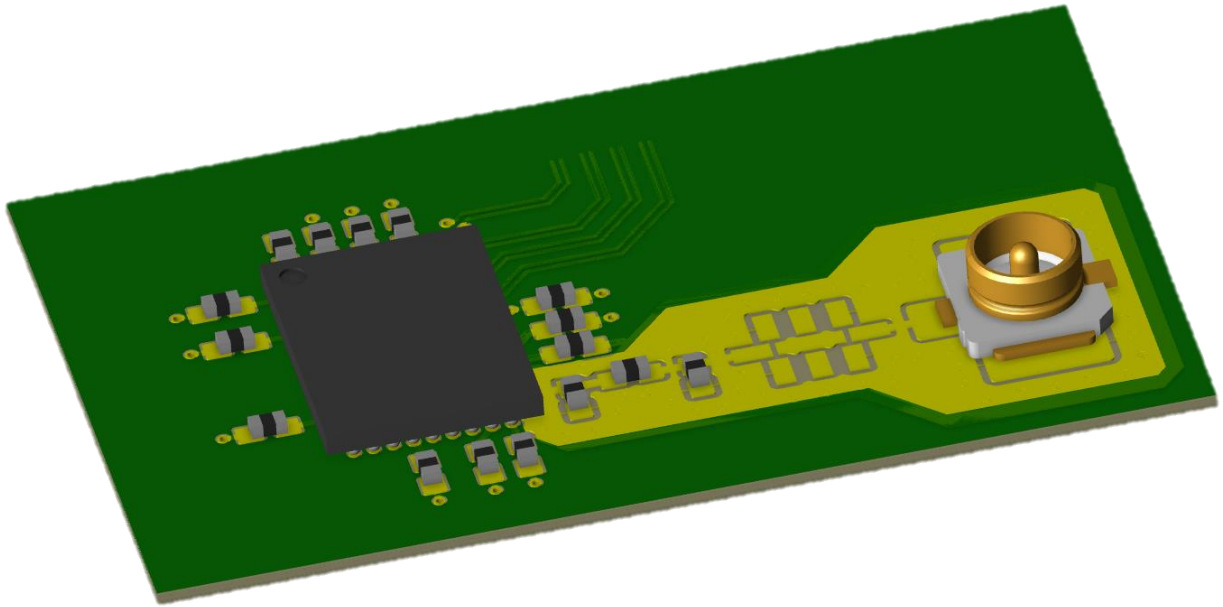
buried impedance module with 130µm (87,9 Ohm)

- As it can be seen from the results, the distance to the reference layer has a greater influence on the impedance than the covering height with resin/glass.

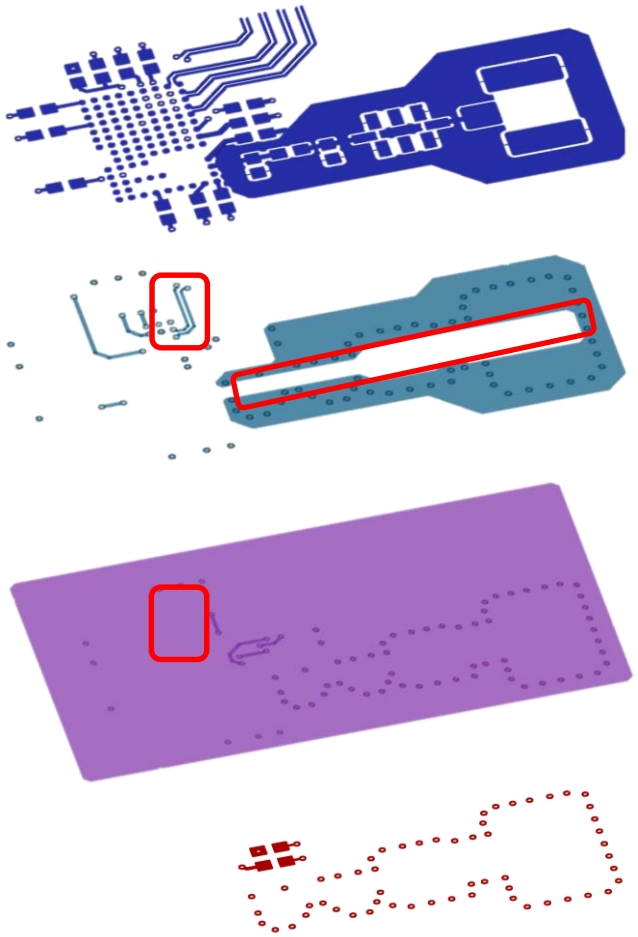
# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

Layer stack of the demo placement

- In the illustration of the individual layers, you can see the gap on layer 2 that is required to use layer 3 as a reference
- In a further step, the area under the differential line pair on layer 2 would have to be cleared in layer 3 and a reference plane would have to be inserted on the bottom layer. The line space parameters then have to be adjusted according to the simulation results.



Demo placement

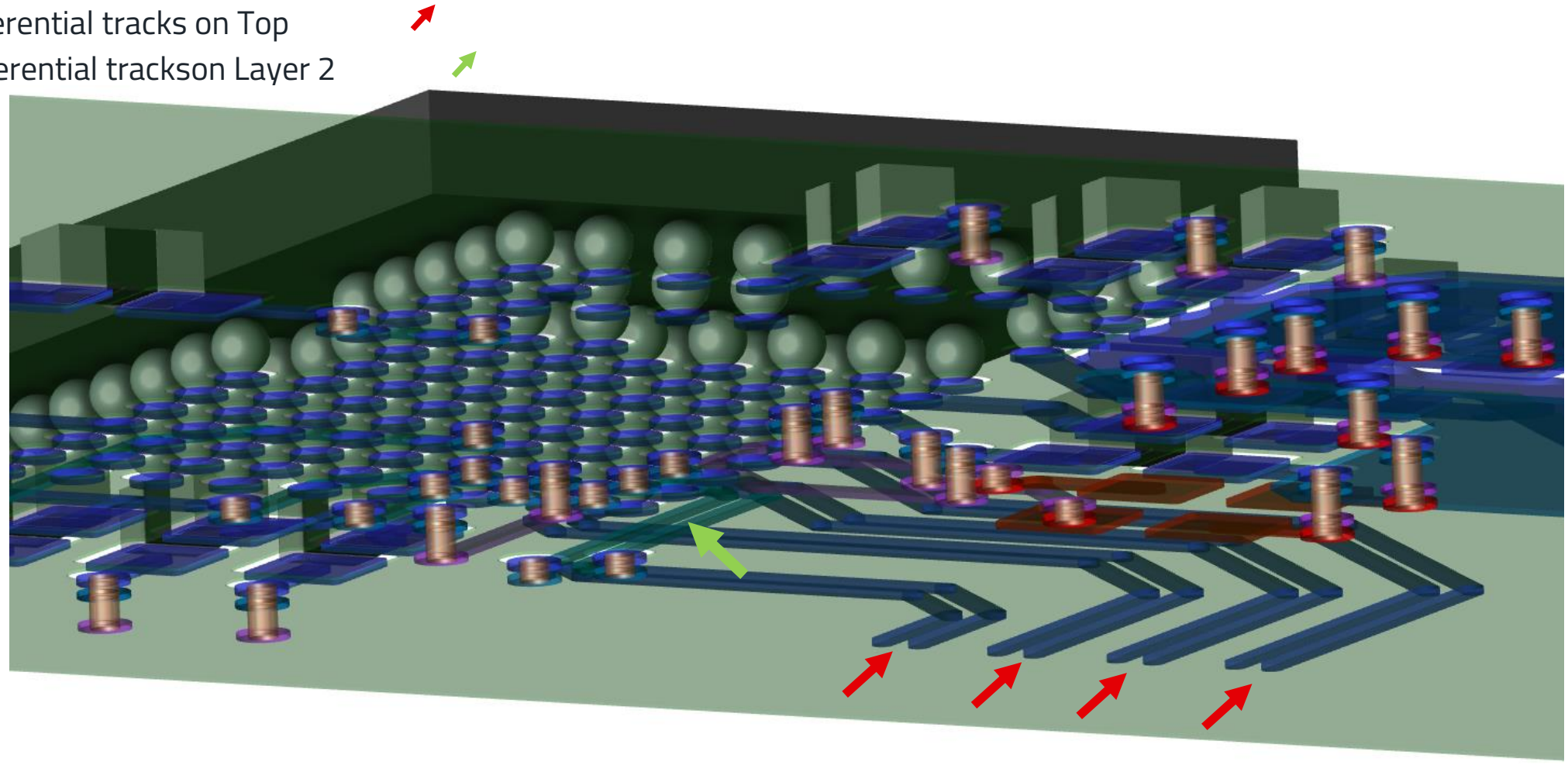


- Top
- Layer 2
- Layer 3
- Bottom

# FAN OUT OF A BGA PITCH 0.35 MM – THIS IS HOW IT WORKS!

Routing unter dem BGA

- stacked micro-vias
- differential tracks on Top
- Differential trackson Layer 2



# THANKS FOR YOUR ATTENTION

Fan out of a BGA Pitch 0.35 mm –
This is how it works!