

Anniversary webinar: what counts

Webinar March 01, 2016, 11:00 a.m. CET

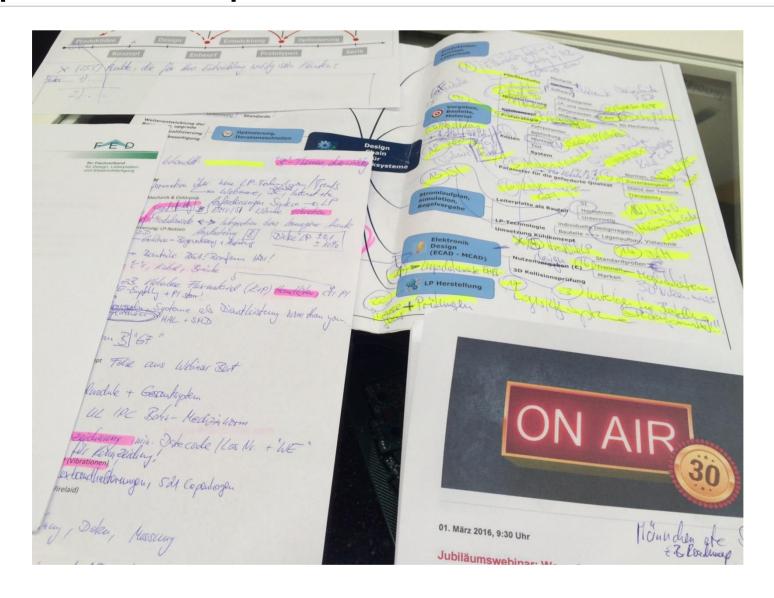
Speaker: Andreas Schilpp



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Approach to the topic



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Approach to the topic

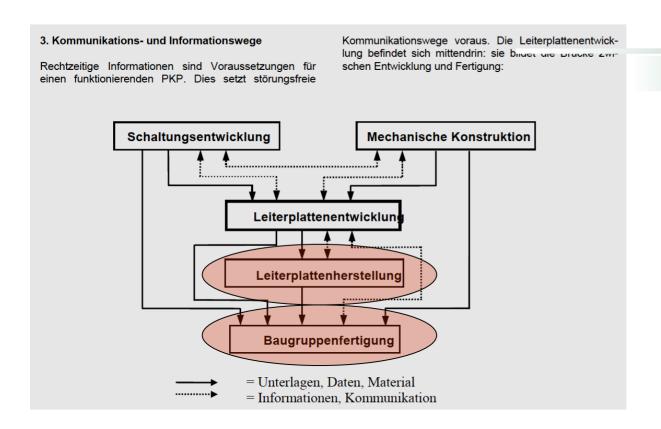
- value chain
- PCP product creation process
- Design Chain



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Approach to the topic





Ihr Fachverband für Design, Leiterplattenund Elektronikfertigung

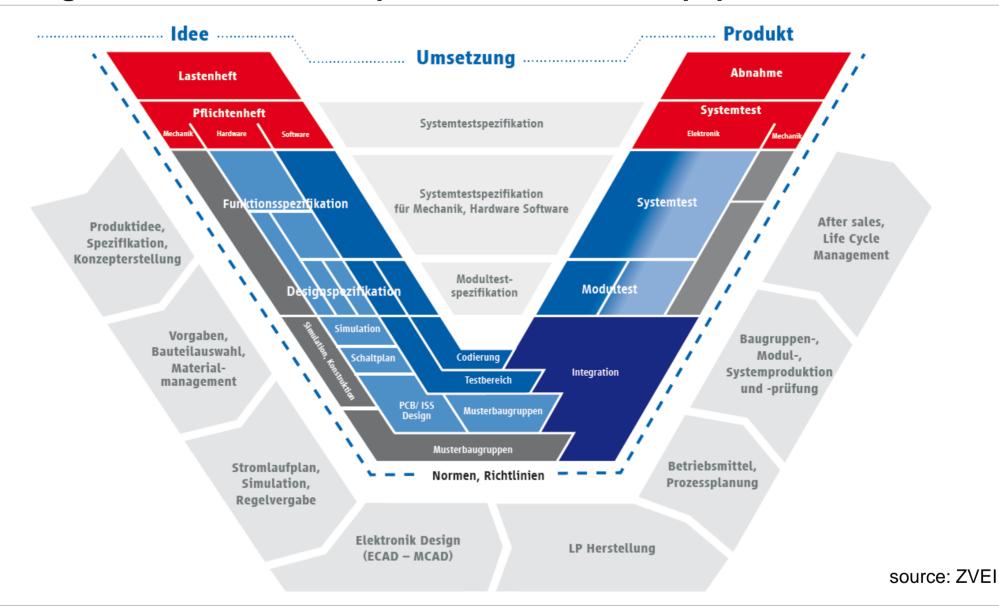
FED-22-02A

FED-Designrichtlinie

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Design Chain of the development of electronic equipment



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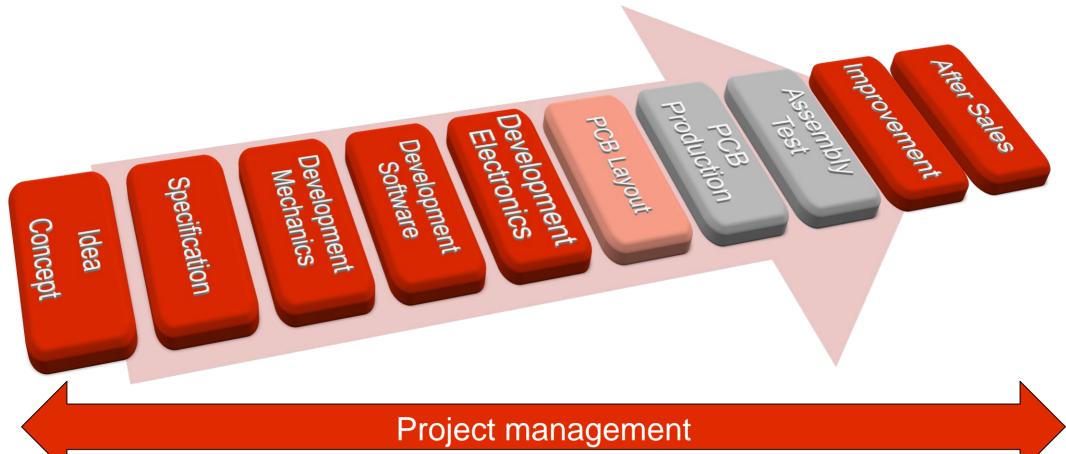
Design Chain of the development of electronic equipment



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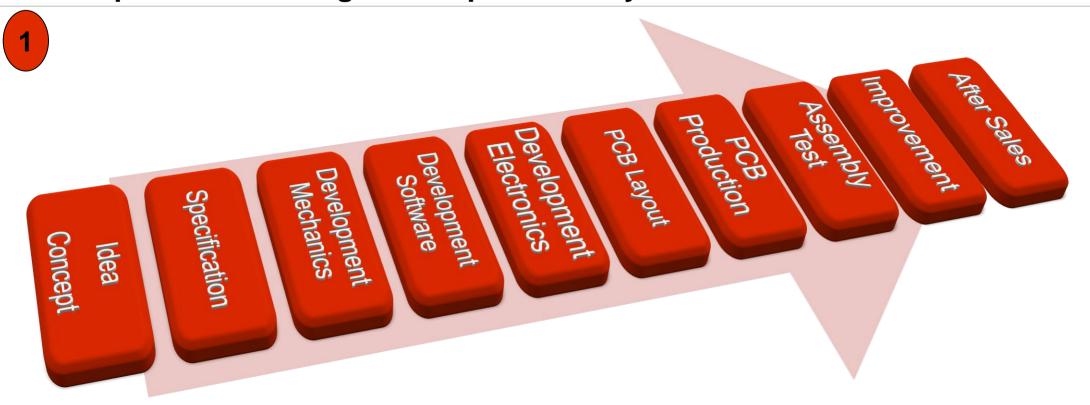


Design Chain of the development of electronic equipment



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Ongoing Information Aquisition and Training about Technologies, Components, Tools etc.

Fairs, Webinars, Design Conferences, Design Guides, technical articles, Internet

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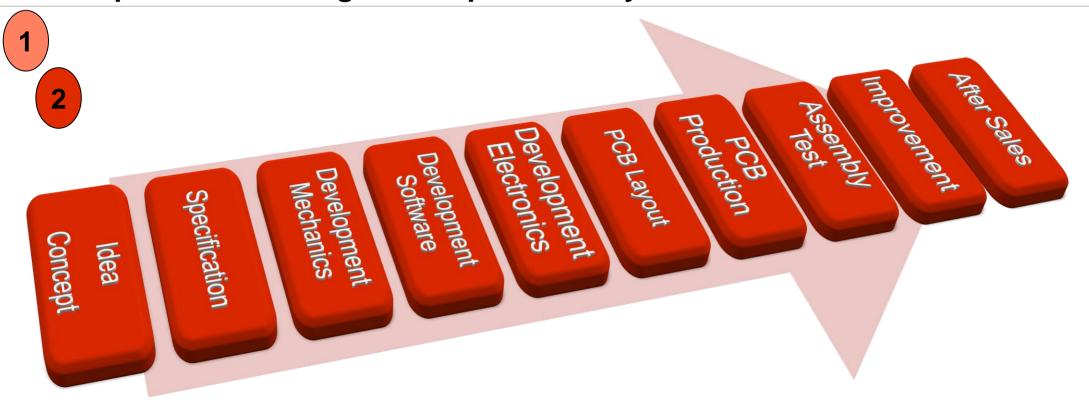
Information source Designguides





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Product idea, Concept and Technology Choice

Target market, ramp-up

Modular Approach

←→Integrated Approach

Availability, 2nd source

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Modular Approach ⇔ Integrated Approach

Power Board

102 mm x 95mm 8 Layer standard FR4 Current Cost ~ £17

Connector Board

102 mm x 104mm 10 layer standard FR4 Controlled impedance Current Cost ~ £25

FPGA Board

102 mm x 110mm 16 High Tg FR4 Controlled impedance Current Cost ~ £43

Sensor Board

90 mm x 95mm 10 layer standard FR4 Controlled impedance Current Cost ~ £25

PWR/Connector Board

102 mm x 104mm 16 layer high Tg FR4 Controlled impedance

FPGA Board

102 mm x 110mm 16 Layer high Tg FR4 Controlled impedance

PWR/Connector Board

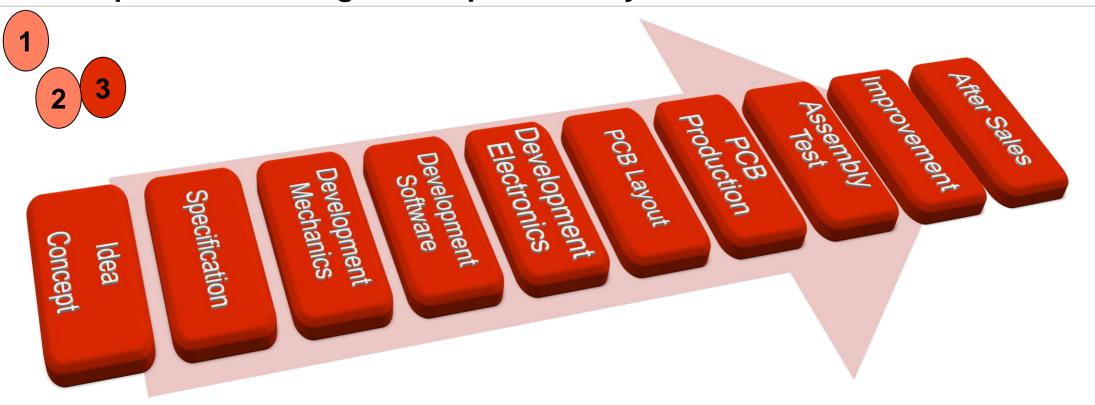
90 mm x 95mm 16 layer high Tg FR4 Controlled impedance



Added flex interconnect 4 layers, signal, GND, signal, POWER

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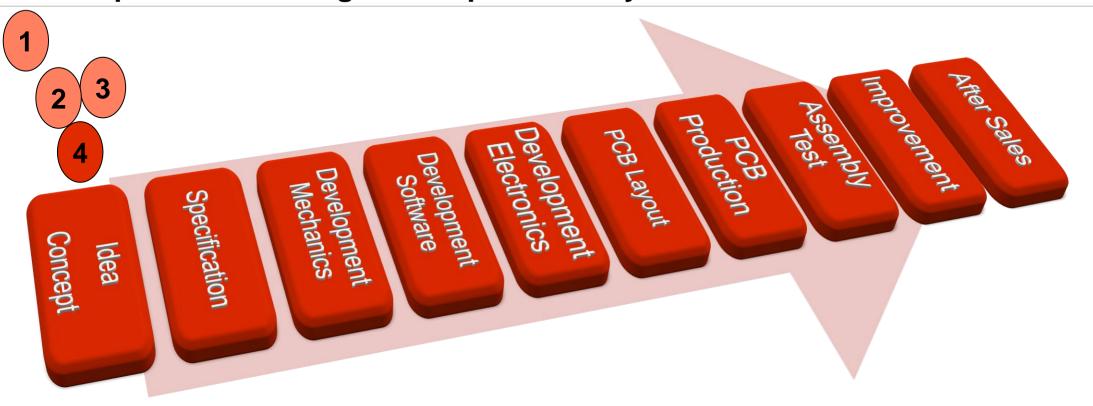
Functional Specifications for Mechanics & Elektronics & Software, Size

Requirements for the PCB derived from the System
Start-up may be only "DIN-A4 page" → high risk of late engineering changes!

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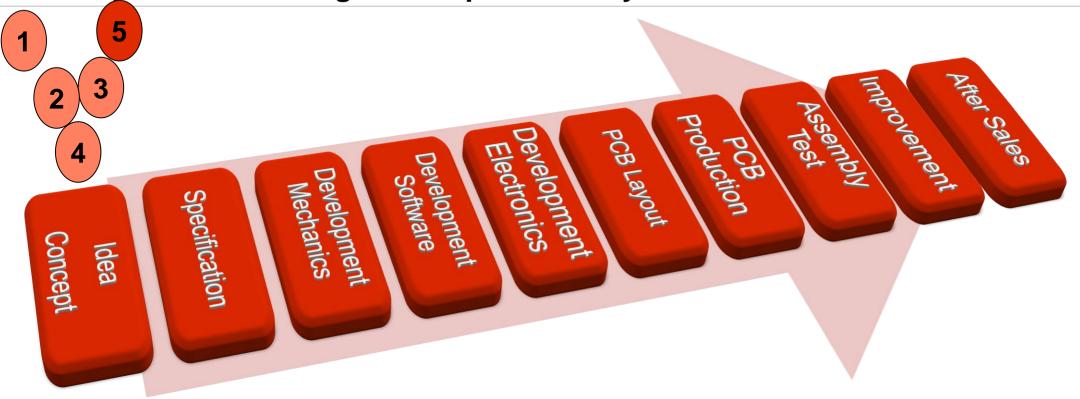


Standards und Legal Regulations

Impact from the System onto the PCB

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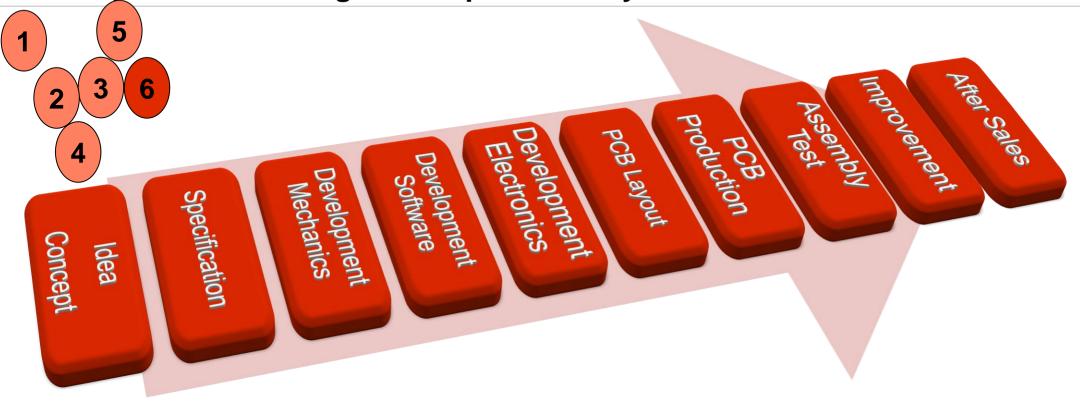
Mission profile, Reliability Requirements, Life Span

Impact on Components and PCB

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Design specifikation, Mechatronics und Miniaturisation

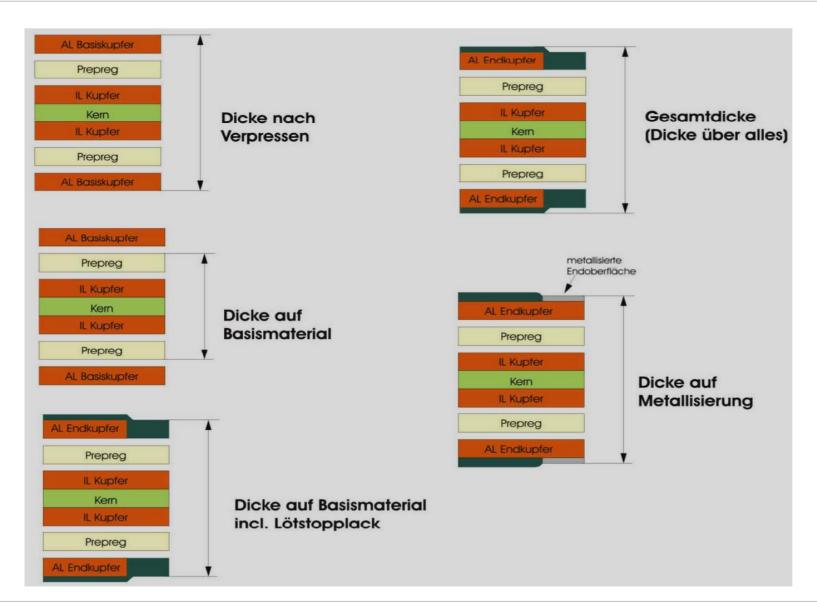
Thickness of the PCB – Definitions and Tolerances Approach for Miniaturisation of the PCB

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different Definitions of PCB thicknesses

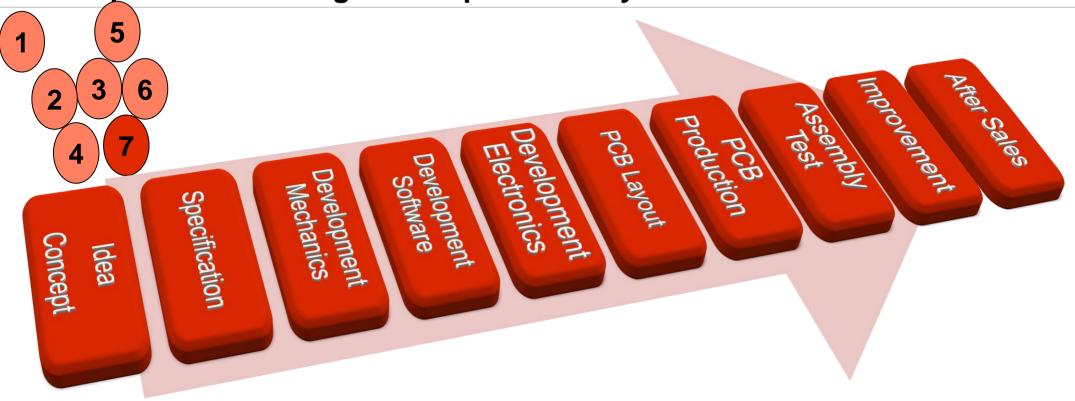


Tolerances:

typical ±10% after Lamination

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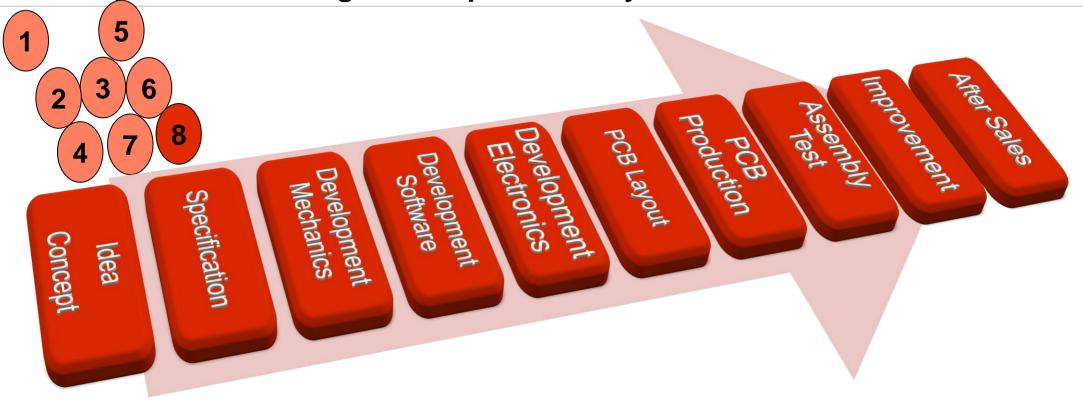




Estimation of needed Time for Layout and Production of the PCB bare board

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Mechanics, Assembly and Fastening of the PCB, Shock and Vibration

Options of Fixation

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Mechanics: Fastening of a PCB – Shock and Vibration

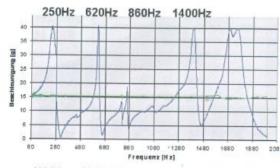


Abbildung 12-15: Experimentell bestimmte Eigenfrequenzen und Modell der simulierten Baugruppe

In einer ersten Berechnung wurden die Bedingungen für eine Befestigung der Baugruppe mit nur vier Schrauben analysiert. Abbildung 12-16 zeigt die berechneten Schwingungsformen für die vier ermittelten Eigenfrequenzen.

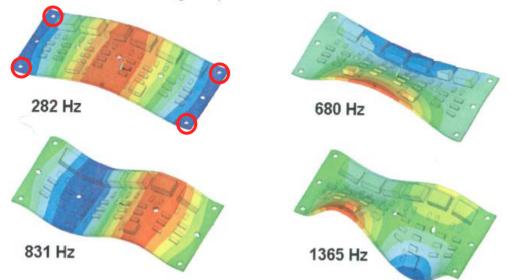
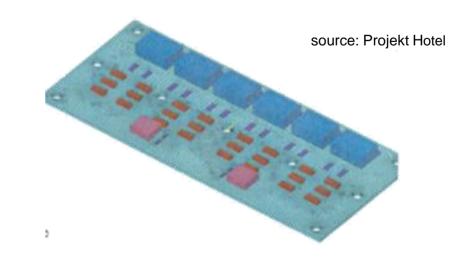


Abbildung 12-16: Eigenfrequenzen der simulierten Baugruppe mit vier Befestigungsschrauben



Fixing with 9 screws:

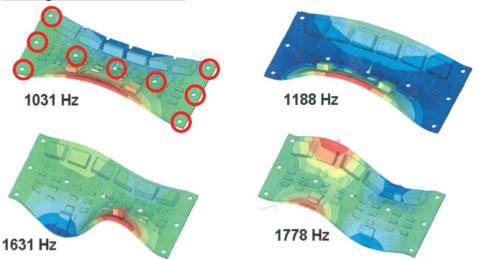


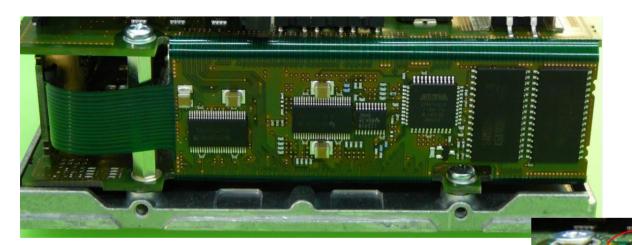
Abbildung 12-18: Berechnung der Eigenfrequenzen der simulierten Baugruppe mit neun Befestigungsschrau-

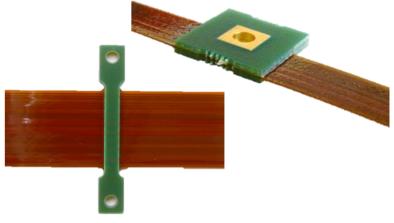
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Mechanics: Fastening of a PCB – Shock and Vibration

NO fixation of one rigid area

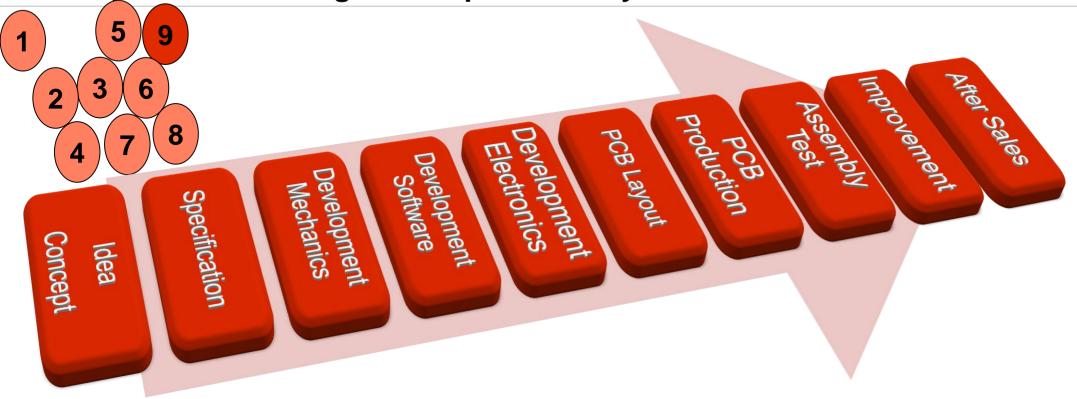




... leads to resonance and destruction even with Rigid-Flex!

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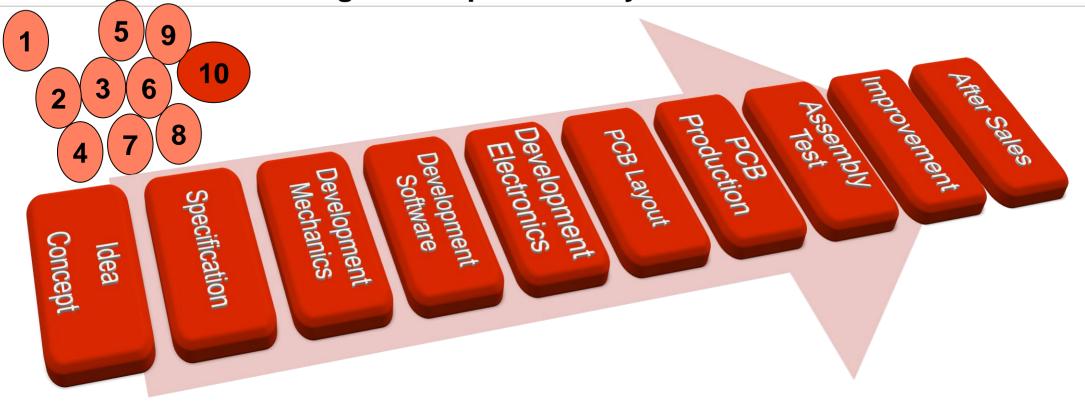
EMC: interfaces

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Proof of Concept regarding emission and interference (less is better)

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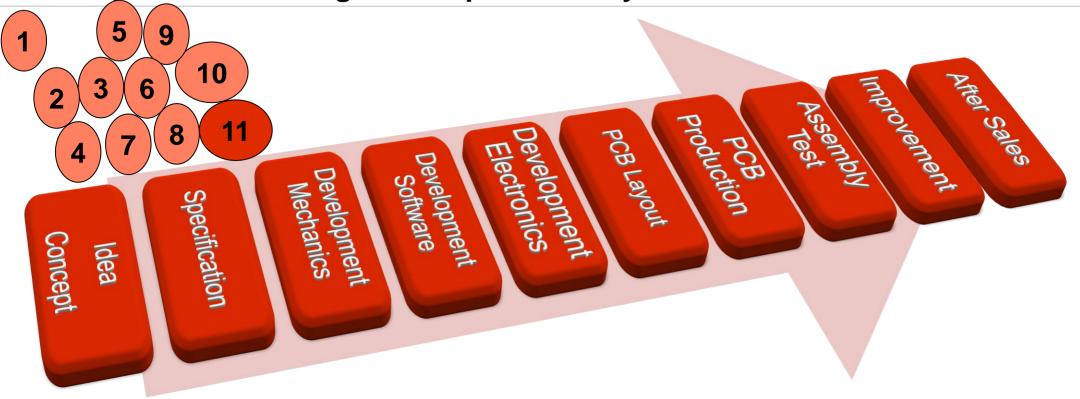
Signal integrity

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Simulation, Documentation (also for a "simple" Multilayer)

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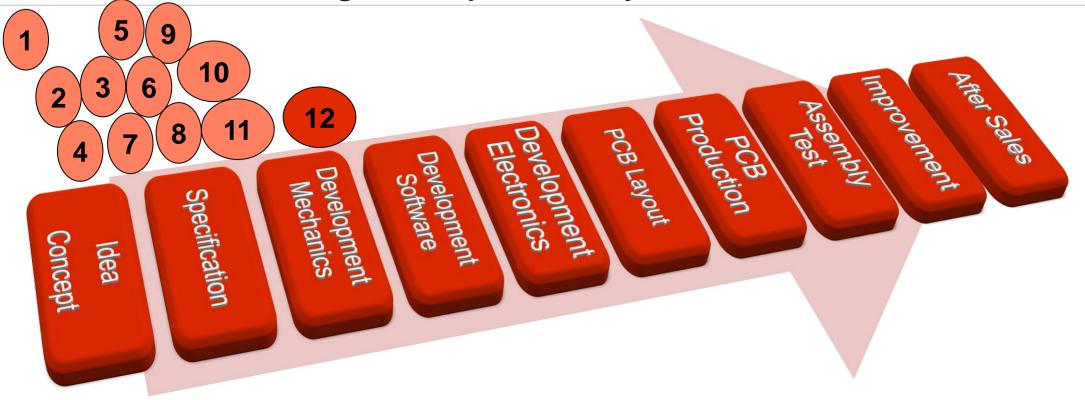
Ampacity

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According to IPC-2152
Options Thick copper technology ⇔ partial Thick copper technology

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Thermal Design

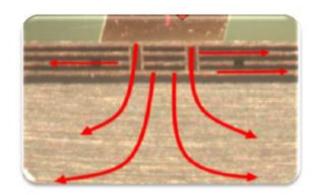
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Simulation based on Gerber data, Adaption of PCB Technology

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Simulation thermal Design - Variants



Options on PCB basis:

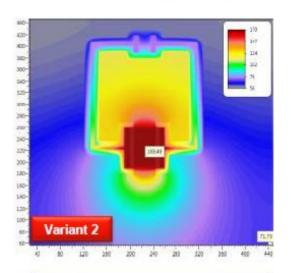
- Heat dissipation using vias
- Heat spreading using planes and heatsinks glued onto the PCBs

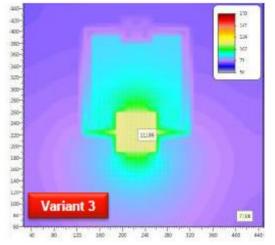
Target:

- Lowering of temperature at the component
- Avoiding critical temperatures inside of the component and unit
- Extention of lifetime and ensure of long term reliability of the unit

At threshold a thermal simulation in preliminary stages is recommended

Thermal Simulation

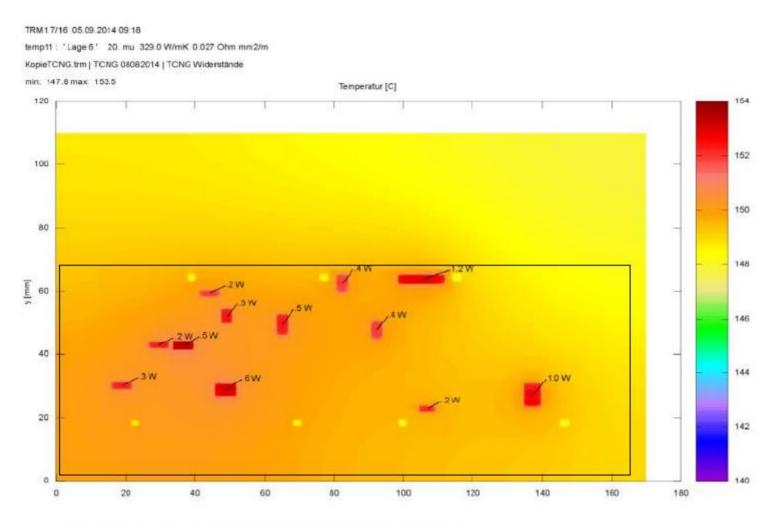




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Simulation heat dissipation of Polymer Resistors



Ambient temperature: 140°C

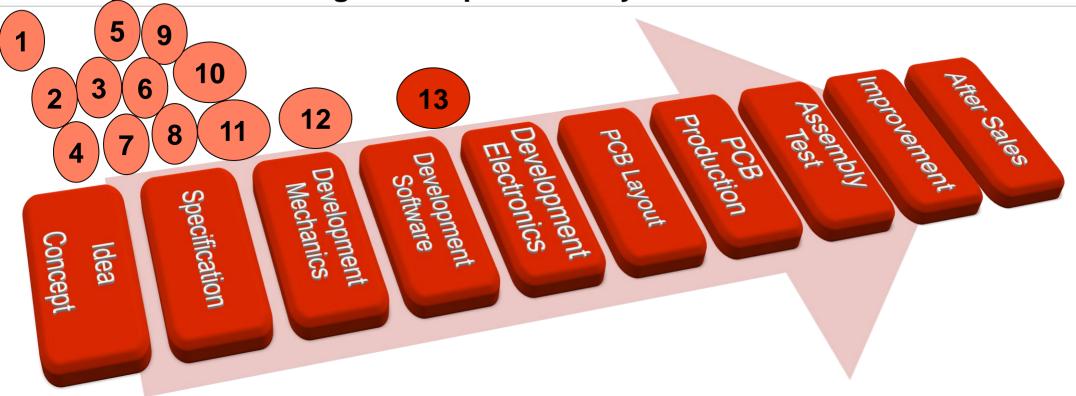
Max. temperature at resistor: 153.5 °C

Power in accordance with customer specifikation

Thermal Simulation - Würth Elektronik CBT Product Management

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System cost

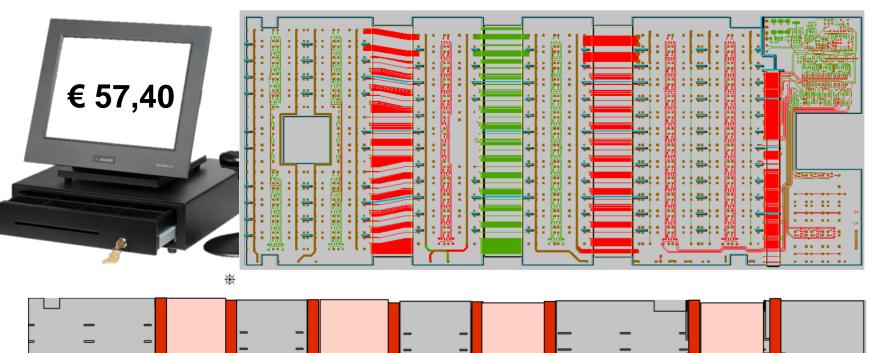
13

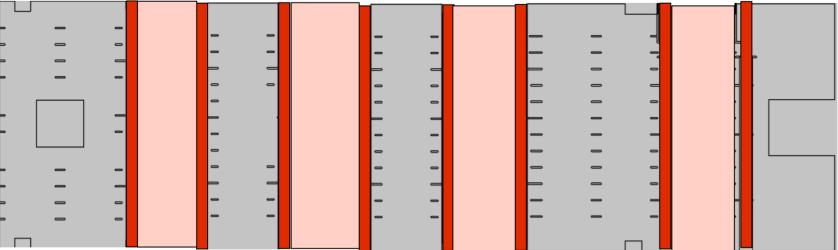
Ball park quotes, System cost estimations

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System cost comparison: modular - integrated







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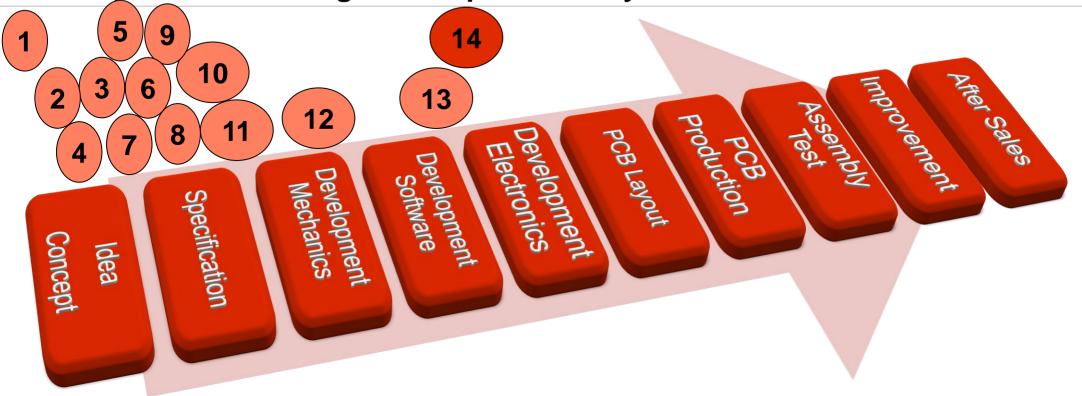


System cost comparison: modular - integrated

	rigid pcbs with cables and connectors		Semiflexible pcb		
balance sheet					
	100 pcs	1.000 pcs	100 pcs	1.000 pcs	Remarks
a) pcb price	58,50 €	40,50€	55,90€	45,50 €	pcbs from Europe
b) FFC cables, ZIF connectors	30,00€	13,00€	-	-	EMS Sweden
c) for this SMD assembly AOI	2,00€	1,50 €	-	-	EMS Sweden
d) final assembly	2,00€	1,50 €	-	-	EMS Sweden
e) final test	1,50 €	1,00€	1,50 €	1,00€	EMS Sweden
sum of BoM and processing	94,00€	57,50 €	57,40 €	46,50 €	
			-39%	-19%	cost saving
additional cost factors:					
f) design for	5 pcbs		1 pcb		_
g) inventory control	17 components + 5 stencils 5 x 6 x 22 positions		1 component + 2 stencils 1 x 1 x 3 positions		
h) assembly expenditure					
i) test expenditure					
k) stock / logistics					_
l) Pin- and solder connections	312 ZIF-contacts + 312 solder joints		integrated Semiflex connection		Reliability

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Circuit diagram, Choice of Components

Impact on PCB Technology!

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Component with highest density determins PCB technology

Excerpts out of our HDI Designguide:

BGA 0.50 mm Pitch

Für 0.50 mm BGA Pitch müssen auf jeden Fall Feinstleiterstrukturen verwendet werden, wir empfehlen 75 um (3 mil). Zusätzlich ist es erforderlich, die Microviapadoröße. zumindest auf den Innenlagen, auf 275 um zu reduzieren. Für 75 um Feinstleiterstrukturen muss die Kupferendschichtdicke auf der Oberfläche auf ca. 25 um begrenzt werden.

Würth Elektronik empfiehlt die oben dargestellte Variante 1, bei der keine Leiterbahnen auf der Außenlage zwischen den BGA Pads hindurchgeführt werden. Damit können auf der Außenlage Feinstleiterstrukturen vermieden werden.

Variante 2 hat den Vorteil einer planaren Lötfläche (geringeres Risiko von Voiding) bei allerdings reduzierter Lötpadgröße.

Bei Variante 3 muss auch auf den Außenlagen mit 75 µm Strukturen gearbeitet werden, was den Fertigungsaufwand erhöht. Zusätzlich muss hier die Lötstoppmaskenfreistellung auf 35 um reduziert werden. Diese Variante kann allerdings möglicherweise helfen eine Microvialage einzusparen. Grundsätzlich hängt die Anzahl der erforderlichen Microvialagen, und damit der Lagenaufbau, von der Komplexität des Bauteils ab.

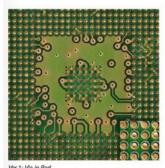
RGA 0 50 mm Pitch

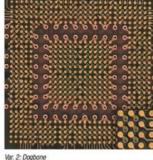
Fine line structures will definitely be required for a 0.50 mm pitch BGA, we recommend 75 um (3 mil). It will also be necessary to decrease the microvia pad size, at least on the inner layers, to 275 um. For 75 um fine line structures the final copper thickness on the surface is limited to approximately 25 um.

Würth Elektronik recommends variant 1 described above, without tracks between the solder pads on the outer layer. This avoids the need to use fine line structures on the outer

Variant 2 gives the advantage of a planar surface (lower risk of voiding), but with a reduced solder pad size.

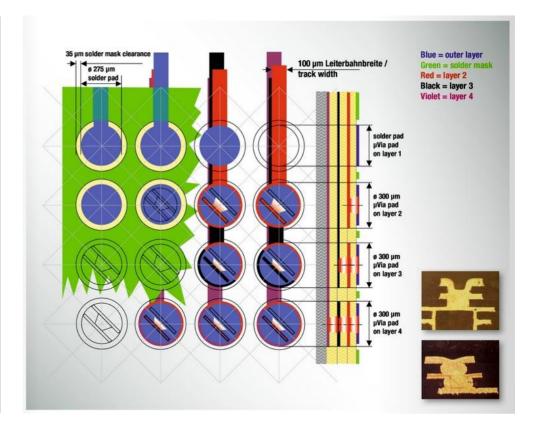
With variant 3, 75 um structures are needed on the outer laver as well. This increases the production effort and the production costs. Moreover, the solder mask clearance has to be reduced to 35 um. This variant could probably help to save one microvia layer. Generally the number of the microvia layers required, and the kind of stack-up, depends on the complexity of the component.







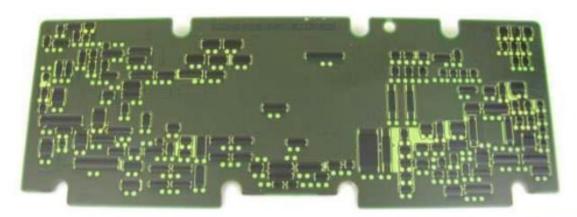




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Option: printed Components

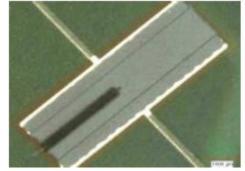


Tolerance of resistance value without laser trimming max. +/- 30%

With Laser Trimming

Process tolerance: down to +/- 1%

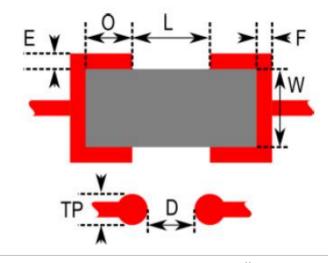
Entire product lifetime: +/- 5%





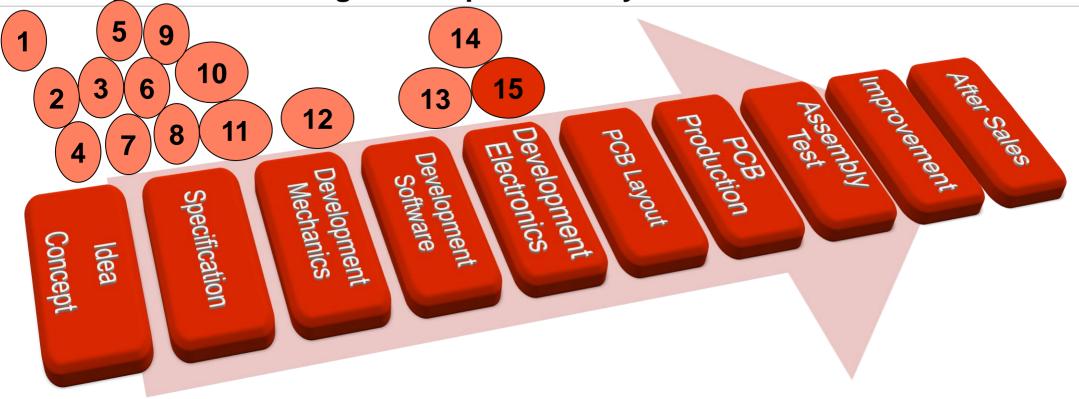
Traceability:

The laser trimming process can also enable perfect traceability by using binary coding on additionally designed resistors.



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Material Choice for the PCB bare board

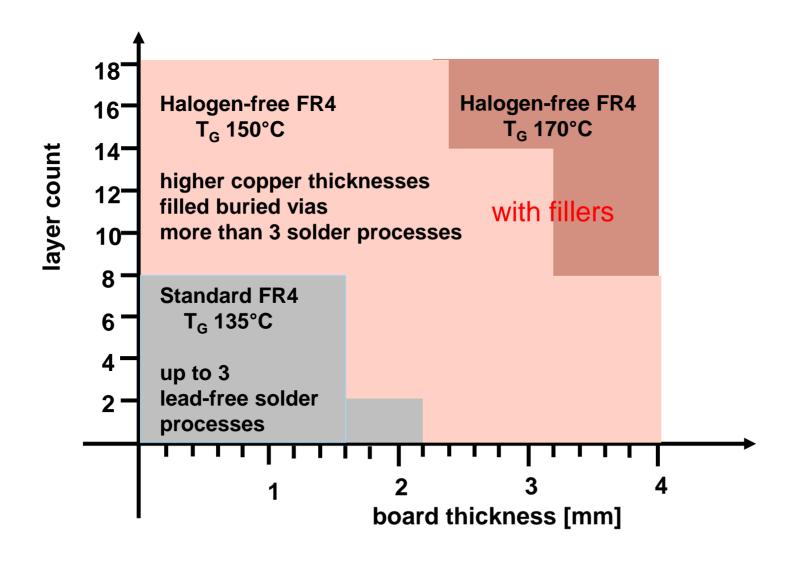
Requirements derived from the System

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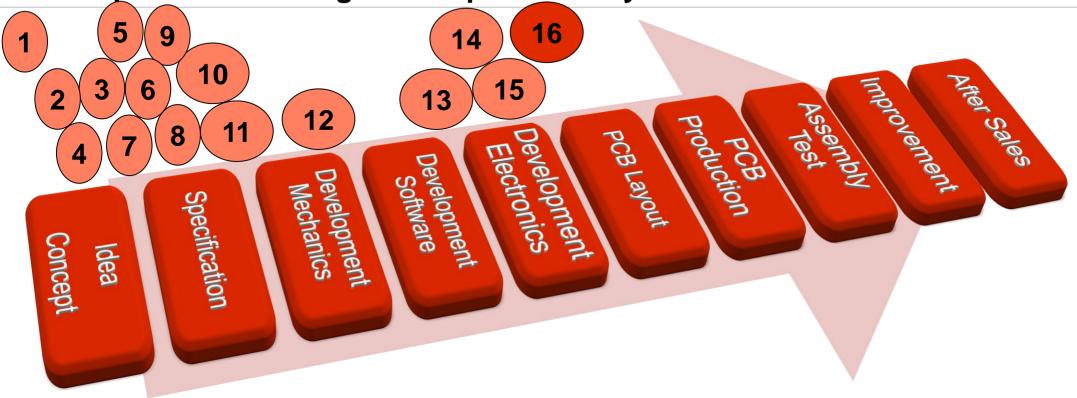


Recommendations for the usage of base material FR4



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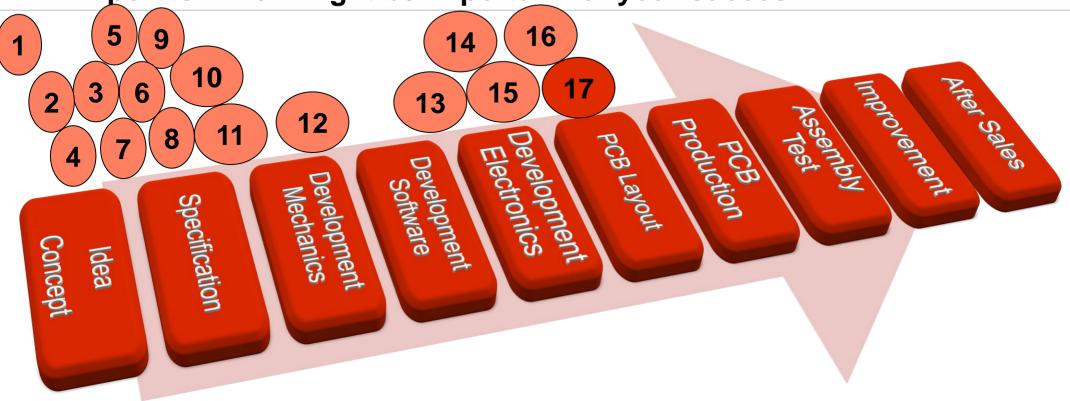
Qualification und Test Strategy

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Qualification of the pcb technology and ensuring of the serial quality

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Traceability

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Content and area needed for markings

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Marking: Must, may and Should

Must: Producer, Datecode

Should: Lot number

UL-Marking

Must: compay name or file number

Must: UL-Type designation

May: Factory identification

– May: UR-Logo

May: burning test classification



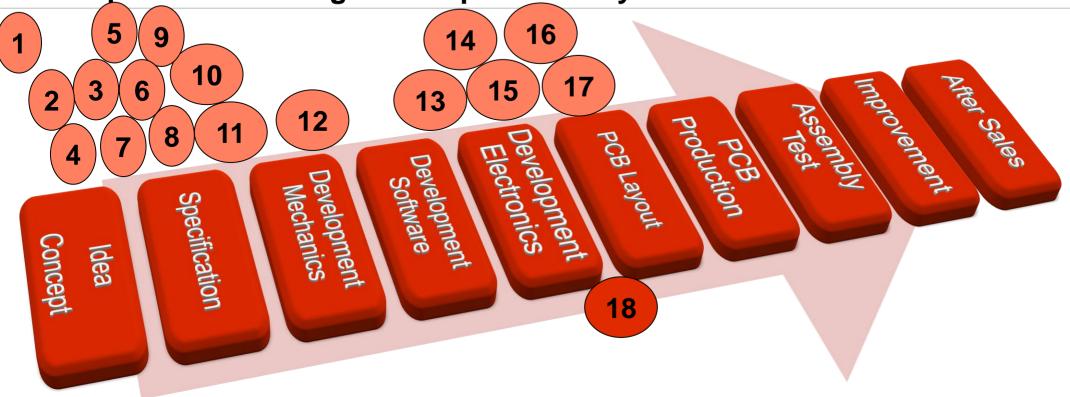


Marking: Company name or tradename "WE" or file number and type designation. May be followed by a suffix to denote factory identification or burning test classification.



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PCB Layout

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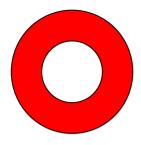
DfM, Design Rules, Annular Ring

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Why do we need annular rings?

Layout / Screen:



Real life



IPC-A-600H:

2.10 PATTERN DEFINITION - DIMENSIONAL

2.10.3 External Annular Ring - Supported Holes

2.10 PATTERN DEFINITION - DIMENSIONAL

2.10.3 External Annular Ring - Supported Holes (cont.)

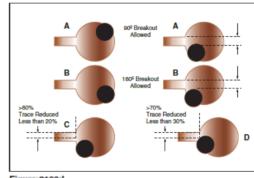


Figure 2103d

Acceptable - Class 2

- 90° breakout or less (see item A in Figure 2103d).
- If breakout occurs at the conductor to land junction area, the land/conductor junction is not reduced by more than 20% of the minimum conductor width specified on the engineering drawing or the production master nominal. The conductor junction should never be less than 0.050 mm [0.0020 in] or the minimum line width, whichever is smaller (see item C in Figure 2103d).
- . Minimum lateral spacing is maintained.

Acceptable - Class 1

- 180° breakout or less (see item B in Figure 2103d).
- If breakout occurs at the conductor to land junction area, the conductor is not reduced by more than 30% of the minimum conductor width specified on the production master nominal (see item D in Figure 2103d).
- · Form, fit and function are not affected.
- . Minimum lateral spacing is maintained.

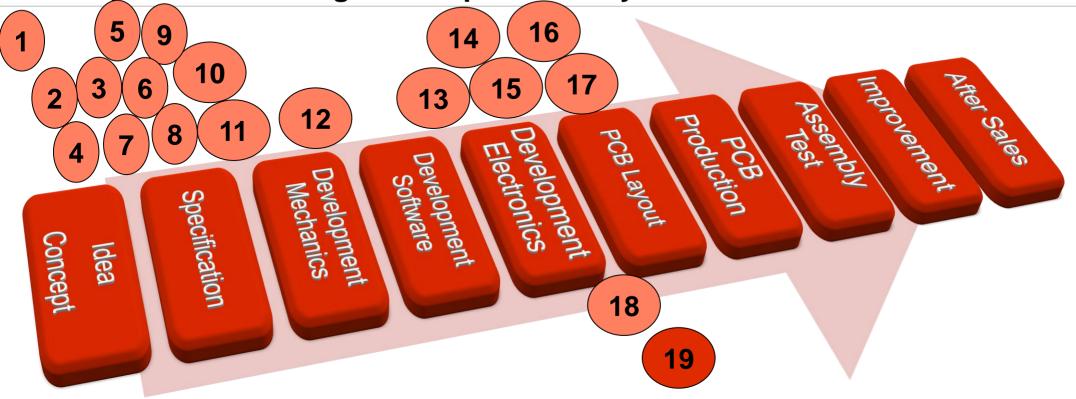
Nonconforming - Class 1, 2, 3

• Defects either do not meet or exceed above criteria.

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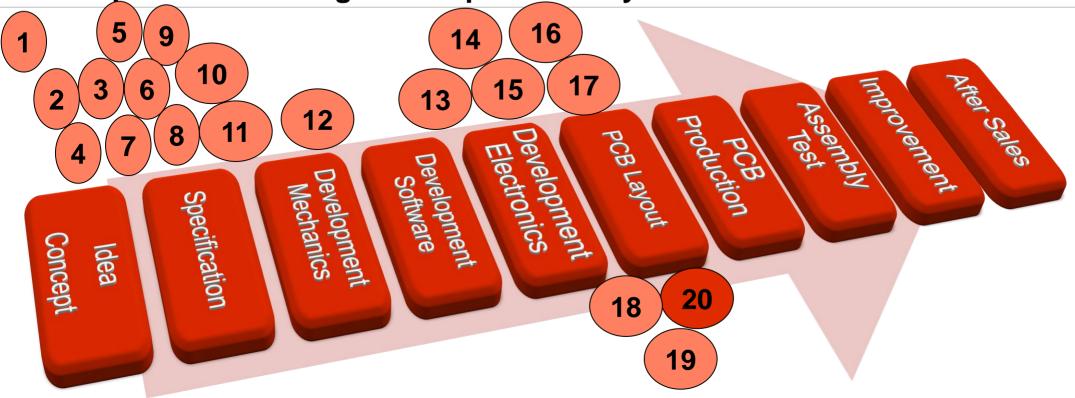
Data post processing and Design of delivery panel

Recommendation: Format 3.4 metric

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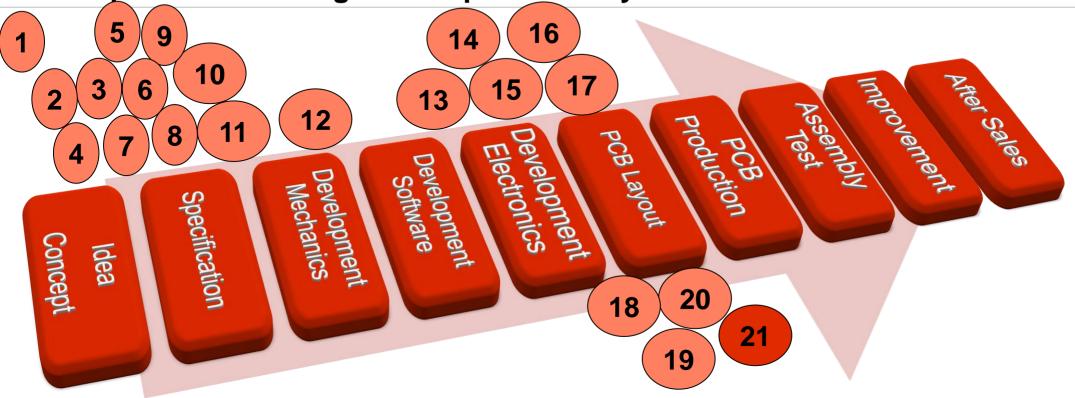
Order documents for the pcb bare board

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Gerber data, stack-up plan, drawings, Spezifications

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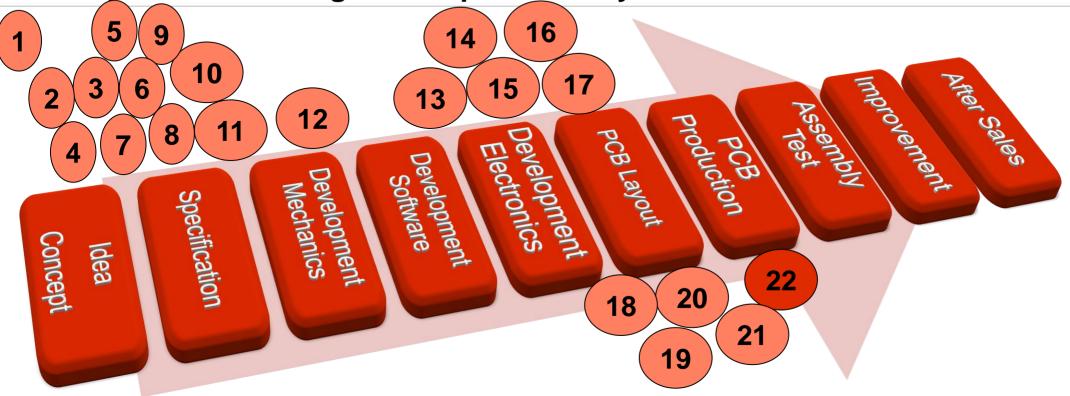
Production PCB bare board

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Rush service, Logistics solutions of Würth Elektronik, Shop WEdirekt

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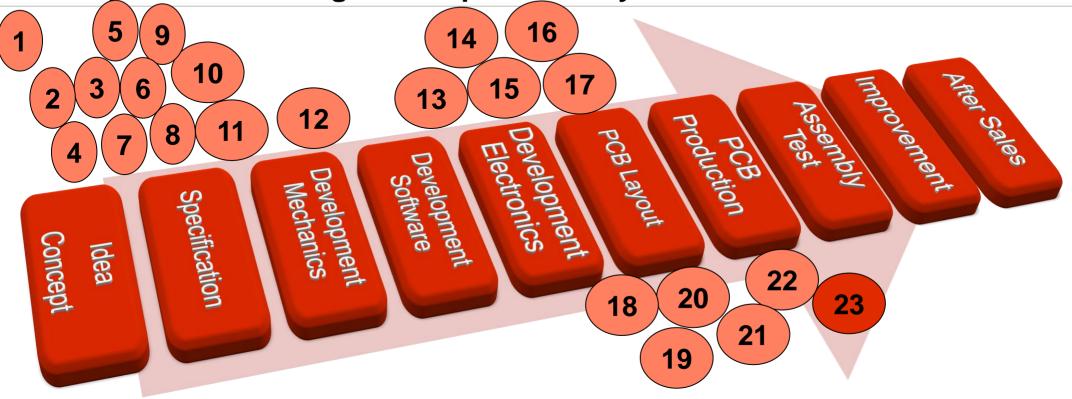
Delivery documents

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from delivery note to PPAP (Production Part Approval Process)

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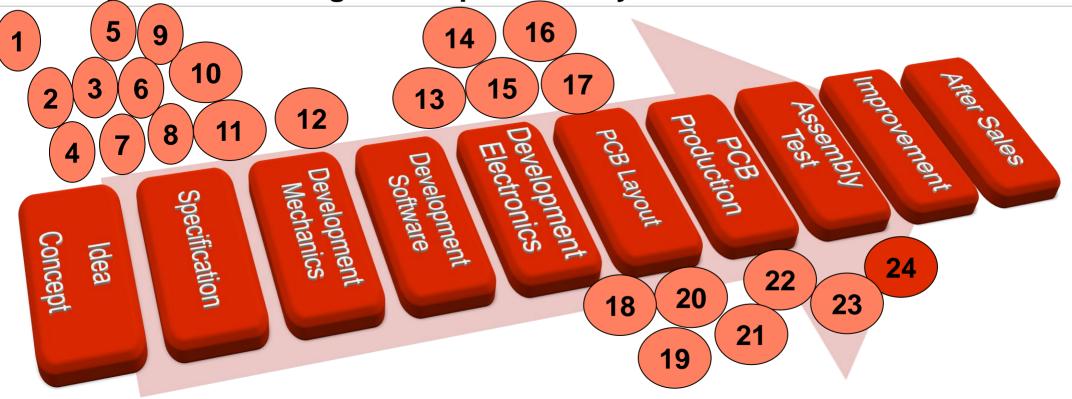
Further processing of the PCBs

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Download "Drying recommendations"

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Panel separation

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Which capabilities does your production have? Side cutter?

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Panel Separation - examples

several processes are in use:

- 1. Tab remover (i.e. Hektor) for cutting single tabs
- 2.cutting knife for V-cut panels (Rolling or fixed knifes)
- 3. Laser up to 0,8mm pcb thickness
- 4. Routing (expensive but good!)
- 5. Stamping or Sawing (for big volumes)
- 6. Cracking of predetermined breaking points

Ritznutzen / V-cut panels





Entfernung von Stegen / tab removal

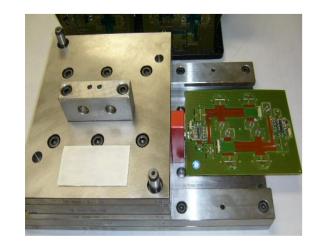




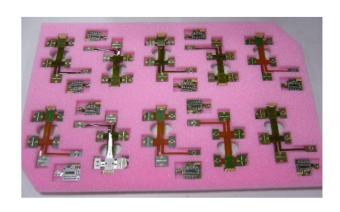
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Panel Separation by stamping - Transport

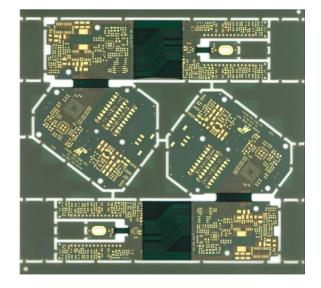






Quelle: Fa. acd





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Summary

the development of an electronic system

- could be very complex
- needs a lot of different technical disciplines
- needs networking and communication very much
- WE like to support you in a project
- You are already in a redesign or improvement loop?
 We are pleased to help you!
- Please contact us as soon as possible!



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Thank you very much for your attention!

this Webinar was presented by





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